Code No. : 5296/S

FACULTY OF INFORMATICS
B.E. 4/4 (IT) I Semester (Suppl.) Examination, June 2012
VLSI DESIGN

Time: 3 Hours] [Max. Marks : 75

Note : *Answer **all** questions from Part **A**. Answer **any five** questions from Part **B**.*

PART – A **(25 Marks)**

1. Explain VLSI design flow. **3**
2. Realize XNOR gate using transmission gates and FETs. **2**
3. What is meant by Bubble pushing ? **3**
4. Draw the layout for non-inverting buffer. **3**
5. Give the stick diagram for NAND-2 gate. **2**
6. What is the significance of gate delays ? **2**
7. Differentiate between carry look ahead and ripple carry adder. **2**
8. What is meant by clock skew ? Explain. **3**
9. Draw the pseudo nMOS circuit for f_2 (a.b) + (c.d). **2**
10. Draw XOR mirror circuit. What is the significance of mirror circuits ? **3**

PART – B **(50 Marks)**

11. a) Design a 4:1 MUX using three 2:1 TG multiplexors. **5**
    b) Derive FET capacitances. **5**
12. a) Define Latch up ? Why latch up occurs in CMOS circuits and explain the remedies for this latch up problem ? **5**
    b) Give RC model of a FET and explain. **5**

(This paper contains 2 pages)

P.T.O.

13. a) What is meant by photolithography ? Explain in detail. 5

    b) Discuss FET sizing and unit transistor. 5

14. a) Explain the principle of SRAM with neat circuit diagram. 5

    b) Explain tristate inverter circuits. 5

15. a) Construct a verilog module for 5-bit shift register. 5

    b) Explain floor planning and routing. 5

16. a) Differentiate between structural gate-level modeling and behavioral modeling. 5

    b) Discuss crosstalk in VLSI design. 5

17. Write short notes on the following : (5+5)

    a) Mirror circuits.

    b) High speed multipliers.
