FACULTY OF ENGINEERING

B.E. 2/4 (ECE) II – Semester (Main) Examination, May 2013

Subject: Pulse, Digital and Switching Circuits

**Time: 3 Hours**   **Max.Marks: 75**

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1.   State the clamping circuit theorem, what is its significance.   (3)

2.   Prove that a high pass RC circuit can function on a differentiator circuit.   (3)

3.   What is hysterisis in a Schmitt trigger circuit?   (2)

4.   What is a multivibrator? Give the applications of a monostable and astable
     multivibrators.   (3)

5.   State and prove Demorgan's theorems.   (3)

6.   Define Prime Implicants and Essential Prime Implicants.   (2)

7.   Explain the different hazards that occurs in combination logic circuits.   (2)

8.   Simplify the following Boolean expression $T(x,y,z) = \bar{x}\,\bar{y}\,z + yz + xz$. On which
     variable the output is dependent.   (2)

9.   Define state diagram and state table in FSM.   (2)

10. Design 3 bit binary to gray code converter.   (3)

PART – B (50 Marks)

11.(a) Sketch the output response for the following clipper circuit when the input is linearly
       varying from 0 to 150 V. Assume diodes are ideal.   (6)
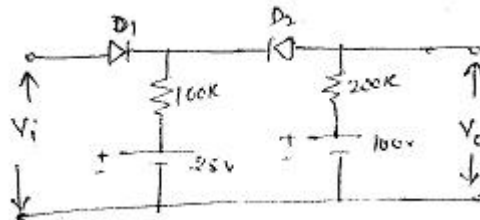
   (b) Draw the circuit diagram of compensated attenuator? Derive the necessary
       conditions for perfect attenuation of the compensated attenuator.   (4)

12.(a) Design an astable multivibrator to generate a 8 KHz squal wave with 70% duty cycle
       and amplitude of 8 V. Show the circuit diagram with all the wave forms.   (7)

   (b) Define the three types of errors that occurs in time base generators.   (3)

13.(a) Simplify the following Boolean functions by using quine Mc-Cluskey tabular method.
       $f(A_1B_1C_1D_1E) = \sum m\,(0, 2, 6, 8, 9, 13, 14, 15, 16, 19, 24, 27, 31)$.   (6)

   (b) Implement the following Boolean expression with the minimum no. of two input
       NAND gates.   (4)
 $f(A_1\,B_1\,C_1\,D) = (A + B') (C + D') (A' + C)$

14.(a) Design the 4 x 2 priority encode circuit and implement it with the logic gates. (5)

(b) What is race around condition? Explain how it is avoided by using master slave – JK flip flop. (5)

15.(a) Design mod 13 asynchronous counter and explain with the timing diagram. (7)

(b) Write the differences between synchronous counter and asynchronous. (3)

16. A sequential circuit has one input and one output. The state diagram is shown in Fig. Design the sequential circuit with 'D' flip flops. (10)
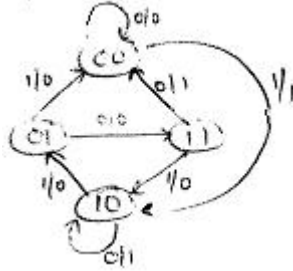
17. Write short notes on: (10)
   a) Regenerative comparator
   b) UJT
   c) Contact networks.

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