c) A 4-bit ring counter and a 4-bit Johnson counter are in turn clocked by a 10 MHz clock signal. Determine the frequency and duty cycle of the output flip-flop in the two cases.

d) Design a 3-bit binary counter using TFF that has a repeated sequence of 6 states.

000-001-010-011-100-101-110. Give the state table, state diagram and logic diagram.

OR

Design a synchronous Mod-6 counter using JKFF.

5. a) Draw the static and dynamic RAM cells.

b) What is access time and cycle time of a memory.

c) Implement the function

$F_1 = \Sigma\,(0, 1, 2, 5, 7)$ and

$F_2 = \Sigma\,(1, 2, 4, 6)$

using PROM.

d) Describe with the help of a schematic diagram, the operation of a tracking-type A/D converter. Explain how it over comes the inherent disadvantage of a longer conversion time of the conventional counter-type A/D converter.

OR

Draw a PLA circuit to implement the function.

$F_1 = \overline{A}B + A\overline{C}$

$F_2 = \overline{(AC + AB + BC)}$

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Roll No ....

EX-403

B.E. IV Semester

Examination, December 2015

Digital Electronics Logic Design - I

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

1. a) i) Convert $(2F.C4)_{16} = (\quad)_8$

ii) Convert $(762.013)_8 = (\quad)_{16}$

b) The 7's complement of a certain octal number is 5264. Determine the binary and hexadecimal equivalents of that octal number.

c) Draw logic implementation of a EX-OR using NOR only.

d) Minimize the Boolean function

$f(A, B, C) = \Sigma_m\,(0, 1, 3, 5) + \Sigma_d\,(2, 7)$

using the mapping method is minimized SOP form.

OR

Simplify the expression

$$\overline{\overline{AB+ABC}+A(B+A\overline{B})}$$

and implement the simplified function using gates.

2. a) Design Half-adder using only NAND gates.

   b) Implement full adder using multiplexer.

   c) Design a three bit even parity generator.

   d) Draw and explain the BCD adder circuit.

OR

Implement the 3-variable Boolean function

$F(A, B, C) = \overline{A}.C + A.\overline{B}.C + A.B.\overline{C}$

Using i) 8 to 1 multiplexer and

ii) 4 to 1 multiplexer.

3. a) Draw the state diagram and characteristics equation of a D-FF.

   b) What is latch? What is the difference between latch and flip-flop?

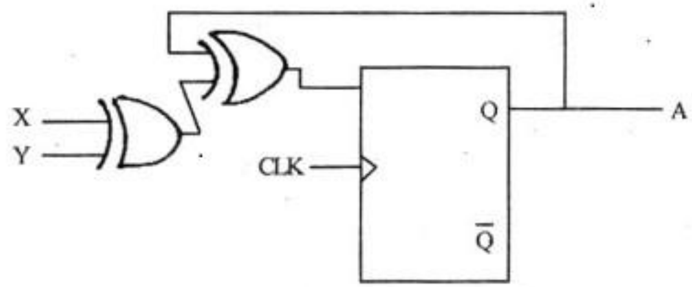
   c) Realize T-flip-flop using SR flip-flop.

   d) Reduce the number of states in the following state table, and tabulate the reduced state table.

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

OR

Analyze the synchronous sequential logic circuit and derive the transition table and state diagram.



4. a) Differentiate Asynchronous and Modulus Counter.

   b) Determine the number of flip-flops required to construct.

      i) a Mod-10 ring counter and

      ii) a Mod-10 Johnson counter