B.E/B.TECH (FULL-TIME) DEGREE EXAMINATIONS, APRIL/MAY 2012

ELECTRONICS AND COMMUNICATION ENGINEERING

IV SEMESTER

EC9255 – COMPUTER ARCHITECTURE & ORGANIZATION

(REGULATIONS 2008)

Time: 3 hours Maximum Marks: 100

Answer ALL questions

PART A – (10 X 2 = 20 marks)

1. What are the different factors to be considered while designing the instruction format?
2. Give the IEEE format of single precision and double precision floating point representation.
3. Draw the data path required to implement 4 bit addition/Subtraction.
4. From the truth table of full adder justify the terms propagate and generate of the carrys.
5. List out the advantages and disadvantages of hardwired control over microprogrammed control.
6. Derive the speedup formula for a pipeline processor over a uniprocessor
7. Sketch the hierarchical memory organization and discuss.
8. How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
9. What are the basic functionalities that should be performed by I/O interface?
10. Write short notes on vectored interrupts.

PART B – (5 X 16 = 80 marks)

11 (a) (i). Explain the Booth's algorithm with a neat flow chart and draw the necessary hardware components. (8)

(ii). Compute 110011 X 110110 by using Booth's algorithm. Use 8 bit representation (8)

12 (a). What is meant by addressing mode? Explain the various addressing modes with example instructions. Also discuss the importance of each of the addressing mode?

(OR)

(b). With a Schematic diagram, explain the organization of CISC machine 68020

13 (a) (i).Give the organization of a microprogrammed control unit and explain its operation. (8)

(ii). Explain with diagram how the conditional branching is taken care in microprogrammed control unit. (8)

(OR)

(b) (i). Design a hardwired control unit of a processor with 5 instructions of your choice including a conditional branch instruction. Draw the necessary logic diagram. (12)

(ii). Explain the concept of nano programmed control unit. (4)

14 (a) (i). Discuss locality of reference, spatial locality, temporal locality, write through and write through with reference to cache memory organization. (8)

(ii). Explain the different types of cache mapping techniques. (8)

(OR)

(i) Discuss the concept of virtual memory and explain how virtual address is converted to physical address. (8)

(ii) A digital computer has a memory unit of 64K X 16 and a cache memory of 1 K words. The cache uses direct mapping with block size of four words. How many bits are there tag, block and word fields of the address format?. How many blocks can the cache accommodate? (8)

15 (a) (i) What is the need for a DMA transfer?. Explain how DMA operation takes place. (12)

(ii) Distinguish between memory mapped I/O and I/O mapped I/O. (4)

(OR)

(b). Write detailed notes on the following:

(i) Bus Arbitration methods
(ii) Multiprocessors
(iii) Comparison of RISC and CISC processors.
(iv) PCI Interrupt

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