BTS(C) – III – 08 – 067 – A

B. Tech Degree III Semester Examination, November 2008

IT 306 COMPUTER ORGANISATION

(2006 Scheme)

Time : 3 Hours | Maximum Marks : 100

PART A

(Answer ALL questions)

(8 x 5 = 40)

I. (a) What is a stack? Explain the stack operations with example.

(b) Explain the terms Hardware, Software and relate them.

(c) Define Guard Bits. Specify the different truncation methods. What is the default mode for truncation specified in IEEE floating point standard?

(d) Explain the following:
(i) Prefetching (ii) Emulation

(e) Explain the following terms:
(i) Dirty Bit (ii) Hit rate
(iii) Miss penalty (iv) Write through protocol
(v) Write back protocol

(f) Draw the internal organization of a static RAM cell and explain its read and write operations.

(g) Differentiate between memory mapped I/O and I/O mapped I/O.

(h) What is DMA? Explain its operation.

PART B

(4 x 15 = 60)

II. (a) Draw the internal structure of a processor and show the connections between the processor and memory. Explain the functional details of each block. (10)

(b) What is an assembly language? Specify its advantages and disadvantages over high level language. (5)

OR

III. (a) What is meant by addressing mode? Explain with example the commonly used addressing modes in general purpose computers. (10)

(b) Specify the basic instruction types and explain with example. (5)

IV. (a) Draw and explain the Hardwired Control unit organization. (10)

(b) Write the control sequence for execution of the instruction Add (R3), R1. (5)

OR

V. (a) Explain Booth's algorithm with an example. (8)

(b) Show the logic circuit arrangement that implement restoring division and explain it with an example. (7)

VI. What is virtual memory? Explain with diagram how address translation is taking place in it. (15)

OR

VII. Discuss the various mapping functions used in cache memory with neat diagrams. (15)

VIII. What is an interrupt? Explain the following with neat diagrams.
(i) Vectored Interrupt (b) Interrupt Nesting (15)

OR

IX. Explain the following standard I/O interfaces and show the sequence of events on bus.
(i) PCI Bus (ii) SCSI Bus (15)

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