Roll No.

B.E. (Full-time) DEGREE END SEMESTER EXAMINATIONS, Nov / Dec 2011

ELECTRICAL & ELECTRONICS ENGINEERING,

Seventh Semester (Regulation 2004)

EE 471 - Digital Signal Processors

Time : 3 hr

Answer ALL questions

Max. marks : 100.

$PART - A (10 \times 2 = 20)$

- 1. What is a single-pole recursive low pass filter?
- 2. The signal $y(t)=3\cos(\pi t)+6\cos(9\pi t)$ is sampled at a frequency of 5 Hz. Plot the frequency spectrum and mark the aliasing frequency?
- 3. Name the important functional units of a Data Address Generator unit?
- 4. What are the computational savings in evaluation of DFT using radix-2 FFT algorithms?
- 5. Represent the floating point number 2.875 in IEEE single precision standard format?
- 6. Why is it necessary to provide 'guard bits' in the accumulator?
- 7. Comment on the location of zeros of anyone type of FIR filter?
- 8. Illustrate through a neat diagram how adaptive filtering is useful in system identification?
- 9. Name atleast three peripherals that are important for implementation of a DSP algorithm? Also, justify each in a line or two.
- 10. Distinguish between the architectural features of a Digital Signal Processor and a Micro-controller?

$PART - B (5 \times 16 = 80)$

- 11. What is an adaptive filter? Discuss the basics of Least Mean Square algorithm for filter parameter adaptation. Write a program for implementing an adaptive FIR filter. You may assume anyone Digital Signal Processor, but employ the Least Mean Square algorithm.
- 12. a) i)Distinguish between a Braun's multiplier and a Baugh–Wooley multiplier. (3)
 ii) Draw the hardware block diagram of a barrel shifter, capable of performing left shift of a given 4-bit unsigned number. (3)

iii) By means of DFT and IDFT, determine the sequence x(n) corresponding to the circular convolution of the sequences $x_1(n)$ and $x_2(n)$ given by,

 $x_1(n) = \{3210\},$ and $x_2(n) = \{1230\}.$ Also verify your answer by directly performing the circular convolution. (10)

OR

b) i) Write a MATLAB program for rearranging the elements of a given vector in bit reversed sequence, after performing zero-padding to make the vector size equal to the next higher 2^n . (8)

ii) Find the 8-point DFT of $x[n] \approx (0 \ 1 \ 2 \ 3 \ 3 \ 2 \ 1 \ 0)$, by employing butterfly structure and DIT. Also verify your answer by any other method. (8)

13. a) i) Design a digital Butterworth low pass filter that satisfies the constraints: 0.75 < |H(e^{jw})| < 1, for 0 < w < 0.2π, and |H(e^{jw})| < 0.35, for 0.6π < w < π. Use bilinear transformation and assume T = 1 sec. (8)
ii) Write a program for generating Pseudo Random Bit Sequence. You may use the fixed point Digital Signal processor TMS320C2407 or floating point Digital Signal processor TMS320C2407 or floating point Digital Signal processor TMS320C30. Add comments to your program, briefly explaining the algorithm employed. (8)

OR

b) i)Discuss the methodology for FIR filter design using 'windowed sinc filter'. Also distinguish between Hamming and Hanning windows.
(6)
ii) Write down the program for IIR filter using the floating point Digital Signal processor TMS320C30 and discuss the working principle of the program. (10)

14. a) i) What is 'bit reversed addressing' mode? How is it helpful in the implementation of real-time applications?

ii) Along with a block diagram of the event manager A of TMS320C2407, discuss its features. Write a program for generating a square waveform, at T1PWM pin and also at PWM1 pin. (9)

OR

b) i) What is 'circular buffer'? How is it helpful in the implementation of real-time applications? (7)

ii) Explain how convolution sum can be computed using the instruction MAC by writing a program. What is the extra operation performed by MACD instruction when compared to MAC instruction? How is this used in real-time applications? (9)

15. a) Discuss the architecture and features of anyone fixed point or floating point Digital Signal processor chip. Also discuss the operation of any two of its instructions..

OR

b) Write down the difference equation defining Fibonacci series. Employing unilateral Z-transform technique, solve it and obtain a generic expression for the n^{th} element of Fibonacci series. Also write a program in anyone Digital Signal Processor for generating the first ten elements of the Fibonacci series.