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FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2011

EE 09 405/PTEE 09 404—DIGITAL ELECTRONICS

(2009 Admissions)

Time: Three Hours

Maximum: 70 Marks

Part A

- 1. Define Propagation Delay.
- 2. Give the truth table of NAND and XNOR gate.
- 3. Differentiate between Combinational logic circuit and Sequential logic circuit.
- 4. How is JK FF converted to T FF?
- 5. What is the function of program counter?

 $(5 \times 2 = 10 \text{ marks})$

Part B

- 6. Compare CMOS and TTL technologies based on power dissipation voltage levels, noise immunity.
- 7. Perform the following operations in two's complement form:
 - (i) $-36_{\rm H} + 4 \, \rm D_{\rm H}$.
 - (ii) $-AF_H 6C_H$.
- 8. Draw the circuit of a full adder along with truth table.
- 9. Explain the 4-bit comparator circuit.
- 10. Draw and explain a static RAM cell and a dynamic RAM cell.
- 11. List the salient features of 8085 microprocessor.

 $(4 \times 5 = 20 \text{ marks})$

Part C

12. (a) Discuss the operation of CMOS inverter circuit with characteristics.

Or

- (b) Explain the schematic of 3 input TTL NAND gate.
- 13. (a) Construct a truth table for BCD to gray code converter and draw the simplified circuit schematic (Use Karnaugh map).

Or

(b) (i) Differentiate between ROM, PLA and PAL.

(4 marks)

(ii) Implement a 4 × 1 multiplexer in the above 3 methods.

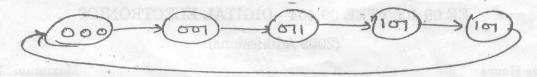
(6 marks)

Turn over

14. (a) Explain the operation of bidirectional shift register.

Or

(b) Design a synchronous counter for the state diagram given below:



Use D flip-flop.

- 15. (a) (i) Discuss the basic microcomputer operations.
 - (ii) What are the various flags available and state their uses.

Or

(b) Write the VHDL code, using structural modelling for a full subtractor.

 $(4 \times 10 = 40 \text{ marks})$

(a) $(a \times 2 = 10)$ marks)

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(ii) Implement a 4 × 1 multiplexer in the above 3 methods

Turn over