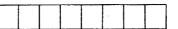
Reg. No.





B. Tech. Degree III Semester Examination November 2014

CS 1302 LOGIC DESIGN

(2012 Scheme)

Time: 3 Hours

Maximum Marks: 100

PART A (Answer ALL questions)

 $(8 \times 5 = 40)$

I. (a) Simplify the expression using K.map $F = \Sigma m(1,5,6,12,13,14) + al(2,4)$

Convert the decimal number 27.315 to binary and then to octal. (b)

- Design half adder and full adder using NOR gates only. (c)
- Design a circuit to convert binary to excess-3. (d)
- What is a Johnson counter? Explain with diagram. (e)
- (f) Explain what is meant by PAL & PLA.
- Explain how TTL to CMOS interface can be done. (g)
- (h) Differentiate between RTL and DTL.



PART B

 $(4 \times 15 = 60)$

- II. Represent the decimal number 5, 137 in (i) BCD (ii) excess 3 code (iii) 2421 and (5) (iv) 6311.
 - Consider the minimization of the following using Quine McCluskey method (10)(b) $f(x_1 x_2 x_3 x_4) = \Sigma_m(0,5,7,8,9,10,11,14,15)$

- III. Prove the theorems of boolean algebra by using postulates. (15)
- IV. (15)Implement the function using a multiplexer $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$

V. Design a 4-bit carry look ahead adder and explain the operation. What is the number (15)of gate delays involved in the circuit?

- VI.
 - Design a synchronous confer to generate the following sequence 0-1-3-5-7. (10)(a) (b) Draw the diagram of a BCD counter using J-K flip flop and explain briefly. (5)

(15)

VII. Explain with diagram the working of (i) ripple counter (ii) ring counter (iii) Synchronous counter.

- VIII. Explain with circuit diagram a typical 2 input TTL NAND gate (7)
 - Define the terms. (i) Fan out (ii) Noise margin (iii) Propagation delay (iv) Power (8) dissipation.

IX. Explain the operation of a 2 input CMOS NOR gate and CMOS inverter in detail. (15)