BTS.III.11.14.0946 Reg. No. | | | | | | | | |

B

B.Tech. Degree III Semester Examination November 2014

CS 1302 LOGIC DESIGN

(2012 Scheme)

Time : 3 Hours Maximum Marks : 100

PART A

(Answer *ALL* questions)

(8 × 5 = 40)

I. (a) Simplify the expression using K.map $F = \Sigma m(1,5,6,12,13,14) + al(2,4)$

(b) Convert the decimal number 27.315 to binary and then to octal.

(c) Design half adder and full adder using NOR gates only.

(d) Design a circuit to convert binary to excess-3.

(e) What is a Johnson counter? Explain with diagram.

(f) Explain what is meant by PAL & PLA.

(g) Explain how TTL to CMOS interface can be done.

(h) Differentiate between RTL and DTL.

PART B

(4 × 15 = 60)

II. (a) Represent the decimal number 5, 137 in (i) BCD (ii) excess 3 code (iii) 2421 and (iv) 6311. (5)

(b) Consider the minimization of the following using Quine McCluskey method (10)

$f(x_1 x_2 x_3 x_4) = \Sigma_m(0,5,7,8,9,10,11,14,15)$

OR

III. Prove the theorems of boolean algebra by using postulates. (15)

IV. Implement the function using a multiplexer $F(A,B,C,D) = \Sigma(1,3,4,11,12,13,14,15)$ (15)

OR

V. Design a 4-bit carry look ahead adder and explain the operation. What is the number of gate delays involved in the circuit? (15)

VI. (a) Design a synchronous confer to generate the following sequence 0-1-3-5-7. (10)

(b) Draw the diagram of a BCD counter using J-K flip flop and explain briefly. (5)

OR

VII. Explain with diagram the working of (i) ripple counter (ii) ring counter (iii) Synchronous counter. (15)

VIII. (a) Explain with circuit diagram a typical 2 input TTL NAND gate (7)

(b) Define the terms. (i) Fan out (ii) Noise margin (iii) Propagation delay (iv) Power dissipation. (8)

OR

IX. Explain the operation of a 2 input CMOS NOR gate and CMOS inverter in detail. (15)

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