M 26154

Reg. No. : .....

Name : .....

VII Semester B.Tech. Degree (Reg./Sup./Imp. – Including Part Time) Examination, November 2014
(2007 Admn. Onwards)
PT 2K6/2K6 EC 701 : MICROELECTRONICS TECHNOLOGY

Time : 3 Hours Max. Marks : 100

PART – A

I. a) Briefly explain MTF.

b) Explain subtractive etching and additive etching with neat diagrams.

c) What is subthreshold conduction ?

d) Explain the VTC of pnedo nMOS inverter.

e) Briefly explain different layers of MOS.

f) Briefly explain MOS capacitor.

g) Why device isolation is required ? Explain junction isolation.

h) Briefly explain electron spin transport. **(8×5=40)**

PART – B

II. a) Explain three types of photolithographic printing techniques. **15**

OR

b) With a neat diagram, explain CVD process for Si in detail. **15**

III. a) With proper diagrams explain the process detail of nMOS transistor. **15**

OR

b) Explain with neat diagram the process sequence of Bi CMOS transistor. **15**

P.T.O.

IV. a) Give the stick diagram of NAND using nMOS and static CMOS design style with stick diagram and its ckt diagram. **15**

OR

b) Give the stick diagram and ckt diagram of 2 input XNOR using static nMOS and CMOS design style. **15**

V. a) Write short note on :

i) LOCOS. **7**

ii) SMAMI. **8**

OR

b) Write short notes on :

i) Junction isolation and Trench isolation. **10**

ii) Ballastic nano transistor. **5**