SE | ETRX | IV (Rev.) 21 | 5 | 2012

Digital System Design - II

PH March Exam (4) 129

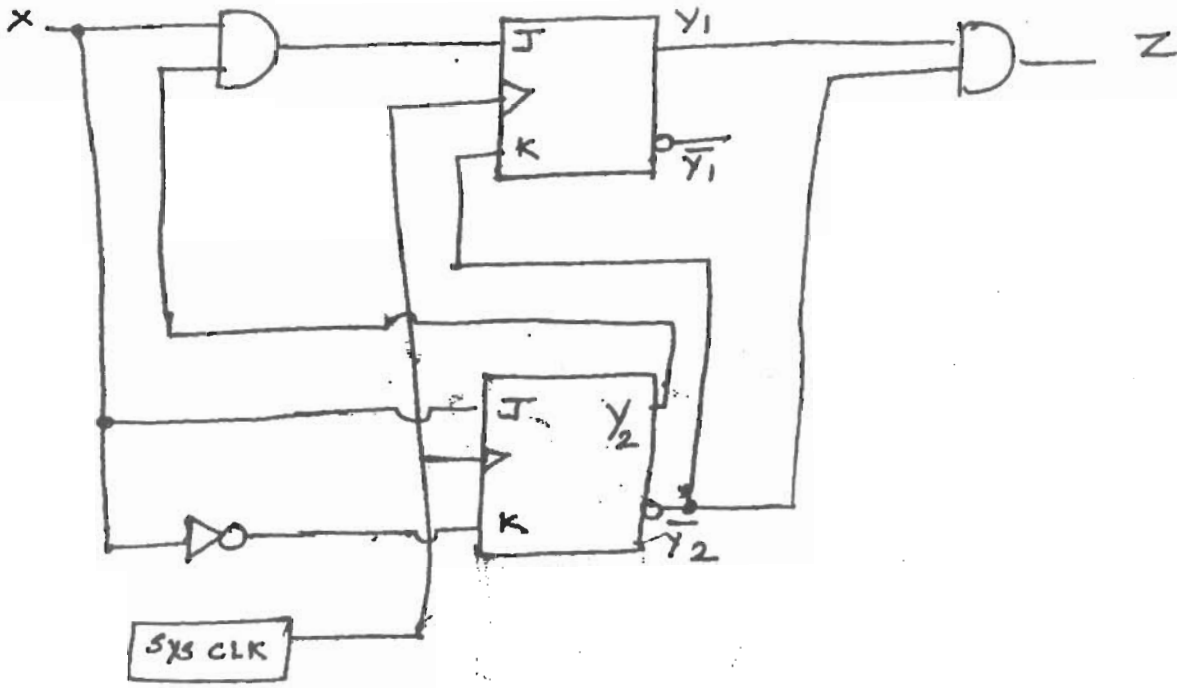
Con. 3790-12.

GN-5519

(3 Hours) [Total Marks : 100

N.B. (1) Question No. 1 is **compulsory**.
(2) Answer any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicates **full** marks.
(4) Assumptions made must be **clearly** stated.

1. (a) 10



Analyze the sequential M/c and draw the state diagram.

(b) Write V.H.D.L. code for full adder using half adder as component. 10

2. (a) Write behavioural description code of simple 11 bit floating point encoder. 10
(b) Write a V.H.D.L. code for multiplexer IC 74151. 10

3. (a) Reduce the state table using implication chart method and design state machine using D F/F and decoder. 10

Present state	Next state		O/P (z)	
	x = 0	x = 1	x = 0	x = 1
S_0	S_4	S_3	0	1
S_1	S_5	S_3	0	0
S_2	S_4	S_1	0	1
S_3	S_5	S_1	0	0
S_4	S_2	S_5	0	1
S_5	S_1	S_2	0	0

(b) Design MOD 16 counter using IC 74169 and SSI package using following counting sequence. . . . . 7, 6, 5, 4, 3, 2, 1, 0, 8, 9, 10, 11, 12, 13, 14, 15, 7, 6, ... 10

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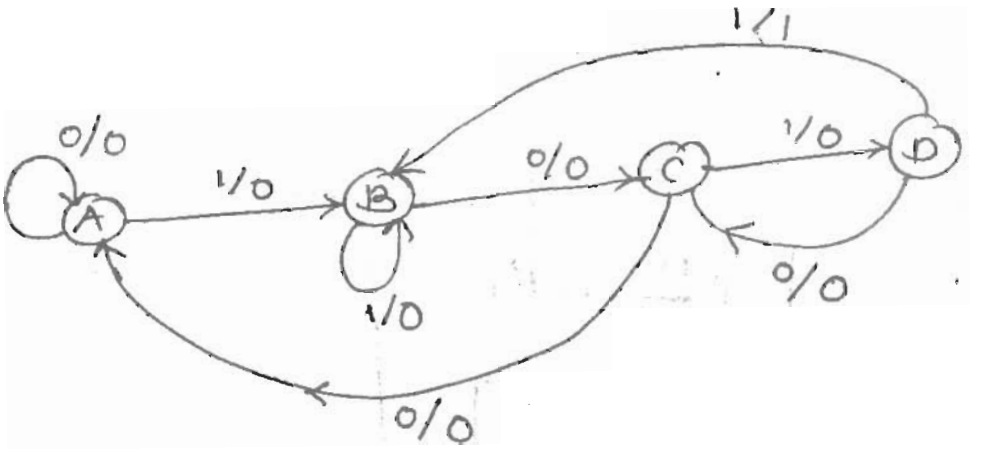
4. (a) Design a Moore sequential machine that detects serial I/P of 010110. Use suitable F/F's and logic for designing. 10
(b) Describe a State Machine shown below in V.H.D.L. 10



5. (a) Design a coin operated vending machine that dispenses Candy under the following conditions– 10
(i) The machine accepts ₹ 5 and ₹ 10 coins.
(ii) It takes ₹ 15 for one piece of candy to be released from the machine.
(iii) If ₹ 20 is deposited the machine will credit the buyer with ₹ 5 and wait for the buyer to make second purchase.
Design using Mealy Machine.
(b) Design MOD 193 counter with the counting sequence . . . . . 63, 64, 65, ... 254, 255, 63, 64, ... use IC 74163. 10

6. (a) Draw and explain Logic diagram of 64 × 1 diode ROM. Use 2-dimensional decoding. 10
(b) Write V.H.D.L. code for JK F/F. Use Asynchronous preset and synchronous clear. 10

7. (a) Explain the working of CPLD XC 9500 in detail. 10
(b) Analyze the pulse mode asynchronous sequential machine and obtain the state diagram. 10