M 23190

Reg. No. : .....

Name : .....

IV Semester B.Tech. Degree (Reg./Sup./Imp. – Including Part Time) Examination, May 2013
(2007 Admn. Onwards)
PT2K6/2K6EC 406 : DIGITAL ELECTRONICS

Time: 3 Hours Max. Marks: 100

Instruction : *Answer* ***all*** *questions.*

PART – A

1. a) If $(982)_{10} = (1726)_x$, what is x ?

   b) Implement f(A, B, C) = $\sum$0, 1, 3, 4, 7 using 4 to 1 MUX.

   c) What is static-1 hazard ?

   d) Prove that a full adder is equal to the sum of two half adders.

   e) What is a Moore machine ?

   f) What is a state diagram ? How do you draw a state diagram for a given circuit.

   g) What are the advantages of CMOS gates.

   h) Compare TTL, CMOS and ECL logic families with respect to their applications.

(8×5=40)

PART – B

2. a) Construct 3 × 1 MUX using 2 × 1 Muxes. **15**

   OR

   b) Simplify P = π (0, 1, 2, 3, 8, 9, 10, 13, 15) using k-map and implement the circuit using logic gates. **15**

P.T.O.

3. a) Draw the circuit of JK master slave flip flop and explain its mode of operation. **15**

OR

b) Draw the circuit of a Mod-5 asynchronous counter. Explain its operation with the timing diagram. **15**

4. a) What is clock skew ? Briefly describe the different methods that are used to avoid clock skew in a circuit. **15**

OR

b) What is a state table ? How do you design a circuit when a state table is given. **15**

5. a) Briefly describe the characteristics of RTL families. **15**

OR

b) Briefly describe the characteristics of DTL families. **15**