



GROUP - B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Design a 2 bit comparator using logic gates.
3. Design a BCD adder circuit to add two BCD numbers maximum. The output of the adder should also be in BCD.
4. Minimize the following expressions using *K* map :

$$F (A, B, C, D) = \pi M (0, 7, 8, 9, 10, 11, 15) + \phi (1, 4)$$
5. Implement the function using only one 8 : 1 max. Connect BCD with selection line.

$$F (A, B, C, D) = \sum m (0, 1, 2, 5, 9, 11, 13, 15)$$
6. What is 'race around problem' ? How can it be overcome in JK flip-flop ?

GROUP - C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

7. a) Simplify the following functions by means of *K*-map :
 i) $F = \sum m (0, 2, 6, 10, 11, 12, 13) + \sum d (3, 5, 14)$.
 ii) $F = \prod M (0, 2, 6, 10, 11, 12, 13) . \sum d (6, 8, 10, 14)$.
 b) Design a common adder-subtractor and explain its function. $5 + 5 + 5$
8. a) Write down the present state-next state table of JK & D flip-flops and derive the characteristic equation for these two flip-flops.
 b) Draw logic diagram of the master-slave flip-flop. Why is it called so ?
 c) What are the differences between edge triggered and level triggered flip-flop. $(3 + 3) + 5 + 4$



9. a) Describe the operation of successive approximation type ADC. How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type ADC ?
- b) Draw a neat diagram for an R-2R ladder type DAC and explain its operation. 7 + 8
10. a) Draw the circuit for a 4-bit Johnson counter using *D* flip-flop and explain its operation. Draw its timing diagram. How does its timing diagram differ from that of Ring counter ?
- b) Design a MOD-6 synchronous up-counter using JK flip-flop. 8 + 7
11. Write short notes on any *three* of the following : 3 × 5
- a) EEPROM
 - b) CMOS logic
 - c) PLD
 - d) Even parity generator & checker
 - e) Comparator.
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