T.E (ETRX) V 22/5/13
up & MC I.

65 : 1st half.13-shilpa(scan) (a)

Con. 9300-13. **GS-8985**

(3 Hours) **[Total Marks : 100**

N.B. 1. Question no. 1 is compulsory.
2. Answer any four questions from remaining six questions.
3. Assume suitable data if necessary.

Q.1.	a.	Explain following signals of 8085 1) ALE, 2) READY 3) INTR	05
	b.	Explain addressing modes of 8085.	05
	c.	Explain different assembly directives of 8051.	05
	d.	Explain control word of 8255.	05
Q.2.	a.	Explain interrupt structure of 8051.	10
	b.	Explain different modes of operation of 8254.	10
Q.3.	a.	Explain register architecture of ARM processor.	10
	b.	Explain architecture of 8051 with neat diagram.	10
Q.4.	a.	Explain interfacing of 8259 with 8085 showing decoding logic.	10
	b.	Explain architecture of 8051.	10
Q.5.	a.	Write assembly language program to read 4 x 4 keyboard interfaced through 8255.	10
	b.	Explain interfacing of external memory with 8051.	10
Q.6.	a.	Compare variants of 8051 such as 89C51, 89C52, 89C2051 and 89C2052.	10
	b.	Explain different I/O mapping techniques. Give suitable example.	10
Q.7.	Write short note :		
	a.	Serial communication supported by 8085	05
	b.	Program Status Word of 8051	05
	c.	Interrupt acknowledge bus cycle of 8085	05
	d.	Instruction set of 8085	05