

(3 Hours)

[Total Marks : 100

- N.B. :** (1) Question No. 1 is compulsory.
 (2) Attempt any four from remaining six questions.
 (3) Make suitable assumptions wherever necessary.

1. Each question carries equal marks. 20marks
 - a) Draw re model and h model for CE amplifier configuration.
 - b) Investigate the effect of I_B on the performance of the inverting amplifier, if $I_B = 10\text{nA}$ and all resistances are $100\text{k}\Omega$. What dummy resistance R_p must be installed in series with the non inverting input to minimize E_O ?
 - c) List features of IC 723 regulator.
 - d) Explain two static and two dynamic parameters of OP_AMP.
 - e) Why voltage divider biasing is widely used? Give reason.

2. a) Draw the circuit diagram of 3 OP_AMP Instrumentation amplifier using IC741. Explain its requirements, applications and its advantages over difference amplifier. 12marks
 b) Derive equations for Z_i , Z_o and A_v for CE amplifier using voltage divider network (with unbypassed RE). 08marks

3. a) Why in an emitter coupled differential amplifier RE resistor is replaced by a constant current source? Draw such circuit. Explain how this network acts as a constant current source (I_o). 10marks
 b) For n-channel FET (unbypassed R_S) with $R_1=910\text{k}\Omega$, $R_2=110\text{k}\Omega$, $R_D=2.2\text{k}\Omega$, $R_S=510\Omega$, $I_{DSS}=5.8\text{mA}$, $V_P=-3\text{V}$ and $V_{GSS}=-2\text{V}$. Find I_D , V_{GS} , V_G , V_D , V_S and V_{DS} . 10marks
 Note: [for common source circuit]

4. a) Design a monostable multivibrator to generate a pulse of 1.1ms . Draw circuit diagram with trigger circuit and waveforms obtained at pin.3 and across capacitor. 10marks
 b) Draw and explain the working of R_2R ladder network and the following terms: 10marks
 - i. Resolution
 - ii. Offset voltage
 - iii. Full scale voltage

5. a) Draw and explain the block diagram of IC 723 regulator and also explain the need of short circuit protection circuitry. 10marks
 b) Draw neat functional diagram of PLL IC 565 and explain the following terms along with the working of this PLL: - 10marks
 - i. Free running frequency
 - ii. Capture range
 - iii. Lock range

6. a) Explain OP_AMP as summer and Comparator. 10marks
b) Compare ideal and practical Integrator circuit 10marks
7. Write short notes on any four of the following: 20marks
- i. Schmitt trigger circuit.
 - ii. Successive approximation resistor Analog to Digital Converter.
 - iii. FET characteristics.
 - iv. Wein bridge oscillator.
 - v. Stability factor of biasing circuit.
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