FACULTY OF ENGINEERING
B.E. 2/4 (ECE) I Semester (Main) Examination, December 2010
ELECTRONIC DEVICES

Time : 3 Hours]

[Max. Marks : 75

Note : Answer **all** questions from Part **A**. Answer **any five** questions from Part **B**.

PART – A (25 Marks)

1. What are the applications of diode ?   2

2. Define Avalanche and Zener Break down of PN junction diodes.   3

3. The reverse saturation current of a silion PN junction diode is $10\,\mu$ A. Calculate the diode current for the forward bias voltage of 0.65V at 27°C.   3

4. Define peak inverse voltage. What is the Peak inverse voltage of a Full wave rectifier ?   2

5. A FET has a driven current of 4 mA. If I_{DSS} = 8 mA and $V_{GS(off)}$ = – 6V. Find the value of V_{GS} and V_p.   3

6. What is thermal runaway ? How is prevented in amplifier ?   3

7. Draw h-parameter equivalent circuit of CB configuration.   2

8. When an SRC-FWR is connected across a sinusoidal voltage of 200 sin 314t, the RMS value of the current flowing through the device is 20 A ? Find the power raring of the SCR.   3

9. Draw the V.I. characteristics of TRIAC.   2

10. Give some applications of CRO.   2

PART – B (50 Marks)

11. Determine the resistivity of germanium

   a) In intrinsic condition at 300°K.

   b) With donor impurity of 1 in 10^7

   c) With acceptor impurity of 1 in 10^8

   d) With both the above impurities simultaneously.

   Given that for germanium at room temperature.

   $n_i = 2.5 \times 10^{13}/cm^3$, $\mu_n = 3800$ cm^2/V-S, $\mu_p = 1800$ cm^2/V-S and a number of Germanium atoms/cm$^3 = 4.4 \times 10^{22}$.   **10**

12. a) Draw the Full wave – Rectifier circuit and explain also find I_{rms}, V_{rms}, Ripple factor and efficiency.   **7**

   b) What are the advantages and disadvantages of tunnel diode ?   **3**

13. a) Compare CB, CE and CC configurations in terms of R_i, R_o, A_I, A_V and phase shift.   **5**

   b) Draw and explain the block diagram of CRO.   **5**

14. a) Explain Ebers-moll model.   **4**

   b) Calculate the values of R_1 and R_c in the voltage divides bias circuit so that Q-point is at $V_{CE} = 6$ V and I_c and 2 mA. Assume the transistor parameters are $\alpha = 0.985$, $I_{CBO} = 4 \mu A$ and $V_{BC} = 0.2$ V.   **6**

15. a) Derive the expression for saturation drain current in JFET.   **7**

   b) Define rd, μ and g_m in JFET.   **3**

16. a) Draw basic structure of charge-coupled device and its operation also give the applications.   **6**

   b) Find the stability factor of collector-to-base bias circuit.   **4**

17. Write short notes on :   **10**

   a) Pinch-off voltage

   b) Liquid crystal display

   c) Early-Effect

   d) CMOS circuit.