Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/MCA/SEM-1/MCA-101/2012-13

2012

COMPUTER ORGANISATION AND ARCHITECTURE

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) 'Cycle Stealing' is associated with

      a) Data transfer among registers

      b) DMA

      c) Pipelining

      d) Microprogramming.

   ii) The largest integer that can be represented in signed @'s complement representation using n bits is

      a) $2n - 1$ b) 2^n

      c) 2^{n-1} d) $2^n - 1$.

   iii) Using an additional NOT gate, a JK flip-flop can be converted into

      a) T flip-flop b) RS flip-flop

      c) Master Slave flip-flop d) D flip-flop.

iv) A microprocessor has a data bus with 64 lines and an address bus with 32 lines. The maximum number of bits that can be stored in this memory is

a) 32×2^{32} b) 32×2^{64}

c) 64×2^{32} d) 64×2^{64}.

v) The expression 'delayed load' is used in context of

a) Processor-printer communication

b) Memory-monitor communication

c) Pipelining

d) Computer arithmetic.

vi) Break point is used for

a) Stopping a program at a desired place

b) Manipulating the stack

c) Executing each instruction individually

d) Calling a subroutine.

vii) A truth table of n variables has ..... minterms.

a) n^2 b) $(n-1)^2$

c) 2^n d) 2^{n-1}.

viii) Which of the following shift operations divide a signed binary number by 2 ?

a) Logical left shift b) Logical right shift

c) Arithmetic left shift d) Arithmetic right shift.

ix) Dual of $a + b * c$ is

a) $(a + b) * (a + c)$ b) $a * (b + c)$

c) $a' * (b' + c')$ d) $(a' + b') * (a' + c')$.

x) A memory accessed by content is called

a) Associative memory

b) Content associative memory

c) All of the above

d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Why NAND gate called universal logic gate ? 2

   b) Write the differences of 1's complement and 2's complement representations of the binary number system. 3

3. Convert a JK flip-flop into a *D* flip-flop. 5

4. Verify the de Morgan' theorem by means of truth table. 5

5. Why Grey code is called self-reflective code and Excess-3 code is called self-complementing code ? What are the problems with Grey code ? 5

6. Construct a 5 × 32 decoder with the help of 2 × 4 decoders. 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Write an algebric function for the given function and simplify algebraically $F(X, Y, Z) = \Pi\ (0, 1, 4, 5)$

   b) Simplify algebraically $[\ X'(Y' + Z')\ \ (X + Y + Z')\ ]$.

   c) Design a combinational circuit that can convert a BCD code to it's equivalent Grey code.

   d) Design a block diagram of a 4 – bit adder/subtractor circuit. 3 + 3 + 3 + 6

8. a) Write down the advantage and disadvantage of Karnaugh map ? Why does 11 comes before 10 in Karnaugh map ?

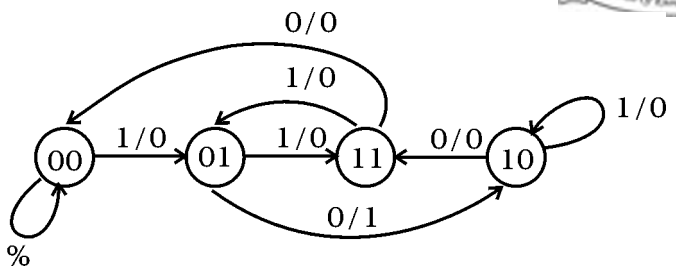
   b) How many input line(s) must be present in a demultiplexer that has 32 possible output lines ?

   c) Why is gated D latched called "transparent" latch ?

   d) Construct a one bit BCD adder using two 4 — bit Binary adder and an additional external circuit.

   (2 + 2) + 1 + 2 + 8

9. a) Design a sequential circuit using JK flip-flop which realizes the following scale diagram :



b) Draw a schematic diagram of JK Master-Slave flip-flop.

c) Find out the value of R if $(125)_R = (203)_5$. 8 + 4 + 3

10. a) Design a 8 : 1 MUX using two 4 : 1 MUX.

b) Design a MOD 10 synchronous counter.

c) Design the circuit using Multiplexer.

11. Write short notes on any *three* of the following : 3 × 5

a) Universal Gate

b) Addressing Mode

c) Cache Memory.

d) Von Neuman Architecture

e) 2's complement subtraction.