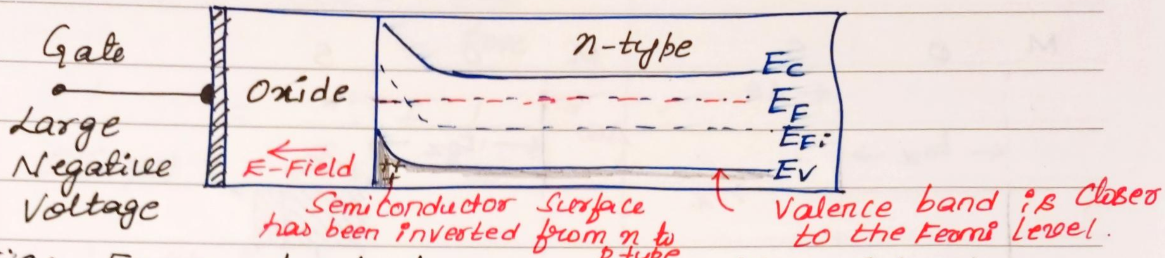


Fig: Energy-band diagram of the MOS Capacitor with an n-type substrate.

→ Conduction and valence bands bends upward.

→ Semiconductor surface adjacent to the oxide semiconductor interface is p-type.

CAPACITANCE - VOLTAGE CHARACTERISTICS

→ The MOS Capacitor structure is the heart of the MOSFET.

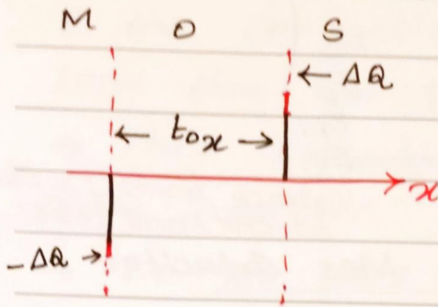
→ It is the small signal capacitance

→ i.e we apply dc potential V & on top of that we apply a change in potential ΔV

→ There is charge in semiconductor because of applied dc voltage i.e Q, & there is increase in charge of ΔQ by the voltage ΔV.

$$C = \frac{\Delta Q}{\Delta V} = \frac{dQ}{dV}$$

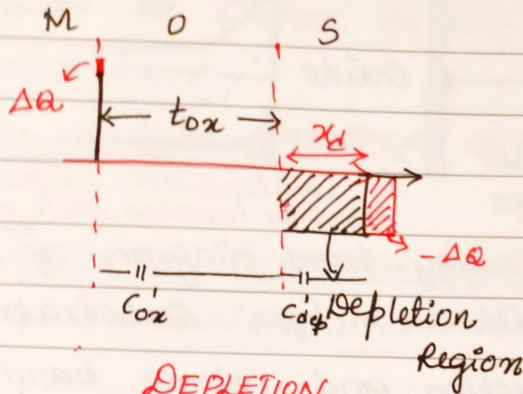
→ Consider charge distributions in Accumulation mode, Depletion mode & Inversion mode



ACCUMULATION

V_G (-ve)

$$C' = \frac{\varepsilon_{ox}}{t_{ox}}$$

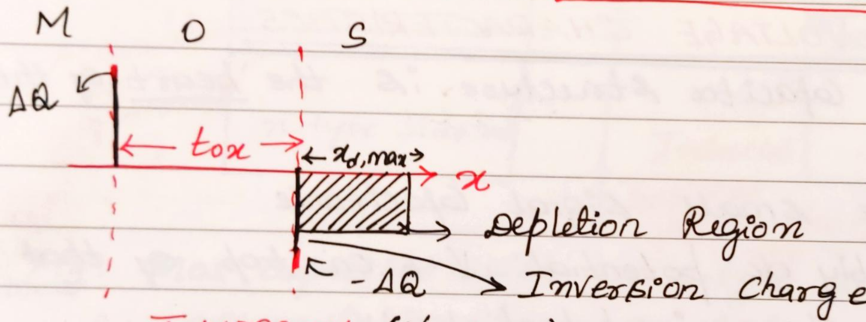


DEPLETION

V_G (+ve Small)

$$\frac{1}{C'} = \frac{1}{C'_{ox}} + \frac{1}{C'_{dep}}$$

$$C'_{dep} = \frac{\varepsilon_{si}}{x_d}$$



INVERSION (V_G (+ve))

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

→ In the depletion region.

$$\frac{1}{C'_{(dep)}} = \frac{1}{C'_{ox}} + \frac{1}{C'_{SD}} \qquad C'_{SD} = \frac{\varepsilon_{si}}{x_d}$$

$$C'_{(Dep)} = \frac{C_{ox} C'_{SD}}{C_{ox} + C'_{SD}} = \frac{C_{ox}}{1 + \frac{C_{ox}}{C'_{SD}}} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right) x_d}$$

∴ As the space charge width increases, the total capacitance $C'_{(dep)}$ ~~inc~~ decreases.

MANJULA.K, Assistant Prof, Dept. of ECE

Summarising all Capacitances.

$$C'(acc) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\frac{1}{C'(depl)} = \frac{1}{C_{ox}} + \frac{1}{C'_{SD}}$$

$$C'(inv) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}.$$

→ For increased V_G, when maximum depletion width is increased. This condition yield to minimum Capacitance C'_{min}

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}}$$

→ Figure below shows ideal Capacitance versus gate voltage or C-V characteristics of the MOS Capacitor

Fig: Ideal low-frequency Capacitance V/s gate voltage of MOS Capacitor.

→ The point on the curve that corresponds to the flat-band condition is of interest.

- Flat band condition occurs between the accumulation & depletion conditions.

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \frac{\epsilon_{ox}}{\epsilon_s}\sqrt{\frac{KT}{q}\left(\frac{\epsilon_s}{qN_a}\right)}}$$

FORMULAE for Capacitance Calculation.

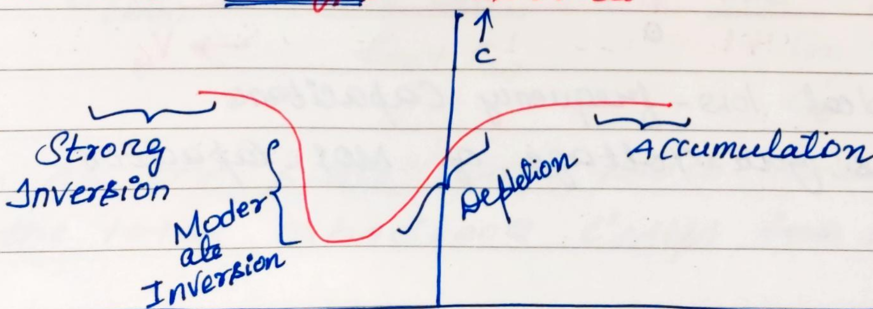
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$x_{dT} = \sqrt{\frac{4\epsilon_s \phi_{fp}}{qN_a}} \qquad \phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right)$$

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}}$$

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\frac{KT}{q}\right)\left(\frac{\epsilon_s}{qN_a}\right)}}$$

→ C-V characteristics for an MOS capacitor with an n-type substrate



Frequency Effects.

→ We must consider the source of electrons that produces a change in the inversion charge density.

→ There are two sources of electrons that can change the charge density of the inversion layer.

1. First source is by diffusion of minority carrier electrons from the p-type substrate across space charge region. this wont be effect by frequency of operation.

2. The second source of electrons is by thermal generation of electron-hole pairs within the space charge region.

→ Both of these processes generate electrons. at a particular rate. i.e electron concentration. in the inversion layer cannot change instantaneously.

→ At high frequency, the inversion layer charge will not respond to a differential change in the capacitor voltage.

i.e The capacitance of the MOS capacitor is then C'_{min}

→ The high frequency & low frequency limits the C-V characteristics

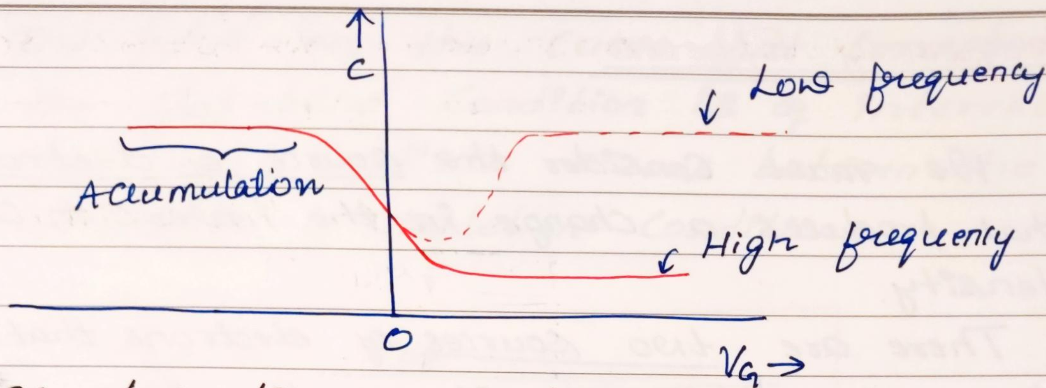
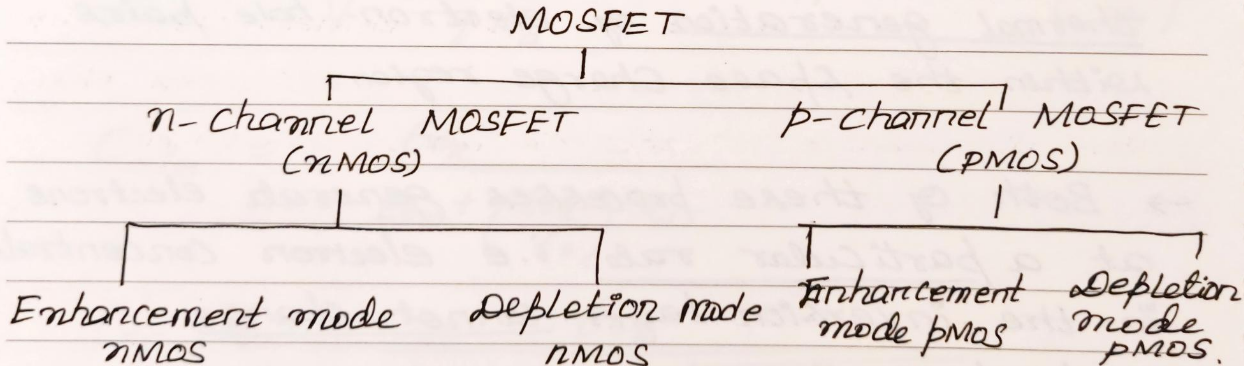


Fig: Low- frequency & high frequency. Capacitance Versus gate. voltage

THE BASIC MOSFET OPERATION

MOSFET Structures

→ MOSFET Classification



→ In Enhancement mode. nMOS Transistor.

- Semiconductor substrate is not inverted directly under the oxide with zero gate voltage i.e No Channel at $V_{gs} = 0$
- A positive gate voltage induces inversion layer (channel) which connects drain & source regions.

→ The source terminal is the source of carriers that flows through channel to the drain terminal.

→ Below fig shows n-channel Enhancement-mode MOSFET

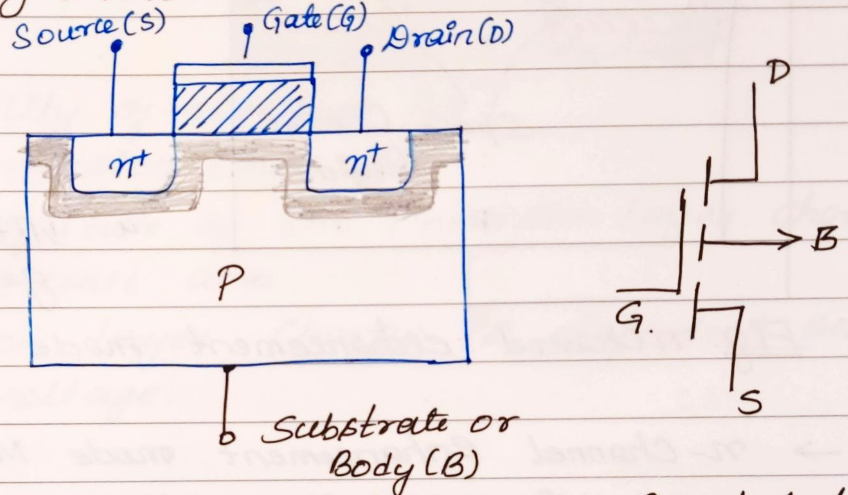


Fig. Cross section & circuit symbol for an n-channel enhancement-mode MOSFET

→ For this n-channel device, electrons flow from the source to the drain, so current will enter from drain to source.

n-channel depletion mode MOSFET.

→ An n-channel exists under the oxide with zero volts applied to the gate.

→ n-channel shown in the figure below is an electron inversion layer or an intentionally doped n-region.

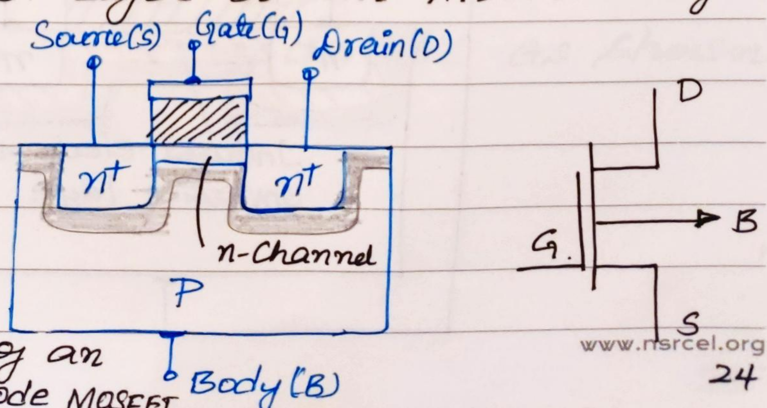
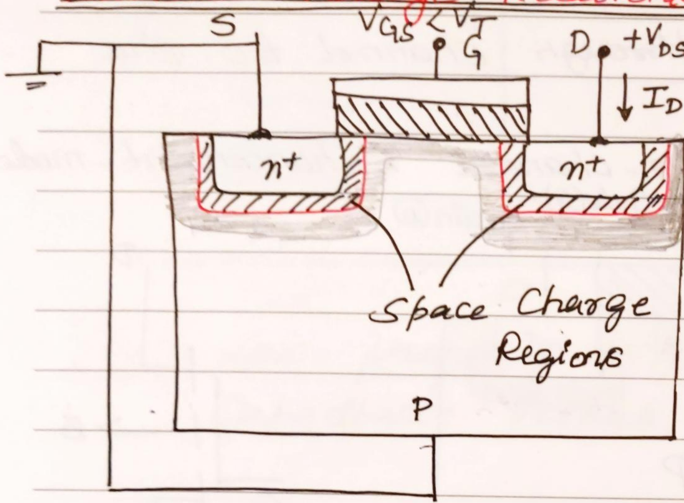


Fig: Cross section & circuit symbol of an n-channel depletion mode MOSFET

Current-Voltage Relationship : Concepts



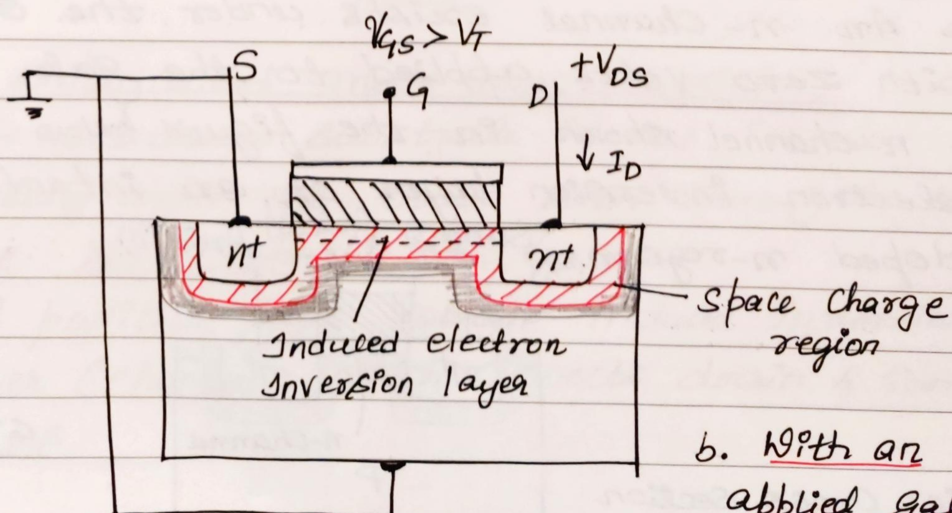
a. With an applied gate Voltage $V_{GS} < V_T$

Fig. n channel enhancement mode MOSFET

→ n-channel enhancement mode MOSFET with a gate-to-source voltage that is less than the threshold voltage & small drain-to-source voltage.

→ Source & body terminals are held at ground potention.

→ With this bias configeration, there is no channel present between source & drain.



b. With an applied gate Voltage $V_{GS} > V_T$

→ For small V_{DS}, the channel region has the resistor characteristics. i.e

$$I_D = g_d V_{DS} \qquad g_d \rightarrow \text{Channel conductance}$$

$$g_d = \frac{W}{L} \mu_n |Q_n'|$$

- μ_n - Mobility of electrons in the inversion layer
- $|Q_n'|$ - Magnitude of the inversion layer charge per unit area.

→ Inversion layer charge is dependent on gate voltage.

→ I-V Characteristics of MOSFET.

- When $V_{GS} < V_T$ the drain current is zero.
- As $V_{GS} > V_T$, the channel inversion charge density increases, which increases channel conductance.
- A larger value of g_d produces a larger initial slope of the I_D versus V_{DS} characteristic as shown in the figure above.

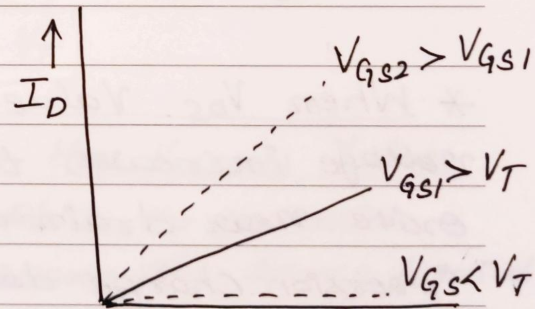


Fig: I_D versus V_{DS} characteristics for small values of V_{DS}.

* Increased V_{DS} voltage.

- For $V_{GS} > V_T$ & small V_{DS} voltage

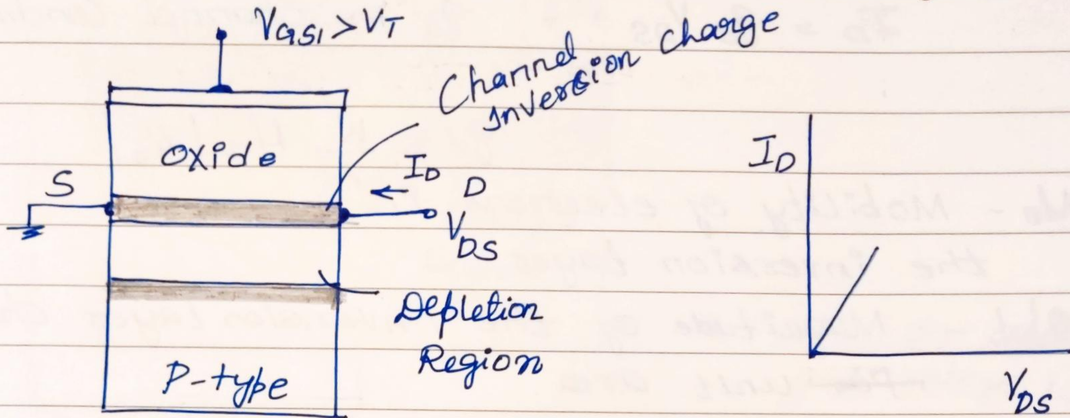


fig: For small V_{DS} value

→ The thickness of the channel indicates the relative charge density. which is constant along the entire channel length. The corresponding I_D vs V_{DS} curve is shown in the figure above.

* When V_{DS} value increases, As the drain voltage increases, the voltage drop across the oxide near drain decreases., i.e the induced inversion charge density also decreases near drain.
- i.e slope of I_D vs V_{DS} curve will decrease.

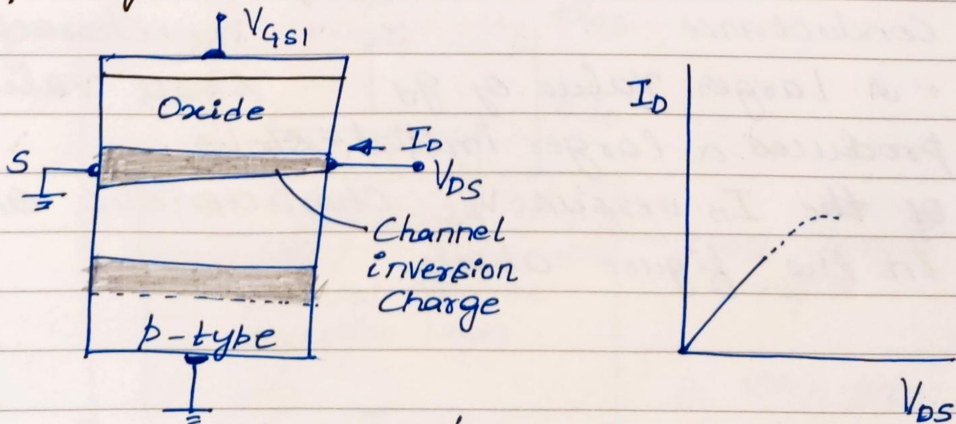


fig: A larger V_{DS} is applied

* When V_{DS} increases to the point where the potential drop across the oxide at the drain terminal is equal to V_T. The induced charge density is zero at the drain terminal.

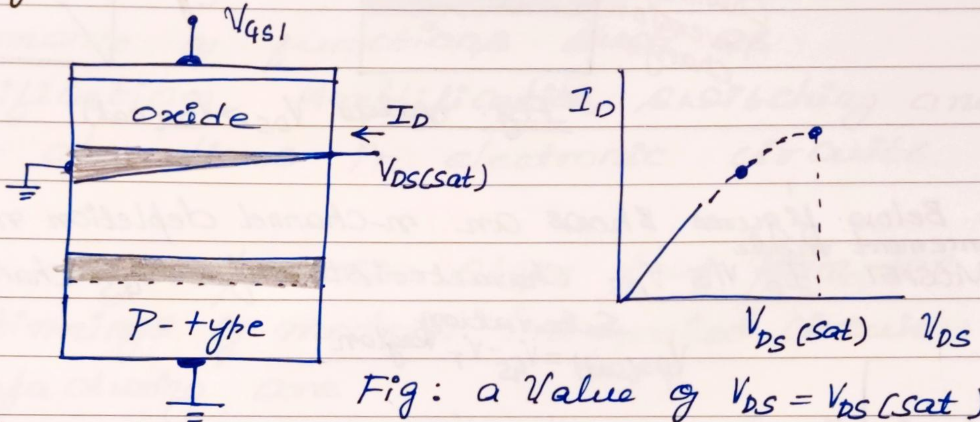


Fig: a Value of $V_{DS} = V_{DS(sat)}$.

- At this point where $V_{DS} = V_{DS(sat)}$, the incremental conductance at the drain is zero.

i.e $V_{GS} - V_{DS(sat)} = V_T$

or

$$\therefore \boxed{V_{DS(sat)} = V_{GS} - V_T}$$

* When V_{DS} becomes larger than the $V_{DS(sat)}$ value, the point in the channel at which the inversion charge is just zero moves towards the source terminal.

– The electrons entered the channel are injected into the space charge region & are swept by E-field to the drain contact. & the current (I_D) will be a constant for $V_{DS} > V_{DS(sat)}$ & this region of operation is called saturation region.

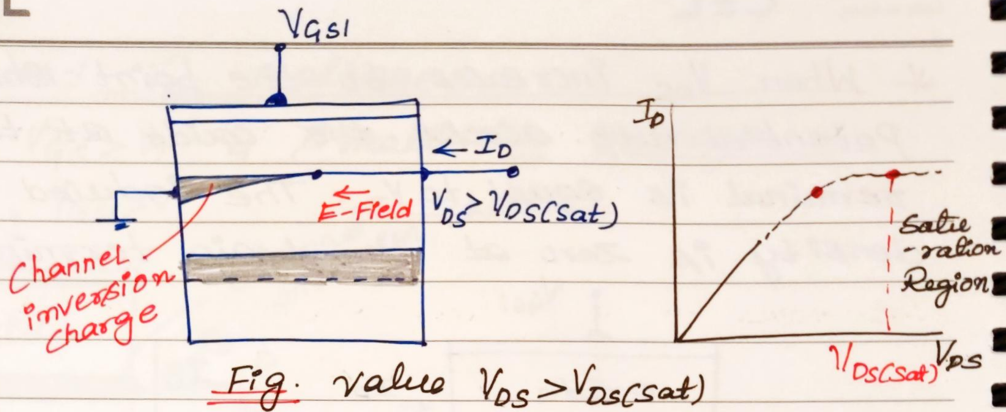


Fig. value $V_{DS} > V_{DS(sat)}$

→ Below figures shows an n-channel depletion mode & Enhancement mode MOSFET I_D V/S V_{DS} Characteristics for V_{GS} changes.

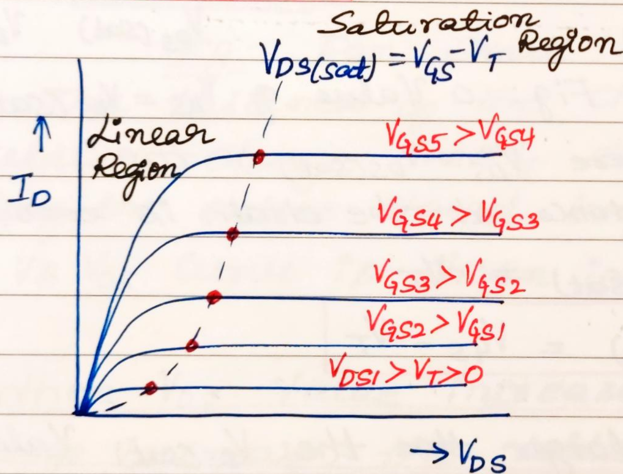


Fig: I_D vs V_{DS} curves for an n-channel enhancement-mode MOSFET

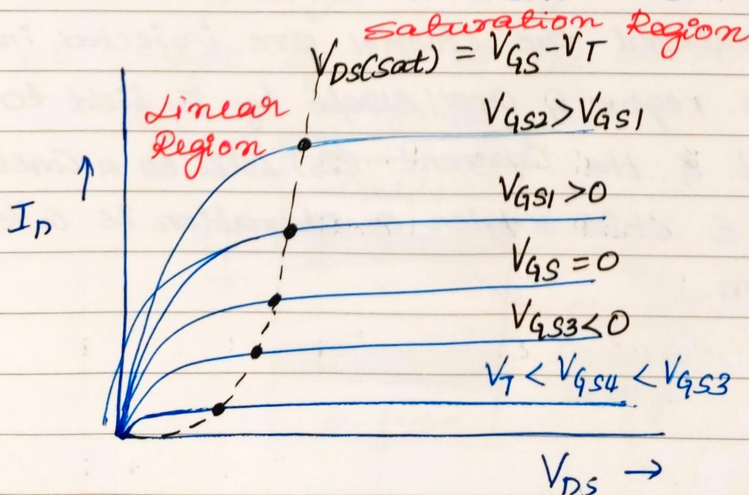


Fig: I_D V/S V_{DS} curves for an n-channel depletion-mode MOSFET