BTS – IV– 04.14 – 0078

C

B.Tech. Degree IV Semester Examination April 2014

EE 1402 DIGITAL ELECTRONICS
(2012 Scheme)

Time : 3 Hours Maximum Marks : 100

PART A
(Answer *ALL* questions)

(8 × 5 = 40)

I. (a) Verify the following expression:

(*i*) $(X \oplus Y) \odot (X + Y) = \overline{X} + \overline{Y}$

(*ii*) $\overline{A\overline{B} + ABC + A(B + A\overline{B})} = 0$

(b) What do you mean by self complimenting codes? Give examples.

(c) Design and implement half subtractor using NAND gate.

(d) Explain the working of monostable multivibrator using logic gates.

(e) Differentiate PLA and PAL.

(f) Explain the working of a 3 bit SISO shift register.

(g) Explain fan in and fan out.

(h) Explain 2 input CMOS NOR gate.

PART B

(4 × 15 = 60)

II. (a) Reduce $f(A,B,C,D) = \text{IIM}(2,8,9,10,11,12,14) + d(3,6,7)$ and implement the minimal expression using universal gates. (10)

(b) Design a 3 bit binary to gray code converter using gates. (5)

OR

III. (a) Convert the following: (10)

(*i*) $(1762.46)_8 = (\quad)_{16}$

(*ii*) $(C64D.39E)_{16} = (\quad)_2$

(*iii*) $(984.143)_{10} = (\quad)_8$

(*iv*) $(11101\,10011.10110) = (\quad)_{16}$

(*v*) $(1376.64)_{10} = (\quad)_2$

(b) Use a multiplexer having three data select input to implement the logic for the function $F = \sum m(0,1,2,3,4,10,11,14,15)$ (5)

IV. (a) Design a full adder circuit using two half adder. (10)

(b) Design and implement a full subtractor using NAND gates (5)

OR

V. (a) Explain look ahead carry adder. (8)

(b) Explain the working of astable multi vibrator using logic gates. (7)

(P.T.O.)

VI.	(a)	Write notes on EPROM and EEPROM.	(5)
	(b)	Explain the working of universal shift register.	(10)
		OR	
VII.	(a)	Realize D flip-flop using JK flip-flop.	(7)
	(b)	Design and set up a Mod 10 synchronous counter using JK flip-flop.	(8)
VIII.	(a)	What is interfacing? Explain how CMOS gate can be interfaced with TTL gate.	(8)
	(b)	Draw and explain the operation of two input TTL NAND gates.	(7)
		OR	
IX.	(a)	Explain ECL, RTL, DTL logic families.	(5)
	(b)	Explain sourcing and sinking current.	(5)
	(c)	Compare CMOS and TTL logic families.	(5)

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