Sem-III (R) – Comp. 7/6/12
Computer organization & Architecture

Con. 4795-12. GN-9323

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) Assume **suitable** data whenever **necessary**.

1. (a) Consider a cache (M 1) and memory (M 2) hierarchy with the following characteristics : **10**
M 1 : 16 K words, 50 ns access time
M 2 : 1 M words, 400 ns access time
Assume 8 words cache blocks and set size of 256 words with set associative mapping.
(i) Show the mapping between M 1 and M 2.
(ii) Calculate the effective access time with a cache hit ratio of h = 0.95
(b) What do you mean by Fetch cycle, instruction cycle, machine cycle and interrupt acknowledgement cycle ? Explain in brief. **10**

2. (a) Multiply (– 7) with (3) by using Booth's multiplication. Give the flow table of multiplication. **10**
(b) What is microoperation ? Give suitable examples of some four types of microoperations. **10**

3. (a) What do you mean by initialization of DMA controller ? How DMA controller works ? Explain with suitable block diagram. **10**
(b) What is virtual memory ? Explain how virtual address is mapped to actual physical address. **10**

4. (a) Explain with an example, how effective address is calculated in different types of addressing modes. **10**
(b) Formulate a four segment instruction pipeline for a computer. Specify the operation to be performed in each segment. **10**

5. (a) Explain any two methods of hardwired control unit. **10**
(b) Explain the von newmann architecture with the help of diagram. **10**

6. (a) With neat flow chart, explain the procedure for division of floating point numbers carried out in a computer. **10**
(b) Explain the Flynn's classification of parallel processing. **10**

7. Write short notes on (any **four**) :– **20**
(a) PCI bus architecture
(b) Systolic arrays
(c) Comparison of RISC and CISC
(d) IEEE 754 format
(e) Programmed I/O.