SE | IT | III | CR) 24|5|13

Digital Logic Design & Application

Con. 6580–13. **GS–6459**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Answer any **four** out of remaining **six** questions.
(3) **All** questions carry **equal** marks.
(4) Assume **suitable** data if **required**.

1. (a) Write the Hamming code for 1100. **5**
   (b) Perform $942_{(10)} - 573_{(10)}$ in BCD using 10's complement. **5**
   (c) Convert T flipflop into D flipflop. **5**
   (d) Implement following function using 8 : 1 MUX **5**
   $F(A, B, C, D) = \sum m(0, 2, 6, 10, 12, 14)$

2. (a) Design and implement BCD to ex-3 code converter. **10**
   (b) Design 2 bit up/down asynchronous counter. **10**

3. (a) Write short note on PAL and PLA. **8**
   (b) Given the logic expression **12**
   $$AB + A\overline{C} + C + AD + A\overline{B}C + ABC$$
   (i) Express in std SOP form
   (ii) Minimize using k-map and realize using only NOR gates.

4. (a) Design 3 bit comparator. **10**
   (b) Minimize using Quine Mc Clusky method **10**
   $F(A, B, C, D) = \sum(0, 1, 3, 5, 7, 9, 11, 14) + d(2, 14)$

5. (a) Design full subtractor using 2 half subtractor. **10**
   (b) Design 2 bit look ahead carry generator. **10**

6. (a) Design a synchronous counter for the following sequence using T F/F **12**
   6–3–5–2–0–4–1–7
   (b) Prove that NAND and NOR are Universal Gates. **8**

7. Write short notes on any **two** :— **20**
   (a) Priority encoder
   (b) VHDL Programming feature
   (c) CAD Tools.
