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(XXXIV cycle)

Analysis, Design and Control of a Modular Full-Si Converter Concept for Electric Vehicle Ultra-Fast Charging

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

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Abstract

The transportation sector is one of the major contributors to the global greenhouse gas generation and is thus subject to considerable political attention. In view of the increasing concerns on the long-term effects of CO_2 emissions in the atmosphere and the worsening air quality in most urban areas, a worldwide shift towards vehicle electrification is currently underway. Government policies are pushing for the phase-out of internal combustion engine vehicles (ICEVs), i.e. no longer able to satisfy the increasingly strict emission requirements, meanwhile supporting the adoption of electric vehicles (EVs).

Even though EVs provide several advantages with respect to ICEVs, such as better performance, no local pollution, reduced maintenance and cost of ownership, limited noise emissions and the option of charging at home and/or at work, there are still significant challenges that impair their widespread adoption. In particular, potential EV customers are typically discouraged by the higher price with respect to comparable ICEVs and fear "range anxiety", due to the limited range (i.e., typically 200 – 500 km), the long charging times (i.e., usually exceeding 30 min for a full charge) and the general lack of charging stations. To ensure a broader EV adoption, the key technical challenges to be overcome are related to improving current battery technology (i.e., in terms of cost, energy density, charge rate, lifetime degradation, etc.), enhancing the performance of EV powertrain components (i.e., in terms of efficiency, size, weight, etc.) and scaling up dramatically the charging infrastructure (i.e., in terms of charging power, number of stations, number of stalls, etc.).

In this context, this thesis deals with the converter-level challenges related to the development of high-power EV battery chargers, which represent a key enabler to mainstream EV adoption as they address one of the major customer concerns, i.e. the charging time. In particular, the focus is on ultra-fast battery charging technology, which aims to achieve a stop-and-go EV refueling experience similar to the one of an ICEV, targeting ≈ 200 km of added range in 5 min. The main goal of this dissertation is to analyze, design, control and assess experimentally a modular converter concept for EV ultra-fast charging, addressing the challenging requirements set by the application. The performed research activity has resulted in several contributions, mainly related to the converter analysis and modeling, the converter design and the converter control.

Abbreviations

1D	One-Dimensional
2D	Two-Dimensional
2LSVPWM	Two-Level Space Vector PWM
3LDPWMA	Three-Level Discontinuous PWM A
3LDPWMB	Three-Level Discontinuous PWM B
3LSVPWM	Three-Level Space Vector PWM
BCM	Boundary Conduction Mode
BMS	Battery Management System
CC	Constant-Current
CCM	Continuous Conduction Mode
CV	Constant-Voltage
DAB	Dual Active Bridge
DAC	Digital-to-Analog Converter
DCM	Discontinuous Conduction Mode
DPF	Displacement Power Factor
DPS	Double Phase-Shift
DSO	Distribution System Operator
DSP	Digital Signal Processor
EDF	Extended Describing Function
EMI	ElectroMagnetic Interference
EV	Electric Vehicle
FHA	First Harmonic Approximation
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor

ICEV	Internal Combustion Engine Vehicle
ISR	Interrupt Service Routine
MAF	Moving Average Filter
MCU	MicroController Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PI	Proportional-Integral
PLL	Phase-Locked Loop
PSFB	Phase-Shift Full Bridge
PWM	Pulse-Width Modulation
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SPS	Single Phase-Shift
SPWM	Sinusoidal PWM
TDA	Time Domain Analysis
THD	Total Harmonic Distortion
THIPWM	Third Harmonic Injection PWM
TIM	Thermal Interface Material
TPS	Triple Phase-Shift
VCO	Voltage-Controlled Oscillator
WBG	Wide BandGap
ZCS	Zero Current Switching
ZMPCPWM	Zero Mid-Point Current PWM
ZOH	Zero-Order Hold
ZVS	Zero Voltage Switching

Contents

Chapter 1

Introduction

As a result of increasing concerns on the long-term effects of CO_2 emissions in the atmosphere caused by the combustion of fossil fuels, a worldwide shift towards renewable energy generation and domestic/industrial electrification is currently underway.

The transportation sector accounts for $\approx 23\,\%$ of the global CO_2 emissions (as of 2021 [1]) and is therefore subject to considerable political attention. Because of government regulations aiming to limit greenhouse gas emissions, internal combustion engine vehicles (ICEVs) are being phased out, as they are no longer able to satisfy the increasingly strict emission requirements. At the same time, the adoption of electric vehicles (EVs) is increasing rapidly [2], in view of their better performance, absence of local pollution, government incentives (when present), reduced maintenance and cost of ownership, limited noise emissions and the option of charging at home and/or at work. Although EV sales already accounted for $\approx 10\,\%$ of the global car market in 2021 [2] (i.e., including battery EVs and plug-in hybrid EVs), they still represent only $\approx 1.5\,\%$ of the global car stock and several challenges have yet to be overcome. In particular, potential EV customers are typically discouraged by the higher price with respect to comparable ICEVs and fear "range anxiety", due to the limited range (i.e., typically $200-500\,\mathrm{km}$), the long charging times (i.e., usually exceeding $30\,\mathrm{min}$ for a full charge) and the general lack of charging stations.

From a technical standpoint, the key challenges for a broader EV adoption are related to improving current battery technology (i.e., in terms of cost, energy density, charge rate, lifetime degradation, etc.), enhancing the performance of EV powertrain components (i.e., in terms of efficiency, size, weight, etc.) and scaling up dramatically the charging infrastructure (i.e., in terms of charging power, number of stations, number of stalls, etc.). In this context, this work deals with the technical challenges related to the development of high-power EV battery chargers, which allow to tackle one of the major obstacles to EV adoption, i.e. the charging time.

1.1 Electric Vehicle Ultra-Fast Charging

Off-board DC fast chargers are a key enabling technology for the widespread adoption of EVs, since they allow to dramatically decrease the EV charging time with respect to built-in on-board AC chargers (cf. **Fig. 1.1**) [3, 4]. Furthermore, a widespread DC charging infrastructure would address the customer fear for range anxiety and simultaneously enable the advent of EVs with smaller battery packs and thus lower cost, addressing a much larger part of the market.

Ultra-fast charging (or extreme fast charging) refers to the ability of achieving a stop-and-go EV refueling experience similar to the one of an ICEV [5], targeting $\approx 200\,\text{km}$ of added range in 5 min. Considering that the typical passenger vehicle energy consumption ranges between $150 - 250\,\text{Wh/km}$ [6], this target translates in a required charging power of $\approx 300 - 500\,\text{kW}$. The high power to be processed, together with several other requirements, poses several technical challenges in the realization of an ultra-fast battery charger. In this section, the key requirements of ultra-fast battery chargers are described and the main challenges related to their design and operation are discussed. Moreover, an overview of the state-of-the-art of ultra-fast chargers is provided.

1.1.1 Requirements and Challenges

The main requirements of an EV ultra-fast battery charger can be summarized in:

- high conversion efficiency, to maximize the energy transferred to the vehicle and minimize the heat dissipation;
- high power density, to minimize the volume and thus the footprint of the system;
- high reliability, to maximize the mean time between failures and therefore maximize the charging station availability;

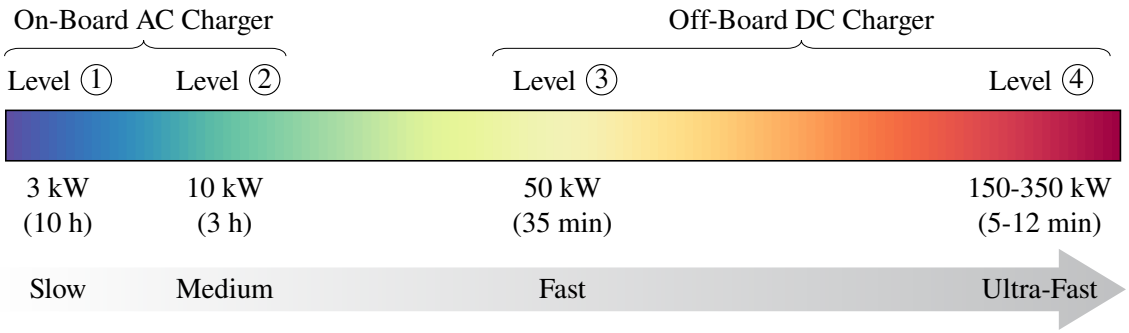


Fig. 1.1: Simplified overview of the existing charging levels [7, 8], the related charging power and the estimated time to charge 30 kWh (i.e., 200 km of range at $150\,\text{Wh/km}$).

- cost effectiveness, as the initial investment cost is charged to the final user and must ensure a competitive price per kWh;
- galvanic isolation between the main distribution grid and the vehicle battery according to safety standards [9];
- wide output voltage range, to provide a universal supply capable of charging all commercially available EVs;
- sinusoidal grid-side currents with low distortion and harmonics according to grid-code standards [10, 11];
- low battery-side current ripple, to limit the premature aging of the battery itself.

The simultaneous achievement of all aforementioned requirements poses significant technical challenges.

In particular, achieving at the same time high efficiency, high power density, high reliability, cost effectiveness, galvanic isolation and wide output voltage range leads to an extremely challenging converter design. For instance, the high amount of transferred power together with the limited converter volume require an adequate heat dissipation system (e.g., a 95 % efficiency at 300 kW translates in 15 kW of heat to be dissipated).

Furthermore, ensuring clean sinusoidal grid currents and low battery charging current ripple lead to a challenging converter control, which may be addressed with advanced control strategies implemented by digital means.

Another significant challenge is related to the impact of ultra-fast battery chargers on the distribution grid [12–14]. In fact, conventional DC fast charging stations represent a high-power, unpredictable and discontinuous load for the electrical system. The large scale diffusion of this kind of stations is increasing the utility daily peak load, directly causing transformer overload and accelerated aging, meanwhile increasing system power losses [12]. Moreover, their lack of flexibility leads to high peak power charges for the station operator, which are then reflected on the charging price for the final users, and poses serious challenges to the power distribution system, affecting its stability and decreasing the power quality [15]. Most of the issues mentioned above can be addressed either by directly connecting the charger to the medium-voltage grid [16–19] or by having local energy storage at disposal, e.g. leveraging the EV batteries (i.e., known as vehicle-to-grid operation) or installing separate storage to the station [20–22]. In particular, a correct sizing of the storage unit provides great flexibility to the charging station, allowing to reduce its peak power demand and the size of the protection equipment, thus leading to both lower operational costs and initial investment [22, 23]. Moreover, the availability

of stored energy opens up the possibility of providing grid ancillary services, such as active power injection/absorption for grid frequency regulation, reactive power support for voltage regulation, grid harmonic reduction and fault current generation during voltage dips/swells [13]. These features can directly support the power distribution system, effectively turning around the drawbacks of conventional ultra-fast charging stations, meanwhile allowing for an additional revenue stream for the station operator [24].

It is worth noting that this work only focuses on the converter-level challenges of low-voltage ultra-fast chargers, therefore medium-voltage converter architectures and the integration of fast-charging stations into the grid are not discussed here.

1.1.2 State-of-the-Art

DC fast chargers directly deliver DC current to the vehicle battery pack, meanwhile ensuring galvanic isolation from the mains (i.e., for safety reasons in case of fault). As of today, most commercially available DC fast chargers are rated between 50 kW and 150 kW [5], nevertheless a new generation of ultra-fast chargers rated at 350 kW and above is starting to be deployed [16, 17, 39–41]. The technical specifications of several state-of-the-art ultra-fast chargers currently available on the market are summarized in **Table 1.1**. These

Tab. 1.1: Technical specifications of several commercially available ultra-fast chargers.

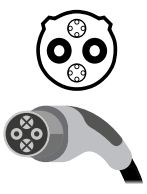
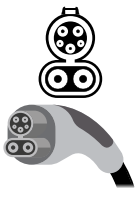
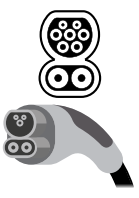
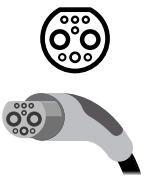
Manufacturer and Model	Nominal Power	Input Voltage	Output Voltage	Output Current	Nominal Efficiency
Blink RT 175-S [25]	175 kW	480 V_{RMS}	200 – 920 V	350 A	> 94.5 %
BTC Power HPCT-200 [26]	200 kW	480 V_{RMS}	50 – 950 V	500 A	> 92 %
Delta UFC 200 [27]	200 kW	400 V_{RMS}	200 – 1000 V	500 A	–
Tesla Supercharger V3 [28]	250 kW	480 V_{RMS}	50 – 500 V	631 A	–
Alpitronic HYC 300 [29]	300 kW	400 V_{RMS}	150 – 1000 V	500 A	> 94 %
Siemens SICHARGE D [30]	300 kW	400 V_{RMS}	150 – 1000 V	500 A	> 95.5 %
ABB Terra HP350 [31]	350 kW	400 V_{RMS}	150 – 920 V	500 A	> 94 %
ENERCON E-Charger 600 [32]	350 kW	400 V_{RMS}	200 – 920 V	500 A	> 94 %
EVBox Ultroniq [33]	350 kW	480 V_{RMS}	50 – 950 V	500 A	–
SIGNET DP350K [34]	350 kW	480 V_{RMS}	150 – 920 V	500 A	–
PHIHONG DO 360 [35]	360 kW	480 V_{RMS}	150 – 950 V	500 A	> 94 %
EVTEC ristretto&charge [36]	384 kW	400 V_{RMS}	150 – 920 V	500 A	> 94.5 %
ChargePoint Express Plus [37]	400 kW	400 V_{RMS}	200 – 1000 V	500 A	> 95 %
Ingeteam RAPID ST [38]	400 kW	400 V_{RMS}	50 – 1000 V	500 A	–

chargers are all designed to be connected to the low-voltage grid and typically consist of several paralleled units with a reduced power rating (i.e., 10 – 30 kW). Notably, the modularity allows to benefit from economies-of-scale, ensures an upgradable system, enables the disconnection of some units at light load to preserve efficiency and allows to reconfigure the connections between units to achieve a wider output voltage/load range.

All commercially available ultra-fast chargers support one or more of the five existing DC fast-charging standards reported in **Table 1.2**, namely CHAdeMO (global), CCS Type 1 (US), CCS Type 2 (EU), GB/T (China), and the Tesla proprietary supercharger system (global). It is worth noting that the ultimate limit to the charging power is set by the voltage/current capability of the connector (and cable). For this reason, liquid cooled cables and connectors are typically adopted when the charging current exceeds 350 A. Although the standards differ on several technical aspects (e.g., the connector, the communication protocol, etc.), the charging process follows similar steps, starting with a signal handshake, the isolation verification and the exchange of fundamental information, such as the vehicle charging limits. Once these steps are completed, the vehicle DC relay is closed and the charging session begins. During the charging process, the vehicle battery management system (BMS) communicates to the charger the desired current and/or voltage reference. Finally, once the desired state-of-charge is met, the vehicle disconnects itself by opening its DC relay.

As mentioned earlier, all state-of-the-art EV ultra-fast chargers are designed to be connected to the three-phase low-voltage grid, mainly to leverage the existing industrial power electronics knowledge and availability [4, 5, 17, 42]. According to safety standards [9], the charging station must ensure the galvanic isolation (i.e., with isolation monitoring) between the main distribution network and the vehicle battery, such that the

Tab. 1.2: Overview of the five DC fast-charging standards (adapted from [39]).

	CHAdeMO	**CCS Type 1**	**CCS Type 2**	**GB/T**	**Tesla**
					
Maximum Voltage	1000 V	1000 V	1000 V	950 V	–
Maximum Current	400 A	500 A	500 A	400 A	–
Maximum Power*	400 kW	500 kW	500 kW	380 kW	–

*based on maximum voltage and current ratings.

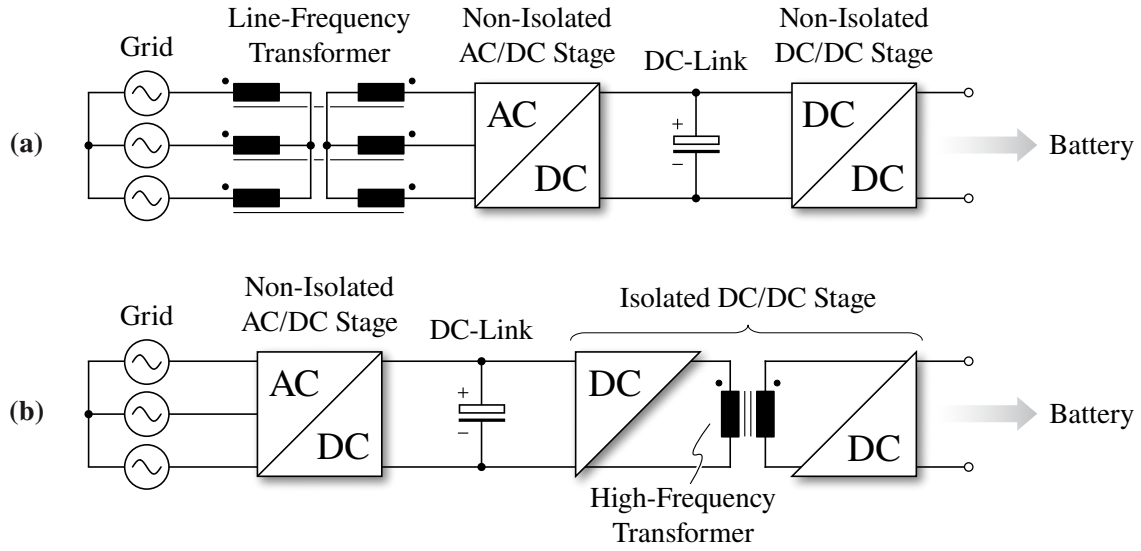


Fig. 1.2: Equivalent circuit schematic of the two most adopted ultra-fast charger architectures, addressing the galvanic isolation requirement **(a)** with a line-frequency transformer connected to the grid and **(b)** with a high-frequency transformer located within the DC/DC stage.

system acts as an unearthed IT power supply system, allowing the driver to safely touch the car in the presence of one isolation fault. This requirement can be approached in two different ways, which lead to two different charger architectures [5]. The first architecture is shown in **Fig. 1.2(a)** and provides the galvanic isolation by means of a conventional line-frequency transformer connected to the grid, followed by a rectifier (i.e., AC/DC) stage and a non-isolated DC/DC stage to address the wide output voltage range. The second architecture, reported in **Fig. 1.2(b)**, features an AC/DC stage directly connected to the grid and implements the galvanic isolation within the DC/DC converter stage by means of a high-frequency transformer, allowing to significantly reduce the overall system volume. For this reason, the second architecture is the most adopted in practice and is the one considered herein.

1.2 Goals and Research Contributions

The main goal of this dissertation is to analyze, design, control and assess experimentally a modular converter concept for EV ultra-fast charging, addressing all requirements and challenges reported in **Section 1.1.1**. In particular, in view of the strict requirements in terms of reliability and cost-effectiveness, only silicon (Si) semiconductor devices are considered, aiming to quantify the performance achievable by a full-Si ultra-fast charger implementation with state-of-the-art Si technology.

The research contributions of this thesis can be organized under three main categories, as illustrated in **Fig. 1.3**:

- *Converter analysis and modeling*. The stresses on all active and passive components (i.e., semiconductors, capacitors, inductors, transformers) are analyzed in detail and several approximate analytical expressions, useful for the converter design and assessment, are obtained for the first time. Furthermore, approximate small-signal models of both the AC/DC and the DC/DC converter stages are derived, providing straightforward tools for the design and tuning of the closed-loop controllers. In particular, a novel simplified dual first-order small-signal model for LLC resonant converter is proposed.

- *Converter design*. A complete step-by-step design procedure of both converter stages is provided, including the selection of the semiconductor devices, the sizing of the capacitors, the multi-objective optimization of the magnetic components and the sizing of the heat dissipation system. In particular, a novel iterative design procedure for LLC resonant converters is proposed, aimed at identifying the optimal parameter values that minimize the converter conduction losses.

- *Converter control*. High-performance digital multi-loop control strategies are proposed for both the AC/DC and the DC/DC converter stages, aiming to maximize the control dynamics and disturbance rejection capabilities. Furthermore, the derived small-signal models are exploited to provide straightforward design/tuning procedures for all control loops.

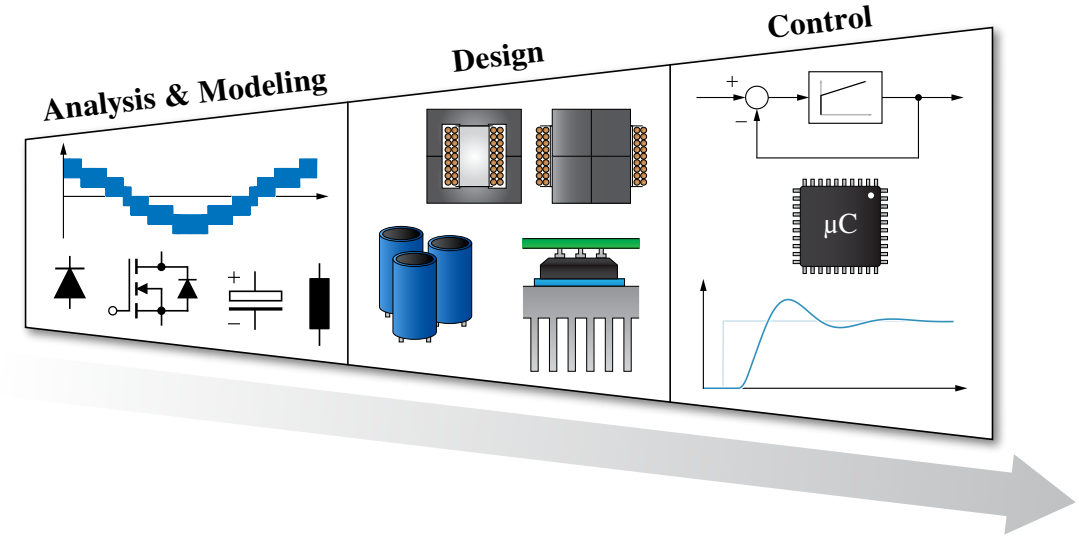


Fig. 1.3: Overview of the three main subjects of this dissertation: converter analysis and modeling, converter design, converter control. All research contributions belong to one of these categories.

1.3 Specifications and Architecture

The considered ultra-fast charger architecture consists of two converter stages, as shown in **Fig. 1.4** (cf. **Fig. 1.2(b)**). The first stage is a three-phase grid-connected AC/DC converter with unity power factor correction capabilities. The role of this stage is to absorb the total amount of charging power from the grid, meanwhile ensuring sinusoidal input currents (i.e., with low distortion and harmonics). The second stage is a high-frequency DC/DC converter, which provides the galvanic isolation from the main distribution grid and regulates the charging process by controlling the output current.

In view of the high target nominal power of ultra-fast chargers (cf. **Section 2.1.1**), the full power is typically addressed with a modular approach, i.e. paralleling multiple converter units rated at a fraction of the total power. The modularity provides several advantages [43], as it allows to benefit from economies-of-scale, increases the total converter reliability, improves the thermal management, ensures an upgradable system and enables the disconnection of some units at light load to preserve efficiency. On the other hand, the use of multiple paralleled units increases the overall system complexity, particularly at the control level. For instance, the DC/DC units cannot be controlled independently when operating in constant-voltage (CV) charging, as only one unit must control the output voltage (i.e., behaving as a voltage source) and send the output current references to the others (i.e., behaving as current sources) [44, 45]. Nonetheless, this issue can be addressed by adopting a master/slave control hierarchy.

Besides having to employ only Si semiconductor devices (i.e., due to their high maturity, reliability and cost-effectiveness), the considered converter module must comply with the target specifications and operating conditions summarized in **Table 1.3**. In particular, considering the relatively high power rating (i.e., 60 kW) and the wide output voltage range (i.e., 250–1000 V), and leveraging the split DC-link provided by the three-level AC/DC stage (cf. **Chapter 2**), the DC/DC converter stage is split into 4x15 kW units with reconfigurable series/parallel outputs, as schematically represented in **Fig. 1.5(a)**. This architecture is already adopted in industry [32] and allows to reduce by a factor of two the output voltage range to be addressed by the single unit (i.e., from 250 – 1000 V to

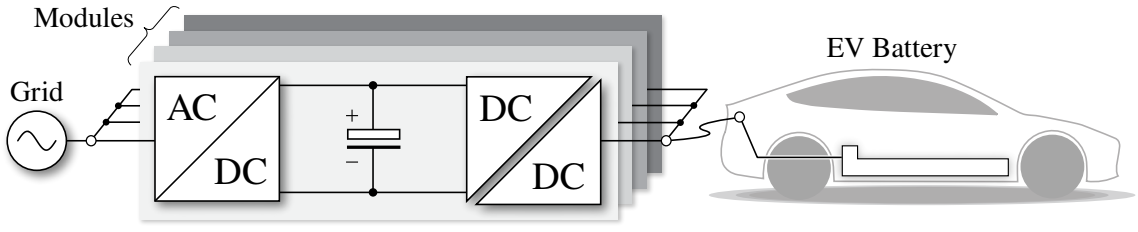


Fig. 1.4: Typical EV ultra-fast charger architecture, consisting of several converter modules in parallel.

Tab. 1.3: Specifications and operating conditions of the considered ultra-fast charger module.

Nominal Power	Input Frequency	Input Voltage	Input Current	Output Voltage	Output Current	Nominal Efficiency
60 kW	50 Hz	400 V_{RMS}	86.5 A_{RMS}	250 – 1000 V	150 A	> 95.5 %

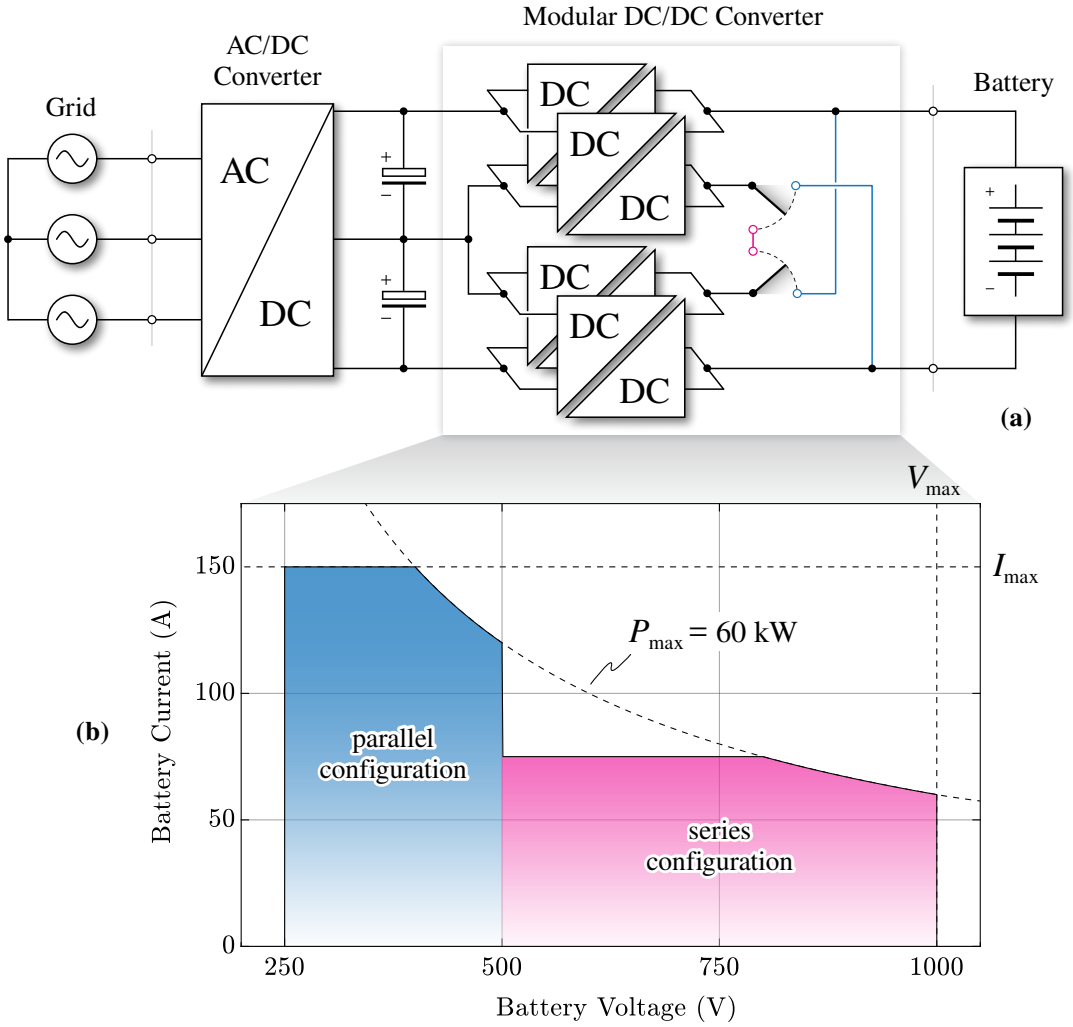


Fig. 1.5: **(a)** equivalent circuit schematic of the architecture of the considered 60 kW DC fast charger module and **(b)** highlight of the output voltage/current feasible operating region assuming reconfigurable (i.e., series/parallel) DC/DC converter outputs.

250 – 500 V), significantly improving the achievable converter performance. Furthermore, the power split allows to simplify the realization of the magnetic components, to employ discrete semiconductor devices without the need of hard-paralleling and to turn-off one or more modules at light load operation, ensuring higher efficiency over the complete charging range (cf. **Chapter 6**). The feasible operating region of the 60 kW converter module is shown in **Fig. 1.5(b)**, where the maximum converter output current I_{max}, voltage

V_{max} and power P_{max} limits are indicated. The two output voltage intervals corresponding to the two different DC/DC converter configurations are highlighted.

It is worth noting that a nominal efficiency $> 95.5\,\%$ is targeted, aiming to outperform all commercially available EV ultra-fast chargers (cf. **Table 1.1**). Since the considered converter module consists of two stages, an efficiency target of $98.5\,\%$ is set for the AC/DC stage and, consequently, a minimum efficiency target of $97\,\%$ is obtained for the DC/DC stage.

1.4 Outline of the Thesis

This thesis consists of two parts (with three chapters each) and a conclusive chapter. The content of each chapter is summarized here.

PART I: AC/DC Converter

- **Chapter 2: Analysis**
  The requirements of the AC/DC stage are introduced and an overview of the existing three-phase pulse-width modulated (PWM) converter topologies for general active rectification is provided, leading to the selection of a unidirectional three-level T-type structure. Therefore, the operational basics of three-level rectifiers are described, including a detailed analysis of the converter operating limits. Moreover, the converter modulation process is explained and seven different modulation strategies are introduced. Finally, the stresses on the converter active and passive components (i.e., semiconductor losses, DC-link RMS current and charge ripple, AC-side inductor RMS and peak-to-peak flux ripple) are estimated analytically and/or numerically for all modulation strategies, providing straightforward tools for the converter design and preliminary assessment.

- **Chapter 3: Design**
  The complete design methodology of the considered 60 kW three-level unidirectional T-type rectifier is outlined. In view of the high target nominal power, a dual three-phase converter structure is adopted, halving the current rating of each bridge-leg and thus allowing for the adoption of discrete Si semiconductor devices. Therefore, the step-by-step converter design procedure is described, including the selection, sizing and/or optimization of all main converter active and passive components, i.e. the semiconductor devices, the DC-link capacitors, the AC-side inductors and the heat dissipation system (i.e., heatsink and fans). Finally, a converter prototype is built and its performance in terms of loss and efficiency is assessed experimentally.

- **Chapter 4: Control**
  This chapter focuses on the design, tuning and experimental assessment of a high-performance digital multi-loop control strategy for the considered three-level uni-directional T-type rectifier, aiming at minimum phase current distortion under all operating conditions (e.g., non-unity power factor, unbalanced split DC-link loading), fast response dynamics and strong disturbance rejection. To accurately design the four control loops (i.e., dq-currents, DC-link voltage, DC-link mid-point voltage deviation), the system state-space equations are described and the small-signal model of the three-level rectifier is derived. The controllers are then tuned leveraging analytical expressions, taking into account the delays and the discretization introduced by the digital control implementation. Finally, the steady-state and dynamical performance of the proposed multi-loop control strategy is verified in circuit simulation and experimentally on the T-type rectifier prototype, adopting a general purpose microcontroller unit (MCU) for the digital control implementation.

PART II: DC/DC Converter

- **Chapter 5: Analysis**
  An overview of the most adopted topologies for EV battery charging is provided and a resonant LLC converter is selected for the present 4x15 kW application, due to its unmatched efficiency and wide output load/voltage regulation capability. The operating principle of the LLC converter is described, leveraging the first harmonic approximation (FHA) method to identify the converter operating limits in terms of switching frequency, input/output voltage gain and output load. Furthermore, the three typical modes of operation of the LLC converter (i.e., boost-mode, unity-gain-mode, buck-mode) are described in detail and the soft-switching mechanisms of the primary-side transistors and secondary-side diodes are explained. Finally, the stresses on the converter active and passive components (i.e., semiconductor devices, resonant capacitor, resonant inductor, transformer, input/output filter capacitors) are assessed both analytically with FHA and numerically with the more accurate time-domain analysis (TDA), providing straightforward tools for the converter design and/or assessment.

- **Chapter 6: Design**
  A novel iterative design procedure for resonant LLC converters is proposed and applied to the considered modular 4x15 kW application, aiming to minimize the total converter conduction losses. In view of the high target nominal power, an unconventional LLC circuit structure is adopted to split the current/voltage ratings of the magnetic components (i.e., resonant inductors, transformers) and the current rating of the output rectifier diodes (i.e., allowing for the adoption of discrete Si

semiconductor devices). Once the main converter parameters are determined by the proposed design procedure, the selection, sizing and/or optimization of all main converter active and passive components is carried out, including the semiconductor devices, the resonant capacitor, the resonant inductors, the isolation transformers, the input/output filter capacitors and the heat dissipation system (i.e., heatsink and fans). Finally, a 15 kW LLC converter prototype is built and its performance in terms of loss and efficiency is assessed experimentally.

- **Chapter 7: Control**
  This chapter focuses on the design, tuning and experimental assessment of a high-performance digital multi-loop control strategy for the considered LLC resonant converter, aiming at constant closed-loop bandwidth, fast response dynamics and strong disturbance rejection across the complete converter operating region. The control scheme consists of two cascaded voltage and current loops. To design and tune these controllers, a novel simplified LLC dual first order small-signal model is proposed. The system non-linear behavior affecting the current control loop is counteracted by a real-time controller gain adaptation process, which ensures constant control bandwidth. In particular, the adaptive gain values are provided by a static switching frequency look-up table (LUT) obtained experimentally. Moreover, the steady state switching frequency value is fed forward at the output of the current loop regulator, providing a further dynamical performance enhancement. Finally, the steady-state and dynamical performance of the current control loop are verified both in circuit simulation and experimentally on the LLC converter prototype, adopting a general purpose MCU for the digital control implementation.

Conclusion and Outlook

- **Chapter 8**
  The content of this thesis is summarized in this chapter, highlighting the most significant findings and research contributions. Furthermore, an outlook on potential improvements and future developments is provided.

1.5 List of Publications

The publications developed during this Ph.D. (i.e., 10 journal articles, 16 conference papers, 3 patent applications) have been the result of different projects and activities, either related or unrelated to the thesis core topic. In the following, the publications are reported in reverse chronological order.

Journal Articles

Related to the thesis core topic:

- **D. Cittanti**, M. Gregorio, E. Vico, F. Mandrile, E. Armando, and R. Bojoi, "High Performance Digital Multi-Loop Control of LLC Resonant Converters for EV Fast Charging with LUT-Based Feedforward and Adaptive Gain", *Transactions on Industry Applications (Early Access)*, May 2022, DOI: 10.1109/TIA.2022.3178394.
- **D. Cittanti**, M. Gregorio, E. Bossotto, F. Mandrile, and R. Bojoi, "Three-Level Unidirectional Rectifiers under Non-Unity Power Factor Operation and Unbalanced Split DC-Link Loading: Analytical and Experimental Assessment", *Energies*, vol. 14, no. 17, p. 5280, Aug. 2021, DOI: 10.3390/EN14175280.
- **D. Cittanti**, M. Gregorio, E. Bossotto, F. Mandrile, and R. Bojoi, "Full Digital Control and Multi-Loop Tuning of a Three-Level T-Type Rectifier for Electric Vehicle Ultra-Fast Battery Chargers", *Electronics*, vol. 10, no. 12, p. 1453, Jun. 2021, DOI: 10.3390/ELECTRONICS10121453.
- **D. Cittanti**, F. Mandrile, M. Gregorio, and R. Bojoi, "Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging", *Energies*, vol. 14, no. 5, p. 1303, Feb. 2021, DOI: 10.3390/EN14051303.
- F. Mandrile, **D. Cittanti**, V. Mallemaci, and R. Bojoi, "Electric Vehicle Ultra-Fast Battery Chargers: A Boost for Power System Stability?", *World Electric Vehicle Journal*, vol. 12, no. 1, p. 16, Jan. 2021, DOI: 10.3390/WEVJ12010016.

Unrelated to the thesis core topic:

- **D. Cittanti**, C. Gammeter, J. Huber, R. Bojoi, and J. W. Kolar, "A Simplified Hard-Switching Loss Model for Fast-Switching Three-Level T-Type SiC Bridge-Legs", *Electronics*, vol. 11, no. 11, p. 1686, May 2022, DOI: 10.3390/ELECTRONICS11111686.
- **D. Cittanti**, E. Vico, and R. Bojoi, "New FOM-Based Performance Evaluation of 600/650 V SiC and GaN Semiconductors for Next-Generation EV Drives", *IEEE Access*, vol. 10, pp. 51693-51707, May 2022, DOI: 10.1109/ACCESS.2022.3174777.
- **D. Cittanti**, M. Guacci, S. Mirić, R. Bojoi, and J. W. Kolar, "Analysis and Performance Evaluation of a Three-Phase Sparse Neutral Point Clamped Converter for Industrial Variable Speed Drives", *Electrical Engineering*, vol. 104, no. 2, pp. 623–642, Apr. 2022, DOI: 10.1007/S00202-021-01290-W.

- **D. Cittanti**, M. Gregorio, F. Mandrile, and R. Bojoi, "Full Digital Control of an All-Si On-Board Charger Operating in Discontinuous Conduction Mode", *Electronics*, vol. 10, no. 2, p. 203, Jan. 2021, DOI: 10.3390/ELECTRONICS10020203.
- S. Rubino, R. Bojoi, **D. Cittanti**, and L. Zarri, "Decoupled and Modular Torque Control of Multi-Three-Phase Induction Motor Drives", *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 3831–3845, Jul. 2020, DOI: 10.1109/TIA.2020.2991122.

Conference Papers

Related to the thesis core topic:

- **D. Cittanti**, E. Vico, M. Gregorio, and R. Bojoi, "Design and Experimental Assessment of a 60 kW All-Si Three-Phase Six-Leg T-Type Rectifier for Electric Vehicle Ultra-Fast Charging", in *Proc. of the International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME)*, Mauritius, Oct. 2021, DOI: 10.1109/ICECCME52200.2021.9590926.
- **D. Cittanti** and R. Bojoi, "Modulation Strategy Assessment for 3-Level Unidirectional Rectifiers in Electric Vehicle Ultra-Fast Charging Applications", in *Proc. of the AEIT International Conference of Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE)*, Torino, Italy, Nov. 2020, DOI: 10.23919/AEIT AUTOMOTIVE50086.2020.9307416.
- **D. Cittanti**, E. Vico, M. Gregorio, F. Mandrile, and R. Bojoi, "Iterative Design of a 60 kW All-Si Modular LLC Converter for Electric Vehicle Ultra-Fast Charging", in *Proc. of the AEIT International Conference of Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE)*, Torino, Italy, Nov. 2020, DOI: 10.23919/AEITAUTOMOTIVE50086.2020.9307381.
- **D. Cittanti**, M. Gregorio, E. Armando, and R. Bojoi, "Digital Multi-Loop Control of an LLC Resonant Converter for Electric Vehicle DC Fast Charging", in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, Oct. 2020, DOI: 10.1109/ECCE44975.2020.9236177.
- **D. Cittanti**, F. Mandrile, and R. Bojoi, "Optimal Design of Grid-Side LCL Filters for Electric Vehicle Ultra-Fast Battery Chargers", in *Proc. of the International Universities Power Engineering Conference (UPEC)*, Torino, Italy, Sep. 2020, DOI: 10.1109/UPEC49904.2020.9209771.

- **D. Cittanti**, M. Gregorio, and R. Bojoi, "Digital Multi-Loop Control of a 3-Level Rectifier for Electric Vehicle Ultra-Fast Battery Chargers", in *Proc. of the AEIT International Annual Conference (AEIT)*, Catania, Italy, Sep. 2020, DOI: 10.23919/AEIT50178.2020.9241196.

Unrelated to the thesis core topic:

- **D. Cittanti**, E. Vico, F. Mandrile, E. Armando, and R. Bojoi, "Analysis and Conceptualization of a Single-Phase Buck-Boost Integrated EV On-Board Charger Based on a Double Bridge Inverter Drive System", in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, Oct. 2022 (accepted for publication).
- F. Stella, E. Vico, **D. Cittanti**, C. Liu, T. Wu, L. Xiong, and R. Bojoi, "Design and Testing of an Automotive Compliant 800 V 550 kVA SiC Traction Inverter with Full-Ceramic DC-Link and EMI Filter", in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, Oct. 2022 (accepted for publication).
- **D. Cittanti**, E. Vico, E. Armando, and R. Bojoi, "Analysis and Conceptualization of a 400 V 100 kVA Full-GaN Double Bridge Inverter for Next-Generation Electric Vehicle Drives", in *Proc. of the IEEE Transportation Electrification Conference and Exhibition (ITEC)*, Anaheim, CA, USA, Jun. 2022, DOI: 10.1109/ITEC53557.2022.9813847.
- **D. Cittanti**, F. Stella, E. Vico, C. Liu, J. Shen, G. Xiu, and R. Bojoi, "Analysis and Design of a High Power Density Full-Ceramic 900 V DC-Link Capacitor for a 550 kVA Electric Vehicle Drive Inverter", in *Proc. of the International Power Electronics Conference (IPEC – ECCE Asia)*, Himeji, Japan, May 2022, DOI: 10.23919/IPEC-HIMEJI2022-ECCE53331.2022.9807220.
- **D. Cittanti**, E. Vico, E. Armando, and R. Bojoi, "Analysis and Conceptualization of a 800 V 100 kVA Full-GaN Three-Level Flying Capacitor Inverter for Next-Generation Electric Vehicle Drives", in *Proc. of the International Power Electronics Conference (IPEC – ECCE Asia)*, Himeji, Japan, May 2022, DOI: 10.23919/IPEC-HIMEJI2022-ECCE53331.2022.9807091.
- **D. Cittanti**, V. Mallemaci, F. Mandrile, S. Rubino, R. Bojoi, and A. Boglietti, "PWM-Induced Losses in Electrical Machines: An Impedance-Based Estimation Method", in *Proc. of the International Conference on Electrical Machines and Systems (ICEMS)*, Gyeongju, Korea, Oct. 2021, DOI: 10.23919/ICEMS52562.2021.9634438.

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- **D. Cittanti**, M. Guacci, S. Mirić, R. Bojoi, and J. W. Kolar, "Comparative Evaluation of 800 V DC-Link Three-Phase Two/Three-Level SiC Inverter Concepts for Next-Generation Variable Speed Drives", in *Proc. of the International Conference on Electrical Machines and Systems (ICEMS)*, Hamamatsu, Japan, Nov. 2020, DOI: 10.23919/ICEMS50442.2020.9291123.
- S. Rubino, R. Bojoi, **D. Cittanti**, and L. Zarri, "Decoupled Torque Control of Multiple Three-Phase Induction Motor Drives", in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, Sep. 2019, DOI: 10.1109/ECCE.2019.8912502.
- S. Borlo, **D. Cittanti**, M. Gregorio, F. Mandrile, and S. Musumeci, "Comparative CCM-DCM Design Evaluation of Power Inductors in Interleaved PFC Stage for Electric Vehicle Battery Chargers", in *Proc. of the International Conference on Clean Electrical Power (ICCEP)*, Otranto, Italy, Jul. 2019, DOI: 10.1109/ICCEP.2019.8890112.

Patents

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PART I

AC/DC Converter

Chapter 2

AC/DC Converter – Analysis

Abstract

The AC/DC conversion stage of an electric vehicle (EV) ultra-fast battery charger must absorb the total charging power from the grid, meanwhile ensuring sinusoidal input current shaping with low harmonic content. Due to the strict conversion efficiency and power density targets set by the application, pulse-width modulated (PWM) active rectifiers are the most suitable converter candidates, ensuring lower current distortion, wider regulation capability and higher overall performance with respect to passive and/or hybrid rectification solutions. In this chapter, an overview of the existing three-phase PWM converter topologies for general active rectification is provided and a unidirectional three-level T-type structure is selected for the present 60 kW application. The operational basics of three-level unidirectional rectifiers are described, including a detailed analysis of the converter operating limits in terms of e.g., modulation index (i.e., voltage range), power factor angle (i.e., reactive power capability) and DC-link mid-point current (i.e., operation under unbalanced split DC-link loading). Moreover, the converter modulation process is explained and seven different modulation strategies are introduced. Finally, the stresses on the converter active and passive components (i.e., semiconductor losses, DC-link RMS current and charge ripple, AC-side inductor RMS and peak-to-peak flux ripple) are assessed analytically and/or numerically for all modulation strategies, providing straightforward tools for the converter design.

2.1 Introduction

The grid-tied AC/DC converter of an EV ultra-fast battery charger has the fundamental role of supplying the subsequent DC/DC conversion stage with the total amount of charging power. In doing so, the AC/DC converter must ensure:

- regulated output (i.e., DC-link) voltage, as this should not be affected by the variation of the grid voltage and/or the charging power;
- sinusoidal input current with limited harmonics (i.e., according to IEEE 519 [10, 11]) and a total harmonic distortion (THD) lower than 5 %;
- ohmic-equivalent grid behavior with a displacement power factor (DPF) higher than 0.99 ;
- high conversion efficiency and power density.

These requirements directly exclude both passive rectification solutions (e.g., diode rectifiers with inductive/capacitive smoothing, multi-pulse rectifiers, etc.) and hybrid rectification solutions (e.g., combinations of diode rectifiers and DC/DC converters, third-harmonic injection systems, etc.), since these systems either fail to comply with the AC-side or DC-side requirements or may not achieve a sufficient trade-off between conversion efficiency and overall converter volume (i.e., including the filtering components) [46, 47]. Therefore, only pulse-width modulated (PWM) active rectifiers, also known as active front-ends (AFEs) or power factor correctors (PFCs), feature the necessary characteristics and performance for the present application.

2.1.1 Converter Topologies

Among three-phase active rectification solutions, a major distinction must be made between voltage-source boost-type rectifiers (i.e., inductive AC-side, capacitive DC-side) and current-source buck-type rectifiers (i.e., capacitive AC-side, inductive DC-side). In particular, boost-type rectifiers can only regulate the output voltage to be higher than the grid line-to-line peak voltage (i.e., V_{ll}) , whereas buck-type rectifiers can only operate with an output voltage below $\sqrt{3}/2\,V_{ll}$. In the present case, only voltage-source boost-type converters are considered, as they typically feature lower complexity, lower semiconductor count and higher efficiency than current-source buck-type solutions, especially considering the practical realization of the bipolar switches required by current-source converters. It is worth noting that the buck-boost functionality of the complete battery charger is ensured by the combination of the DC/DC stage (i.e., featuring a buck-boost characteristic) and the modular, reconfigurable structure of the charging module outlined in **Section 1.3**.

At present, the most widespread topology for three-phase active rectification is the two-level six-switch rectifier/inverter (cf. **Fig. 2.1(a)**), being simple, well-understood, reliable and intrinsically bidirectional. However, the performance achievable by this converter topology in terms of efficiency/power density trade-off is significantly limited by its two-level

output voltage waveform (i.e., requiring large AC-side filtering elements) and by the high voltage rating of the semiconductor devices (i.e., featuring relatively poor conduction and switching characteristics) [48–50]. In particular, assuming a full-Si AC/DC converter realization with a maximum DC-link voltage of 800 V (cf. **Chapter 3**), the two-level bridge-leg structure requires the adoption of 1200 V IGBTs with 1200 V antiparallel diodes, as shown in **Fig. 2.1(a)**. Due to the bipolar nature of IGBTs/diodes (i.e., featuring tail-current and reverse-recovery phenomena) and the high switched voltage, Si-based two-level converters feature poor switching performance and are thus not suited for the present application.

The most effective approach to enhance the overall performance of the rectifier is by adopting multi-level topologies, which simultaneously reduce the stress on the AC-side filter components and allow to employ semiconductor devices with lower voltage rating and thus better figures-of-merit [51]. Nonetheless, as the total count of semiconductor devices and driving circuits scales with the number of introduced levels, the increase in complexity and control effort rapidly counteracts the performance benefits of multi-level topologies, thus limiting the number of practically useful levels in low-voltage applications. Since DC fast chargers typically require unidirectional power flow from the grid to the vehicle, three-level rectifiers represent an attractive alternative to the two-level inverter, trading higher efficiency and power density for a slight complexity increase [46, 47, 52, 53]. In fact, these converter topologies are able to generate a three-level output voltage waveform employing a low number of active switches (i.e., equal or lower with respect to the two-level inverter) and ensuring minimum modulation complexity, as no switching dead-times need to be provided (i.e., each bridge-leg features only one bidirectional bipolar switch that cannot short-circuit the DC-link). Additionally, in three-level rectifiers the active

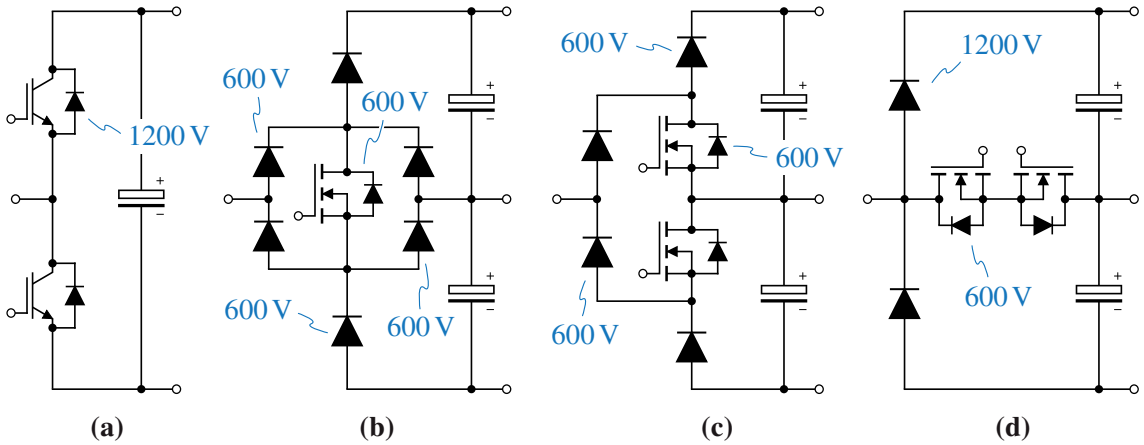


Fig. 2.1: Bridge-leg equivalent circuit schematics of **(a)** the two-level rectifier, **(b)** the three-level VIENNA-type rectifier, **(c)** the three-level NPC-type rectifier, and **(d)** the three-level T-type rectifier. A maximum DC-link voltage of 800 V is assumed and Si IGBTs, MOSFETs and diodes are considered.

devices must only switch half of the DC-link voltage (i.e., 400 V), allowing for a significant reduction of the switching losses and enabling the adoption of 600 V Si MOSFETs, which feature far better switching characteristics than 1200 V IGBTs. Therefore, the combination of increased switching frequency and multi-level output voltage waveform allows to dramatically reduce size of the passive components (i.e., dominating the converter volume) and thus significantly improve power density at constant efficiency or vice-versa.

There are three main variants of the unidirectional three-level rectifier:

- VIENNA-type (cf. **Fig. 2.1(b)**); each bridge-leg employs one 600 V transistor, four 600 V line-frequency diodes (i.e., commutating with the grid frequency, featuring low cost and relatively low on-state voltage drop) and two 600 V fast-recovery diodes (i.e., commutating with the switching frequency, featuring relatively high cost and high on-state voltage drop). The transistor, together with the four line-frequency diodes connected around it, forms a bipolar bidirectional (i.e., four-quadrant, 4Q) switch. The main advantages of this topology are the reduced voltage rating (i.e., 600 V) of all semiconductor devices and the requirement of only three transistors (and gate drivers) for the whole converter. Conversely, the disadvantages are the high total part count (i.e., seven semiconductor devices per bridge-leg), the relatively large conduction losses (i.e., due to the presence of two diodes or two diodes and one transistor in the conduction path) and the unfavorable switching frequency commutation loop (i.e., which includes the parasitic inductance of three elements).
- NPC-type (cf. **Fig. 2.1(c)**); each bridge-leg consists of two 600 V transistors, two 600 V line-frequency diodes and two 600 V fast-recovery diodes. By modifying the structure of the 4Q switch with respect to the VIENNA-type implementation (i.e., adding one transistor and eliminating two line-frequency diodes), the neutral point clamped (NPC) rectifier achieves reduced conduction losses by having only one transistor and one diode in the conduction path when the AC node is connected to the DC-link mid-point. Furthermore, the NPC topology benefits from a low switching frequency commutation loop inductance (i.e., involving only two elements), thus allowing for enhanced switching performance and simple layout. Nonetheless, each NPC bridge-leg still features a high component count (i.e., six semiconductor devices and two gate drivers) and relatively large conduction losses.
- T-type (cf. **Fig. 2.1(d)**); each bridge-leg employs two 600 V transistors in anti-series connection (i.e., forming the 4Q switch) and two 1200 V fast-recovery diodes. The T-type bridge-leg structure allows to minimize conduction losses, as the conduction path is either through a single diode or two transistors. Therefore, despite adopting 1200 V diodes (i.e., featuring relatively high reverse-recovery charge) and having three

elements within a switching frequency commutation loop (i.e., leading to high parasitic inductance), the T-type rectifier provides considerable advantages with respect to the other three-level topologies, namely reduced component count (i.e., four semiconductor devices and only one gate driver per bridge-leg) and low conduction losses.

Overall, the three-phase three-level unidirectional T-type rectifier provides the most promising converter-level performance, combining the advantages of the two-level inverter (i.e., low semiconductor and gate driver count, low conduction loss) and the three-level VIENNA-type and NPC-type rectifiers (i.e., transistors with reduced voltage rating and high switching performance, three-level output voltage waveform). For these reasons, the T-type topology is considered for the AC/DC conversion stage of the 60 kW ultra-fast battery charging converter module.

2.1.2 Key Challenges

Despite achieving an excellent compromise among cost, complexity and overall performance, three-level rectifiers feature unique challenges. For instance, one key issue of unidirectional rectifiers is the discontinuous conduction mode (DCM) operation around the current zero-crossings, which, if not correctly addressed, can lead to unacceptable phase current distortion in light load conditions [54]. Furthermore, besides having to ensure sinusoidal input current shaping, regulated output voltage, ohmic grid behavior and high efficiency/power density, three-level rectifiers must also control the DC-link mid-point voltage deviation (i.e., the voltage balancing between the two DC-link capacitors), as this increases the voltage stress on the semiconductor devices and negatively affects the AC-side current quality [55]. In particular, the voltage balancing feature must be ensured also when a split DC-link load unbalance occurs, which may be the case when separate DC/DC converters are connected to the split DC-link outputs (cf. **Section 1.3**).

Other desirable features (i.e., which are not strictly required) include the minimization of the DC-link mid-point low-frequency voltage oscillation [56, 57], which directly affects the size of the DC-link capacitors and may be hard to reject by the DC/DC conversion stage (cf. **Chapter 7**), and the operation under non-unity power factor, to support the reactive energy flows in distribution grids [13]. Both features are quite challenging to achieve, since the unidirectional nature of three-level rectifiers limits the maximum converter-side displacement power factor (DPF) and affects the DC-link mid-point generation process, limiting the converter ability to compensate the mid-point voltage oscillation.

Part of the content of this chapter has been published in [58] and [59].

2.2 Operating Principle and Limits

Even though the 60 kW rectifier is divided in two paralleled 30 kW converter units, these are assumed to be operated with synchronized and in-phase PWM carriers (cf. **Section 3.1.1**). Therefore, the considered six-leg T-type converter can be analyzed as a generic unidirectional three-phase three-level rectifier, shown in **Fig. 2.2**.

Each converter bridge-leg features two diodes that provide a passive connection between the AC input and the upper/lower DC-link rails (i.e., depending on the current direction), and a bipolar, bidirectional four-quadrant (4Q) switch, which actively connects the AC input to the DC-link mid-point. Notably, the 4Q switch types shown in **Fig. 2.2(a)** and **Fig. 2.2(b)** are typically integrated inside the input diode bridge (cf. **Fig. 2.1(b)**, **(c)**), allowing for the use of diodes with halved voltage rating. To simplify the following analysis and achieve compact analytical expressions (i.e., useful for the converter design and control), the DC-side loads connected to the upper and lower DC-link halves are assumed as ideal current-sources, whereas no inner grid impedance and no AC-side filter are considered.

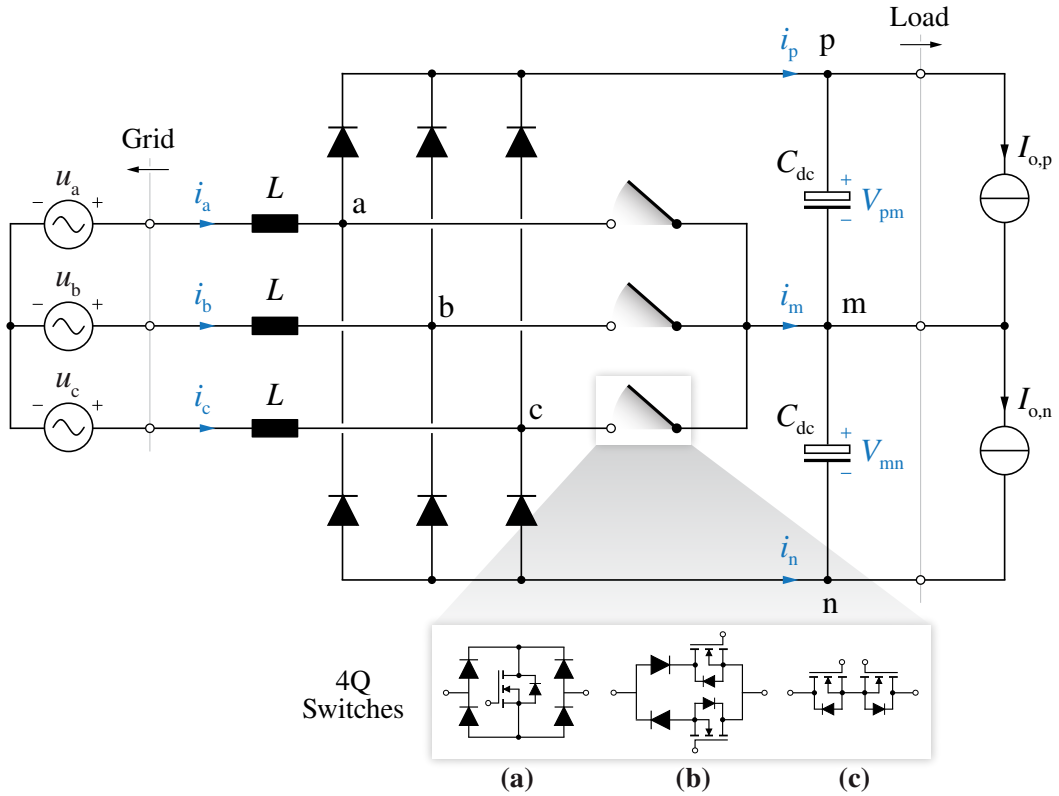


Fig. 2.2: Equivalent circuit schematic of a generic grid-connected three-phase three-level unidirectional rectifier. The mid-point switches are bipolar and bidirectional, i.e., four-quadrant (4Q). A highlight of the possible 4Q switch topologies is provided, namely **(a)** the VIENNA-type, **(b)** the NPC-type, and **(c)** the T-type: switches **(a)** and **(b)** are typically integrated inside the input diode bridge (cf. **Fig. 2.1(b)**, **(c)**), allowing for the use of diodes with halved voltage rating.

2.2.1 Basics of Operation

The system state variables defining the converter operation are the AC-side inductor currents i_a, i_b, i_c and the DC-link capacitor voltages V_{pm}, V_{mn} (cf. **Fig. 2.2**). Due to the three-phase three-wire nature of the system

$$i_a + i_b + i_c = 0, \tag{2.1}$$

therefore only two currents are independent and the total number of state variables is reduced to four. Moreover, the DC-link capacitor voltages V_{pm} and V_{mn} can be rearranged to define the DC-link voltage V_{dc} and the mid-point voltage deviation V_m, respectively

$$V_{dc} = V_{pm} + V_{mn}, \tag{2.2}$$

$$V_m = V_{pm} - V_{mn}. \tag{2.3}$$

Notably, in normal operating conditions $V_m = 0$ assuming balanced split DC-link voltages $V_{pm} = V_{mn} = V_{dc}/2$.

Disregarding the voltage drop at fundamental frequency across the AC-side inductance L (i.e., negligible for converters with high switching-to-fundamental frequency ratios [57]), the phase voltage local averages applied by the rectifier can be expressed as

$$\begin{cases} v_a = M \dfrac{V_{dc}}{2} \cos(\vartheta) \\ v_b = M \dfrac{V_{dc}}{2} \cos(\vartheta - \frac{2}{3}\pi) \\ v_c = M \dfrac{V_{dc}}{2} \cos(\vartheta - \frac{4}{3}\pi) \end{cases}, \tag{2.4}$$

where $\vartheta = \omega t = 2\pi f t$ is the phase angle, f is the grid frequency, $M = 2V/V_{dc}$ is the modulation index of the rectifier and $V \approx U$ is the phase voltage peak value. For the sake of completeness, the phase voltages v_a, v_b, v_c can be represented with a space vector approach as

$$\vec{V} = \frac{2}{3}\left(v_a e^{j0} + v_b e^{j2\pi/3} + v_c e^{j4\pi/3}\right), \tag{2.5}$$

where j is the imaginary operator.

Neglecting the switching ripple, the controlled phase currents are sinusoidal and are therefore expressed by

$$\begin{cases} i_a = I \cos(\vartheta - \varphi) \\ i_b = I \cos(\vartheta - \frac{2}{3}\pi - \varphi) \\ i_c = I \cos(\vartheta - \frac{4}{3}\pi - \varphi) \end{cases}, \tag{2.6}$$

where I is the phase current peak value and φ is the converter-side power factor angle (i.e., $\varphi = \angle v_x - \angle i_x$ with x = a, b, c). Similarly to the phase voltages, i_a, i_b, i_c can be expressed with an equivalent space vector representation as

$$\vec{I} = \frac{2}{3}\left(i_a e^{j0} + i_b e^{j2\pi/3} + i_c e^{j4\pi/3}\right). \tag{2.7}$$

Due to the structure of a three-level unidirectional rectifier, the AC terminal of each bridge-leg may be actively connected to the DC-link mid-point (switch in the ON state) or, depending on the phase current direction, passively connected to either the positive or negative DC-link rails (switch in the OFF state). Consequently, the voltage applied by each bridge-leg with respect to the DC-link mid-point can assume three different values, namely 0, $+V_{dc}/2$ and $-V_{dc}/2$, which correspond to three separate switching states.

The total number of switching state combinations of a three-phase three-level rectifier is theoretically $3^3 = 27$; however all three bridge-legs cannot be connected to the positive or negative DC-link rails at the same time due to the bridge diodes (i.e., $i_a + i_b + i_c = 0$), therefore the total number of states is reduced to 25. The overall number of space vectors can be derived by observing that six space vectors are redundant, leading to total space vector number of $25 - 6 = 19$. An overview of the space vector diagram of a three-level rectifier is provided in **Fig. 2.3(a)**.

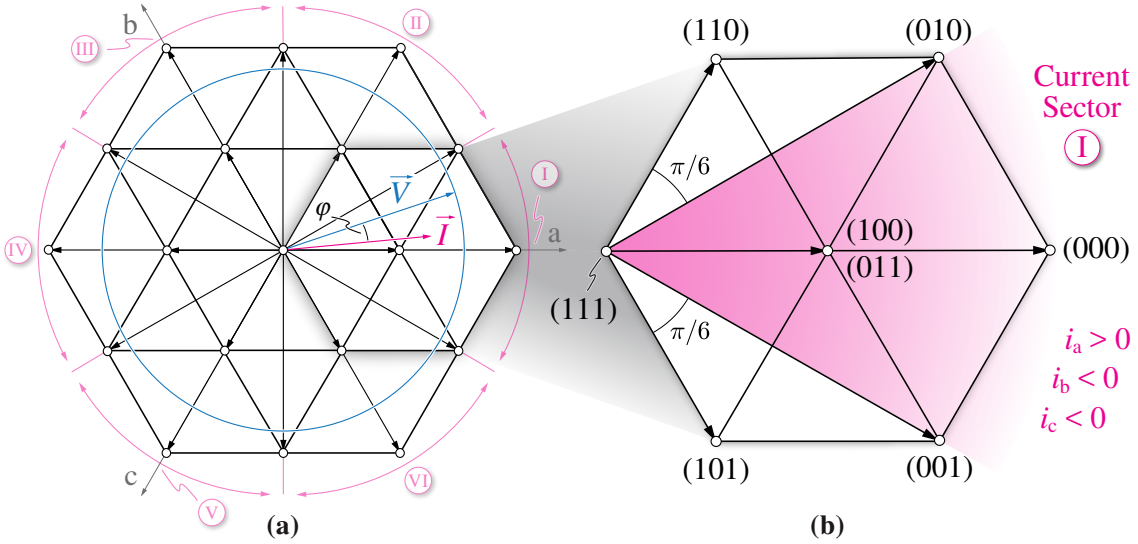


Fig. 2.3: Complete space vector diagram of a unidirectional three-phase three-level rectifier. An overview of the 19 available space vectors, the 6 separate current sectors, the phase voltage vector $\vec{V}$, the phase current vector $\vec{I}$ and the converter-side power factor angle φ is shown in **(a)**. A focus on the voltage space vector hexagon available when $\vec{I}$ is transiting inside current sector Ⓘ is provided in **(b)**: the switching states are defined by the combination of the 4Q switch signals s_x, i.e., 0 when the 4Q switch is OFF and 1 when the 4Q switch is ON.

Due to their unidirectional nature, three-level rectifiers cannot apply all 19 space vectors at any given time, as the feasible bridge-leg voltage values depend on the direction of the phase currents. The 6 different phase current direction combinations (i.e., $2^3 - 2$, being $i_a + i_b + i_c = 0$) define 6 separate regions in the space vector diagram, referred to as current sectors in the following. When the current vector $\vec{I}$ transits through these regions, each bridge-leg can only apply two out of the three possible states, leading to a total of $2^3 = 8$ switching combinations. Therefore, the total number of allowed space vectors becomes 7, being 1 switching combination redundant. The 7 available voltage space vectors when $\vec{I}$ is located within current sector Ⓘ (i.e., $i_a > 0$, $i_b < 0$, $i_c < 0$) are illustrated in **Fig. 2.3(b)**. The highlighted hexagon indicates that whatever voltage space vector $\vec{V}$ located inside the hexagon itself may be generated with a suitable combination of the 7 available space vectors.

AC-Side Voltage Generation

The local average of the bridge-leg voltages applied by the rectifier (v_{xm}) can be expressed as the sum of two contributions, namely the phase voltage component v_x and the zero-sequence voltage component v_o, as

$$v_{xm} = v_x + v_o \qquad x = a, b, c. \tag{2.8}$$

The phase voltages v_a, v_b, v_c are controlled to regulate the converter input currents i_a, i_b, i_c according to their reference sinusoidal values, being

$$\frac{di_x}{dt} = \frac{u_x - v_x}{L} \quad x = a, b, c. \tag{2.9}$$

As previously explained, because of the relatively low value of L in systems with high switching-to-fundamental frequency ratios, the low-frequency voltage drop across the AC-side inductors can typically be neglected [57], such that $v_x \approx u_x$.

The zero-sequence component v_o is defined as the average of the three bridge-leg voltages, i.e.,

$$v_o = \frac{v_{am} + v_{bm} + v_{cm}}{3}. \tag{2.10}$$

Even though v_o has no effects on the phase current generation process in a three-phase three-wire system, it defines the modulation strategy of the rectifier (cf. **Section 2.3**), affecting the high-frequency stresses on the AC-side inductors and DC-link capacitors (cf. **Section 2.4**), and may be leveraged to regulate the DC-link mid-point current, as shown in the following.

DC-Side Current Generation

The three DC-link rail currents i_{p}, i_{m}, i_{n} indicated in **Fig. 2.2** are bounded by the following relation:

$$i_{\mathrm{p}} + i_{\mathrm{m}} + i_{\mathrm{n}} = 0, \tag{2.11}$$

due to the three-wire DC-link structure.

In particular, i_{p} and i_{n} are linked to the total power transfer of the rectifier, being

$$P = v_{\mathrm{a}}\, i_{\mathrm{a}} + v_{\mathrm{b}}\, i_{\mathrm{b}} + v_{\mathrm{c}}\, i_{\mathrm{c}} = V_{\mathrm{pm}}\, i_{\mathrm{p}} - V_{\mathrm{mn}}\, i_{\mathrm{n}} \approx \frac{1}{2} V_{\mathrm{dc}}\, (i_{\mathrm{p}} - i_{\mathrm{n}}), \tag{2.12}$$

where balanced split DC-link voltages (i.e., $V_{\mathrm{pm}} = V_{\mathrm{mn}} = V_{\mathrm{dc}}/2$) are assumed.

The generation process of the DC-link mid-point current i_{m} is slightly more complicated and has been investigated in several papers [55, 56, 60]. The main driver of i_{m} is the zero-sequence voltage component v_{o} injected by the converter. Even though this component does not affect the phase currents, it modifies the duty cycles (i.e., relative ON-times) τ_{a}, τ_{b}, τ_{c} of the mid-point 4Q switches, which in turn affect the mid-point current local average value, namely

$$i_{\mathrm{m}} = \tau_{\mathrm{a}}\, i_{\mathrm{a}} + \tau_{\mathrm{b}}\, i_{\mathrm{b}} + \tau_{\mathrm{c}}\, i_{\mathrm{c}}. \tag{2.13}$$

The values of τ_{a}, τ_{b}, τ_{c} are determined by the ratio between their respective reference bridge-leg voltages v_{xm} and the DC-link voltage V_{dc} as

$$\tau_{\mathrm{x}} = 1 - \frac{2}{V_{\mathrm{dc}}} |v_{\mathrm{xm}}| = 1 - \frac{2}{V_{\mathrm{dc}}} |v_{\mathrm{x}} + v_{\mathrm{o}}| \qquad \mathrm{x} = \mathrm{a,\, b,\, c}. \tag{2.14}$$

Leveraging the three-phase three-wire nature of the system (i.e., $i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}} = 0$) and substituting (2.14) into (2.13), the expression of the mid-point current local average becomes

$$i_{\mathrm{m}} = \sum_{\mathrm{x=a,b,c}} \left(i_{\mathrm{x}} - \frac{2}{V_{\mathrm{dc}}} |v_{\mathrm{x}} + v_{\mathrm{o}}|\, i_{\mathrm{x}} \right) = \sum_{\mathrm{x=a,b,c}} -\frac{2}{V_{\mathrm{dc}}} |v_{\mathrm{x}} + v_{\mathrm{o}}|\, i_{\mathrm{x}}. \tag{2.15}$$

A simplified version of (2.15) can be obtained by recalling that the bridge-leg voltages applied by a three-level unidirectional rectifier can only have the same sign as their respective phase currents (i.e., $v_{\mathrm{xm}} \geq 0$ when $i_{\mathrm{x}} > 0$ and $v_{\mathrm{xm}} \leq 0$ when $i_{\mathrm{x}} < 0$). Therefore, the following relation can be derived:

$$|v_{\mathrm{xm}}|\, i_{\mathrm{x}} = |v_{\mathrm{x}} + v_{\mathrm{o}}|\, i_{\mathrm{x}} = (v_{\mathrm{x}} + v_{\mathrm{o}})\, |i_{\mathrm{x}}| \quad \mathrm{x} = \mathrm{a,\, b,\, c}, \tag{2.16}$$

which is then substituted into (2.15) obtaining

$$i_{\mathrm{m}} = \sum_{\mathrm{x=a,b,c}} -\frac{2}{V_{\mathrm{dc}}} (v_{\mathrm{x}} + v_{\mathrm{o}})\, |i_{\mathrm{x}}| = -\frac{2}{V_{\mathrm{dc}}} \left[\sum_{\mathrm{x=a,b,c}} v_{\mathrm{x}}\, |i_{\mathrm{x}}| + v_{\mathrm{o}} \sum_{\mathrm{x=a,b,c}} |i_{\mathrm{x}}| \right]. \tag{2.17}$$

To assess the ability of the rectifier to work with unbalanced split DC-link loading (i.e., $I_{o,p} \neq I_{o,n}$, cf. **Fig. 2.2**), the expression of the mid-point current periodical average I_m is of particular interest. This is obtained by averaging the value of i_m over $2\pi/3$ (i.e., the DC-side current periodicity), as

$$I_m = \frac{3}{2\pi} \int_0^{2\pi/3} i_m \, d\vartheta = -\frac{3}{\pi V_{dc}} \int_0^{2\pi/3} \left[\sum_{x=a,b,c} v_x |i_x| + v_o \sum_{x=a,b,c} |i_x| \right] d\vartheta. \tag{2.18}$$

Since the first term to be integrated is characterized by $2\pi/3$ periodicity, its integral is null, therefore (2.18) becomes

$$I_m = -\frac{3}{\pi V_{dc}} \int_0^{2\pi/3} v_o \sum_{x=a,b,c} |i_x| \, d\vartheta. \tag{2.19}$$

2.2.2 Zero-Sequence Voltage Limits

The zero-sequence voltage local average that can be applied by a three-level unidirectional rectifier is dynamically limited by the feasible three-phase bridge-leg voltage values, which depend on the signs of the respective phase currents [61], as

$$\begin{cases} 0 \leq v_{xm} \leq +V_{pm} & i_x > 0 \\ -V_{mn} \leq v_{xm} \leq 0 & i_x < 0 \end{cases} \qquad x = a, b, c. \tag{2.20}$$

Assuming balanced split DC-link voltages, namely $V_{pm} = V_{mn} = V_{dc}/2$, (2.20) can be rewritten as

$$\begin{cases} v_{xm} \leq \dfrac{\text{sign}(i_x)+1}{2} \dfrac{V_{dc}}{2} \\ v_{xm} \geq \dfrac{\text{sign}(i_x)-1}{2} \dfrac{V_{dc}}{2} \end{cases} \qquad x = a, b, c. \tag{2.21}$$

Finally, leveraging the bridge-leg voltage definition (2.8), the maximum and minimum zero-sequence voltage limits are obtained:

$$\begin{cases} v_{o,max} = \min \left[\dfrac{V_{dc}}{4} (\text{sign}(i_x)+1) - v_x \right] \\ v_{o,min} = \max \left[\dfrac{V_{dc}}{4} (\text{sign}(i_x)-1) - v_x \right] \end{cases} \qquad x = a, b, c, \tag{2.22}$$

which are characterized by a $2\pi/3$ periodicity. A graphical representation of (2.22) is shown in **Fig. 2.4** for different values of M, and in **Fig. 2.5** for different values of φ. It is primarily observed that a reduction of M widens the feasible zero-sequence injection region, whereas $\varphi \neq 0$ determines the impossibility to apply $v_o = 0$ around the phase current zero-crossings. In particular, this last feature affects the ability of the converter to eliminate the low-frequency mid-point voltage oscillation, as demonstrated in **Section 2.4.2**.

2.2.3 Modulation Index Limits

The modulation index limits of a three-level rectifier can be easily derived from the zero-sequence voltage limits reported in (2.22). It is observed from **Fig. 2.4** that increasing values of M reduce the feasible zero-sequence injection region. Therefore, the maximum modulation index value that preserves linearity in the voltage formation process (i.e., ensuring no low-frequency AC voltage distortion) is found from the intersection of $v_{o,max}$ and $v_{o,min}$, as shown in **Fig. 2.4(c)**. Focusing on $\vartheta \in [0, \pi/3]$, this intersection corresponds to setting $V_{dc}/2 - v_a = -V_{dc}/2 - v_c$ with $\vartheta = \pi/6$. By leveraging the phase voltage definitions

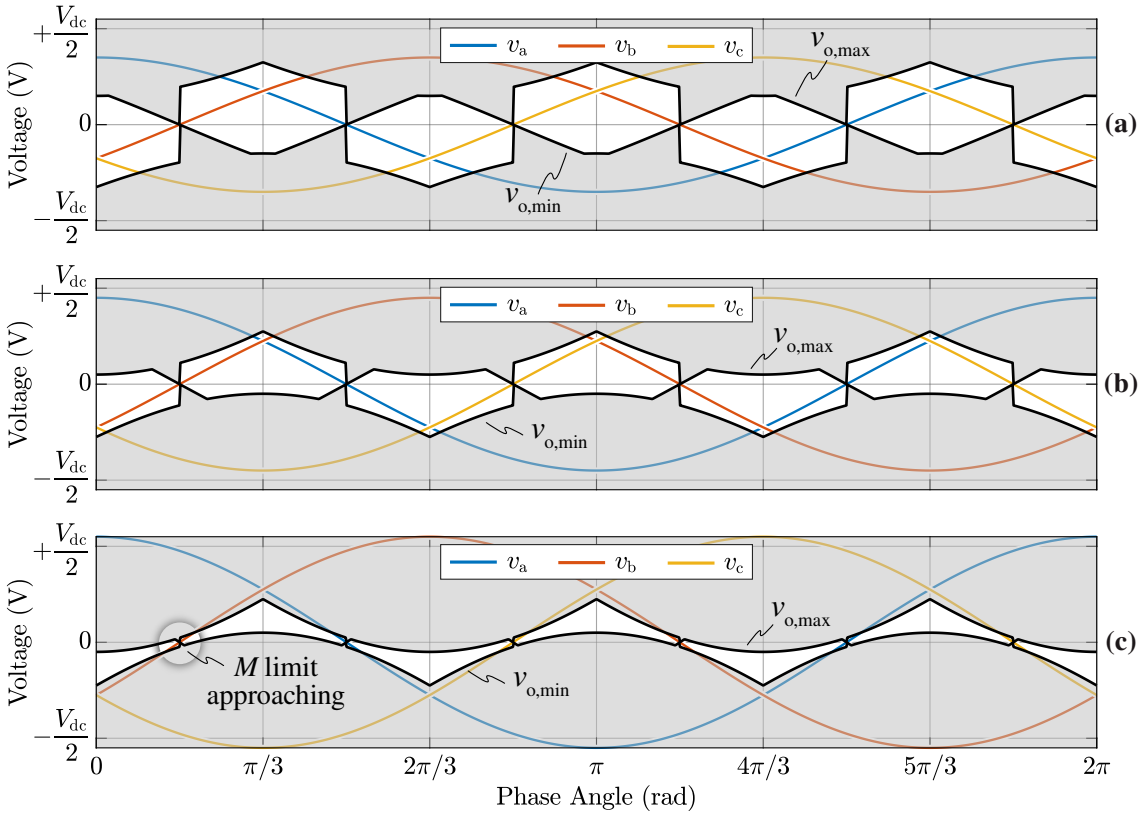


Fig. 2.4: Zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ for **(a)** $M = 0.7$, **(b)** $M = 0.9$, and **(c)** $M = 1.1$, assuming $\varphi = 0$ (unity power factor operation), i.e. $\text{sign}(i_x) = \text{sign}(v_x)$.

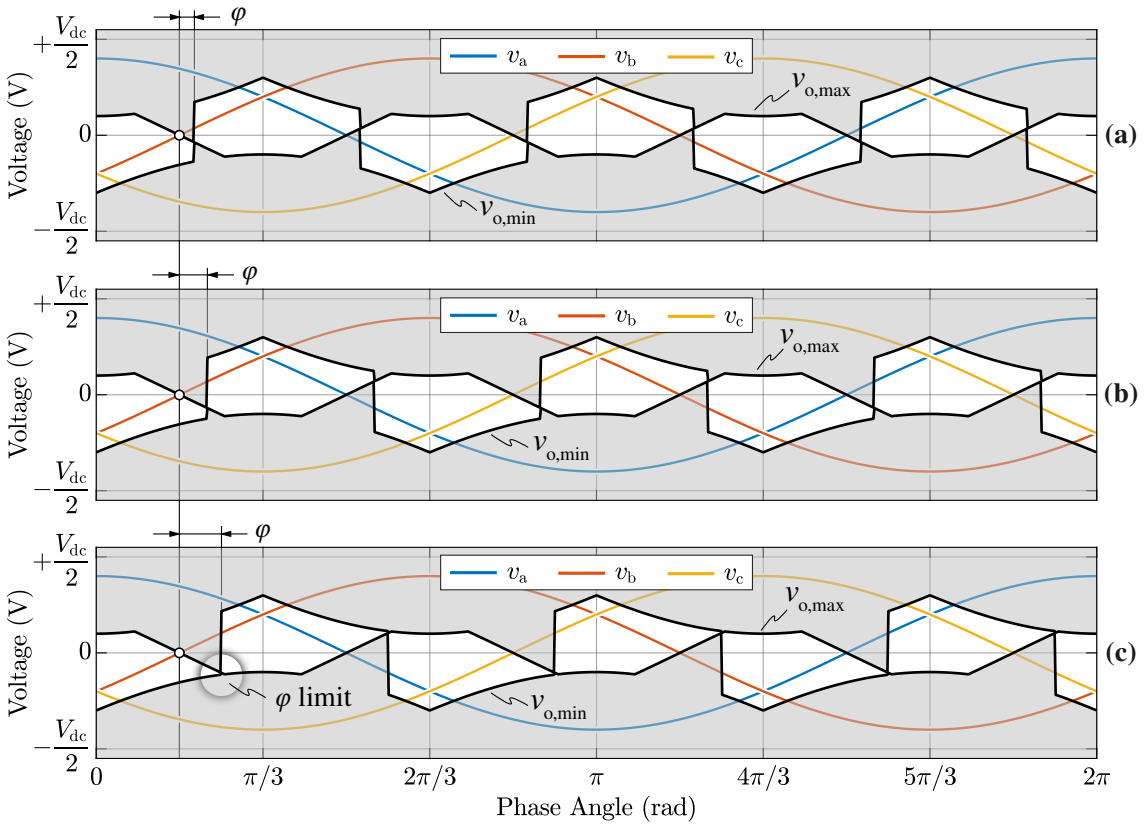


Fig. 2.5: Zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ for **(a)** $\varphi = 5°$, **(b)** $\varphi = 10°$, and **(c)** $\varphi = 15°$, assuming $M = 0.8$.

in (2.4), the maximum modulation index is obtained as

$$M_{max} = \frac{2}{\sqrt{3}} \approx 1.15, \tag{2.23}$$

which corresponds to the limit of conventional three-phase bidirectional two-level and three-level converters. The same results can be obtained by geometrical considerations on the space vector diagram reported in **Fig. 2.3** [52, 61].

It is worth highlighting that the typical rectifier operation is restricted to $M > 2/3$ (i.e., region ③, cf. **Fig. 2.9**), as lower modulation indices would translate into a DC-link voltage higher than $\approx 975\,\mathrm{V}$ for the European low-voltage grid (i.e., $400\,\mathrm{V_{RMS}}$ line-to-line).

2.2.4 Power Factor Angle Limits

Even though three-level rectifiers can operate with non-unity power factor, their reactive power capabilities are limited by their unidirectional nature, as the AC-side voltage formation depends on the phase current sign. The converter φ limits can be derived from

the instantaneous zero-sequence limits reported in (2.22). In particular, the maximum allowed φ at a certain modulation index value M is found from the intersection between $v_{o,max}$ and $v_{o,min}$, as illustrated in **Fig. 2.5(c)**. Focusing on $\vartheta \in [0, \pi/3]$, this intersection corresponds to setting $v_b = v_c + V_{dc}/2$. By leveraging the phase voltage definitions in (2.4), the following expression of the converter-side power factor angle limits is obtained:

$$\varphi_{max} = -\varphi_{min} = \sin^{-1}\left(\frac{1}{\sqrt{3}M}\right) - \frac{\pi}{6} \qquad M \geq \frac{2}{3}, \tag{2.24}$$

which is valid for $2/3 \leq M \leq 2/\sqrt{3}$. With a similar procedure, it can be demonstrated that for lower values of M (i.e., not typical in rectifier applications) the power factor angle is limited within $\varphi \in [-\pi/6, +\pi/6]$. Also in this case, the same results can be obtained by geometrical considerations on the space vector diagram reported in **Fig. 2.3** [52, 61]. In fact, the required continuity of the voltage vector $\vec{V}$ when transitioning between neighboring sectors enforces a maximum angle between $\vec{V}$ and $\vec{I}$, depending on the modulation index M value. For instance, it is clear that $|\varphi| > \pi/6$ cannot be realized for any value of M, as the voltage vector $\vec{V}$ would temporarily fall out of the available space vector hexagon.

As a further note, it is worth highlighting that the values of φ_{max}, φ_{min} derived herein refer to the maximum operating region of the rectifier that ensures no low-frequency harmonics in the input current. In fact, higher values of φ can be obtained if low-frequency distortion is accepted, however the rectifier input current can no longer remain sinusoidal and may not comply with the harmonic limits prescribed by the grid-code [10, 11].

2.2.5 Mid-Point Current Limits

Since the generation process of the DC-link mid-point current i_m depends on the zero-sequence voltage injection (cf. **Section 2.2.1**), it is easily understood that $v_{o,max}$ and $v_{o,min}$ directly limit the feasible values of the mid-point current local average. The upper and lower i_m limits can therefore be derived substituting (2.22) into (2.17), obtaining

$$\begin{cases} i_{m,max} = -\dfrac{2}{V_{dc}}\left[\displaystyle\sum_{x=a,b,c} v_x\,|i_x| + v_{o,min}\sum_{x=a,b,c}|i_x|\right] \\ i_{m,min} = -\dfrac{2}{V_{dc}}\left[\displaystyle\sum_{x=a,b,c} v_x\,|i_x| + v_{o,max}\sum_{x=a,b,c}|i_x|\right] \end{cases}. \tag{2.25}$$

A graphical representation of (2.25) is shown in **Fig. 2.6** for different values of M, and in **Fig. 2.7** for different values of φ. It is observed that a reduction of M increases the mid-point current generation capability of the converter, whereas $\varphi \neq 0$ forces $i_{m,max}$ and

$i_{m,min}$ to cross the line defined by $i_m = 0$, thus preventing to achieve a zero mid-point current local average over the complete fundamental period.

The mid-point current periodical average I_m limits identify the ability of the rectifier to operate under unbalanced split DC-link loading (i.e., being $I_m = I_{o,n} - I_{o,p}$) [55], and can be calculated by averaging $i_{m,max}$ and $i_{m,min}$ along the grid period (i.e., integrating (2.25) over $2\pi/3$). In particular, being the integrals of $i_{m,max}$ and $i_{m,min}$ identical but with opposite sign, the I_m limits are symmetrical:

$$I_{m,max} = -I_{m,min} = -\frac{3}{\pi V_{dc}} \int_0^{2\pi/3} \left[\sum_{x=a,b,c} v_x |i_x| + v_{o,min} \sum_{x=a,b,c} |i_x| \right] d\vartheta. \tag{2.26}$$

Due to the $2\pi/3$ periodicity of the first term, its integral is null, thus resulting in

$$I_{m,max} = -\frac{3}{\pi V_{dc}} \int_0^{2\pi/3} v_{o,min} \left(|i_a| + |i_b| + |i_c| \right) d\vartheta. \tag{2.27}$$

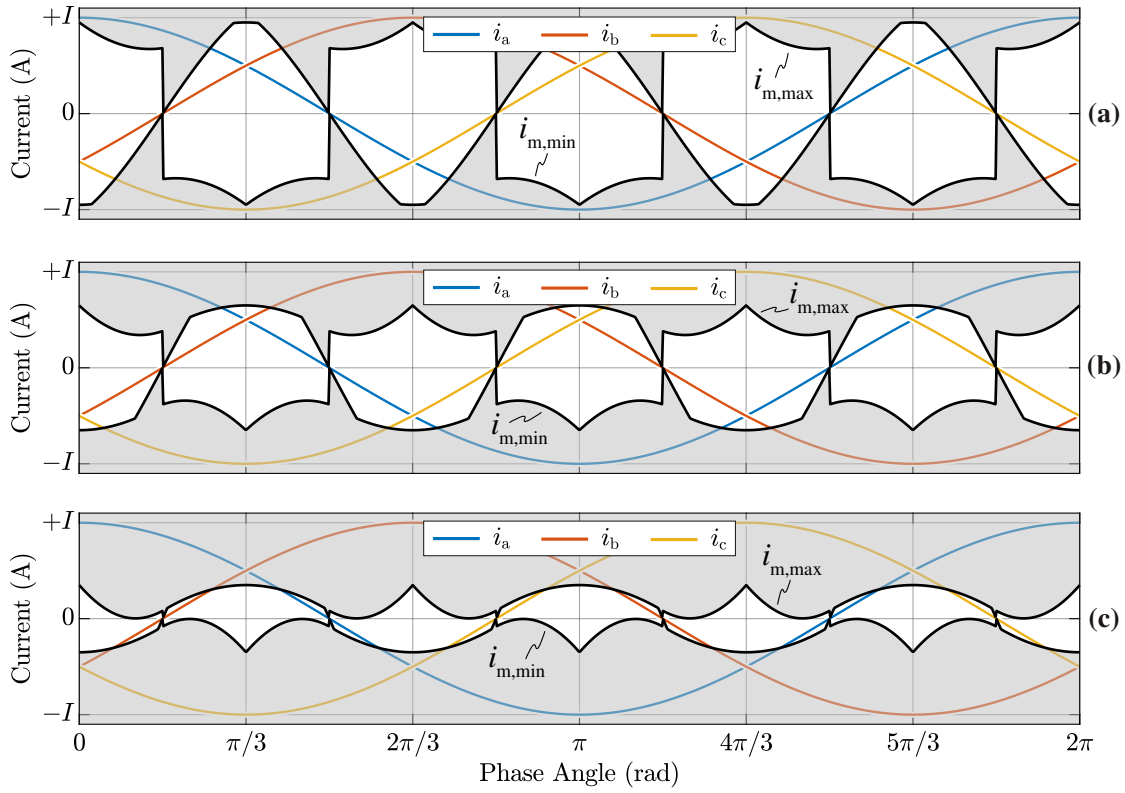


Fig. 2.6: Mid-point current local average limits $i_{m,max}$, $i_{m,min}$ for **(a)** $M = 0.7$, **(b)** $M = 0.9$, and **(c)** $M = 1.1$, assuming $\varphi = 0$ (unity power factor operation), i.e. $\text{sign}(i_x) = \text{sign}(v_x)$.

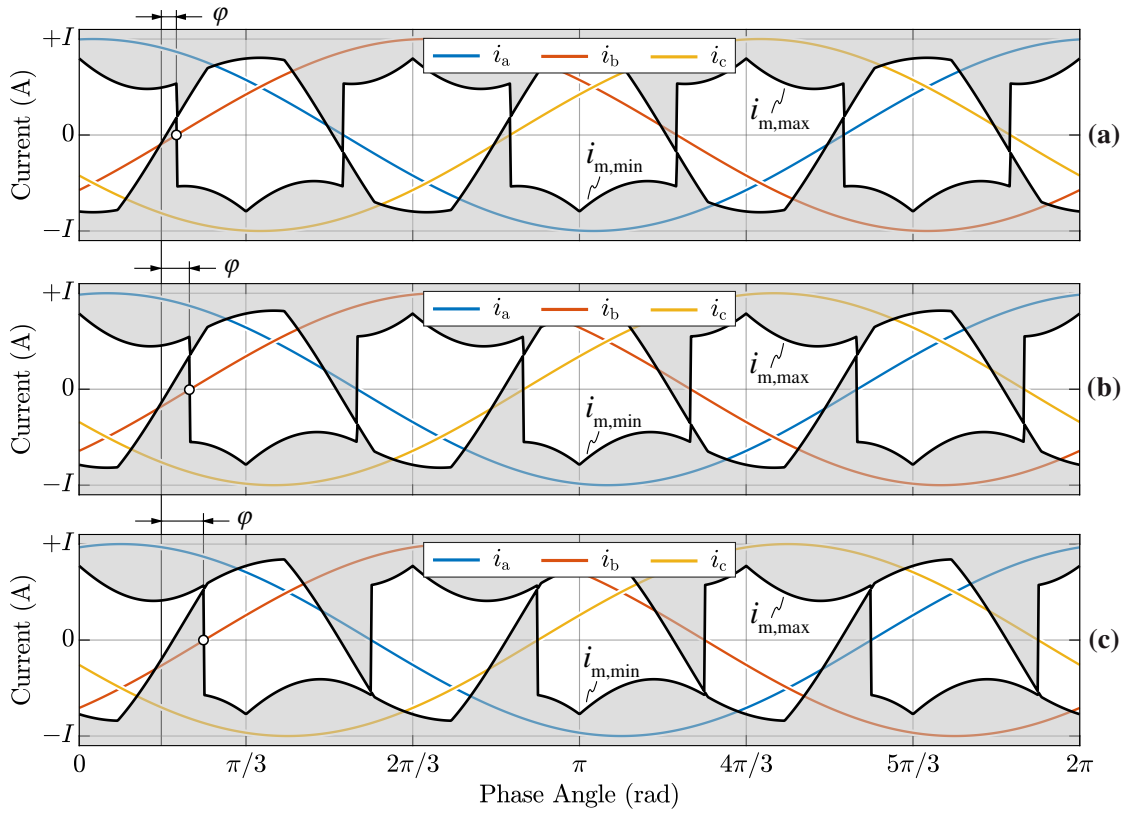


Fig. 2.7: Mid-point current local average limits $i_{m,max}$, $i_{m,min}$ for **(a)** $\varphi = 5°$, **(b)** $\varphi = 10°$, and **(c)** $\varphi = 15°$, assuming $M = 0.8$.

To ease the solution of (2.27), it is worth observing that $i_{m,max}$ within $0 \leq \vartheta \leq \pi/3$ is equal to $-i_{min}$ within $\pi/3 \leq \vartheta \leq 2\pi/3$ (cf. **Fig. 2.6**, **Fig. 2.7**). Therefore, the integration interval may be restricted to $\vartheta \in [0, \pi/3]$ by considering both maximum and minimum i_m envelopes. A highlight of the waveforms within the selected integration interval is provided in **Fig. 2.8**.

Leveraging the definition of $v_{o,min}$ and the signs of i_a, i_b, i_c within the considered averaging window, different $I_{m,max}$ expressions are obtained depending on the value of the modulation index. In particular, three main regions are identified, as illustrated in **Fig. 2.9**: region ① with $M < 1/\sqrt{3}$, region ② with $1/\sqrt{3} \leq M \leq 2/3$ (i.e., the transition region) and region ③ with $M > 2/3$. The current and voltage waveforms for regions ①, ② and ③ are reported in **Fig. 2.8(a)**, **(b)** and **(c)**, respectively.

The expressions of $I_{m,max}$ are therefore:

$$I_{m,max,①} = \frac{6}{\pi V_{dc}} \left[\int_0^{\pi/6+\varphi} i_a v_a \, d\vartheta - \int_{\pi/6+\varphi}^{\pi/3} i_c v_b \, d\vartheta - \int_0^{\pi/6+\varphi} i_a v_b \, d\vartheta + \int_{\pi/6+\varphi}^{\pi/3} i_c v_c \, d\vartheta \right], \quad (2.28)$$

valid for $M < 1/\sqrt{3}$,

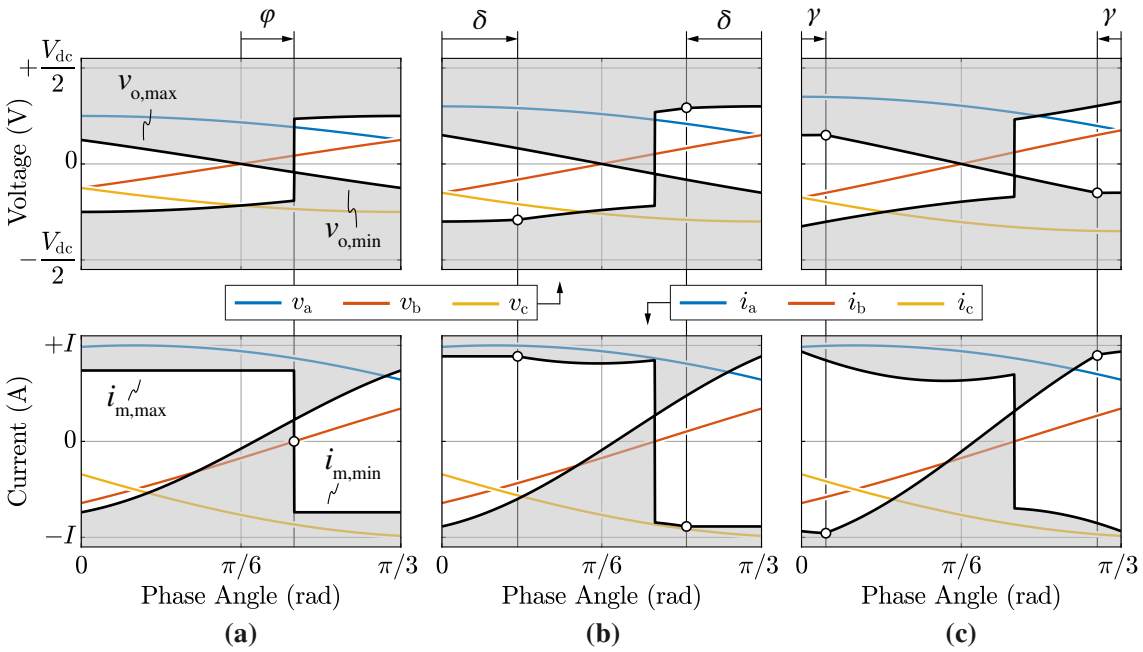


Fig. 2.8: Zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ and mid-point current local average limits $i_{m,max}$, $i_{m,min}$ for **(a)** $M = 0.5$ (region ①), **(b)** $M = 0.6$ (region ②), and **(c)** $M = 0.7$ (region ③), assuming $\varphi = 10°$. The focus is on $0 \leq \vartheta \leq \pi/3$ to highlight the most relevant angle definitions for the analytical calculations (i.e., φ, δ, γ).

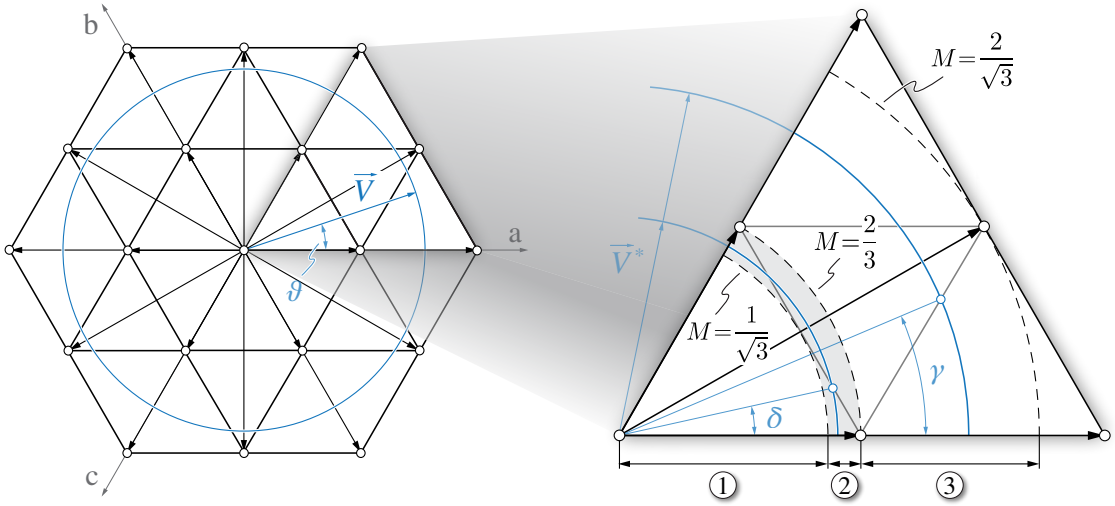


Fig. 2.9: Overview of the modulation index regions ①, ② and ③ on the space vector diagram, focusing on $0 \leq \vartheta \leq \pi/3$. The transition region ② is highlighted in grey and the most significant angle definitions for the analytical calculations are indicated (i.e., ϑ, δ, γ).

$$I_{\mathrm{m,max,}②} = \frac{6}{\pi V_{\mathrm{dc}}}\left[-\int_{0}^{\pi/6+\varphi} i_{\mathrm{a}}\, v_{\mathrm{b}}\, \mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3-\delta} i_{\mathrm{c}} \left(\frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{a}}\right) \mathrm{d}\vartheta + \int_{\pi/3-\delta}^{\pi/3} i_{\mathrm{c}}\, v_{\mathrm{c}}\, \mathrm{d}\vartheta + \right.$$
$$\left. + \int_{0}^{\delta} i_{\mathrm{a}}\, v_{\mathrm{a}}\, \mathrm{d}\vartheta + \int_{\delta}^{\pi/6+\varphi} i_{\mathrm{a}} \left(\frac{V_{\mathrm{dc}}}{2} + v_{\mathrm{c}}\right) \mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3} i_{\mathrm{c}}\, v_{\mathrm{b}}\, \mathrm{d}\vartheta \right], \quad (2.29)$$

valid for $1/\sqrt{3} \leq M \leq 2/3$, and

$$I_{\mathrm{m,max,}③} = \frac{6}{\pi V_{\mathrm{dc}}}\left[\int_{0}^{\pi/6+\varphi} i_{\mathrm{a}} \left(\frac{V_{\mathrm{dc}}}{2} + v_{\mathrm{c}}\right) \mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3-\gamma} i_{\mathrm{c}}\, v_{\mathrm{b}}\, \mathrm{d}\vartheta - \int_{\pi/3-\gamma}^{\pi/3} i_{\mathrm{c}} \left(\frac{V_{\mathrm{dc}}}{2} + v_{\mathrm{c}}\right) \mathrm{d}\vartheta + \right.$$
$$\left. + \int_{0}^{\gamma} i_{\mathrm{a}} \left(\frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{a}}\right) \mathrm{d}\vartheta - \int_{\gamma}^{\pi/6+\varphi} i_{\mathrm{a}}\, v_{\mathrm{b}}\, \mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3} i_{\mathrm{c}} \left(\frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{a}}\right) \mathrm{d}\vartheta \right], \quad (2.30)$$

valid for $M > 2/3$. The angles δ, γ are graphically illustrated in **Fig. 2.8** and **Fig. 2.9**, and their expression is obtained by setting $v_{\mathrm{a}} = v_{\mathrm{c}} + V_{\mathrm{dc}}/2$ and $v_{\mathrm{a}} - V_{\mathrm{dc}}/2 = v_{\mathrm{b}}$, respectively, as

$$\delta = \frac{\pi}{6} - \cos^{-1}\left(\frac{1}{\sqrt{3}M}\right) \qquad \frac{1}{\sqrt{3}} \leq M \leq \frac{2}{3}, \quad (2.31)$$

$$\gamma = \frac{\pi}{3} - \sin^{-1}\left(\frac{1}{\sqrt{3}M}\right) \qquad M \geq \frac{2}{3}. \quad (2.32)$$

Finally, substituting (2.4), (2.6), (2.31), (2.32) into (2.28)–(2.30) and solving the integral terms, the following analytical expressions are obtained:

$$I_{\mathrm{m,max,}①} = \frac{3}{\pi} I \frac{M}{4} \cos\varphi \left(\pi + \sqrt{3} - 2\sqrt{3}\,\varphi \tan\varphi\right) \quad (2.33)$$

valid for $M < 1/\sqrt{3}$ and

$$I_{\mathrm{m,max,}②} = I_{\mathrm{m,max,}③} = \frac{3}{\pi} I \left[1 + \frac{1}{2M} \cos\varphi \left(\sqrt{3M^2 - 1} - \frac{1}{\sqrt{3}}\right) + \right.$$
$$\left. + \frac{M}{2} \cos\varphi \left(3 \sin^{-1}\left(\frac{1}{\sqrt{3}M}\right) - \pi - \frac{\sqrt{3}}{2} - 2\sqrt{3}\,\varphi \tan\varphi\right)\right] \quad (2.34)$$

valid for $M > 1/\sqrt{3}$, which is the typical rectifier operating range. Expressions (2.33) and (2.34) are graphically illustrated in **Fig. 2.10**, where the modulation index regions ①, ② and ③ are also indicated.

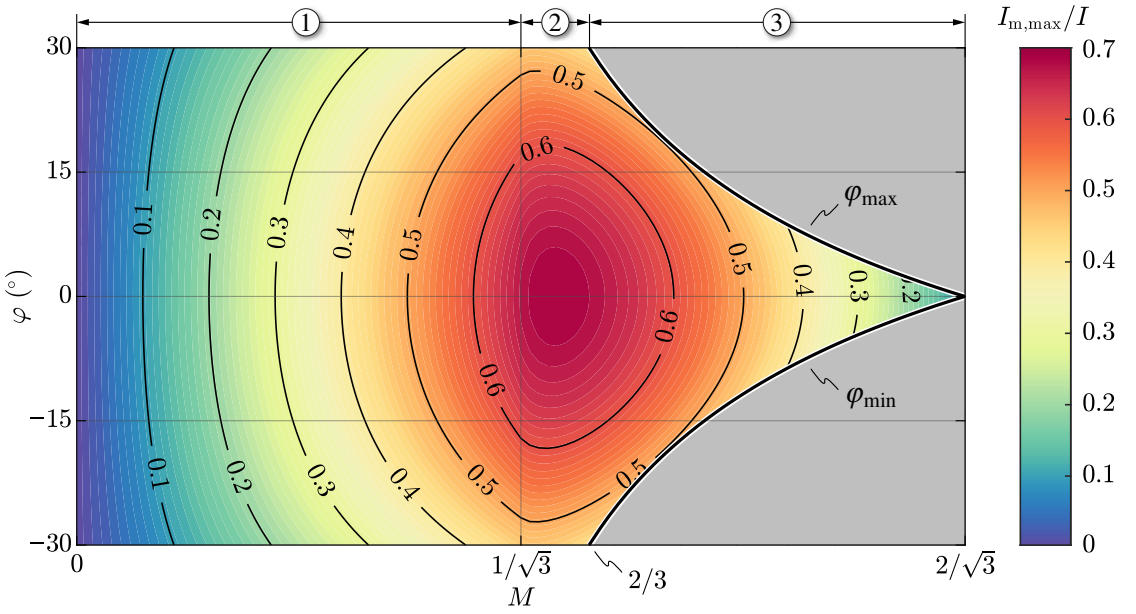


Fig. 2.10: Maximum mid-point current periodical average $I_{\mathrm{m,max}} = -I_{\mathrm{m,min}}$ (i.e., normalized with respect to the peak phase current I) as function of the modulation index M and the power factor angle φ. The three modulation index regions ①, ② and ③ are indicated (cf. **Fig. 2.9**).

2.3 Modulation Strategies

It is well known that the injection of a zero-sequence (i.e., common-mode) voltage component v_{o} represents a degree of freedom in the input voltage formation process of all three-phase converters, leading to different PWM strategies [57, 62–66]. Although the zero-sequence voltage injection does not modify the local average of the generated phase voltages (cf. **Section 2.2.1**), it allows to extend the feasible modulation range of the converter (i.e., from $M = 1$ up to $M = 2/\sqrt{3}$) and it affects both the active and passive converter component stresses, namely the semiconductor losses, the AC-side inductor flux/current ripple and the DC-link charge/voltage ripple. In particular, three-level rectifiers may witness a DC-link mid-point voltage oscillation at three times the grid frequency [56, 57, 67, 68], which strongly depends on the adopted modulation strategy. This low-frequency voltage oscillation can represent a notable issue in EV charging applications, as the DC/DC converter stage may not be able to reject it (cf. **Chapter 7**), leading to unacceptably large current ripple flowing into the battery.

This section introduces the most adopted modulation strategies for unidirectional three-phase three-level rectifiers.

2.3.1 Modulator

The pulse-width modulator of three-level rectifiers may be implemented either with carrier-based (CB) or space-vector (SV) approaches [63, 64, 66]. While SVPWM generates the switch duty cycles by leveraging geometrical relationships within the space vector hexagon (cf. **Fig. 2.3**), CBPWM is based on adding a suitable zero-sequence component to the normalized phase voltage references. Although SVPWM strategies may be more straightforward to analyze and modify, they are characterized by higher levels of complexity and computational burden [66]. Therefore, a certain effort has been historically spent in converting SVPWM strategies into CBPWM, exploiting the relationship between redundant space vector allocation (SV approach) and zero-sequence injection level (CB approach) [57, 62–66]. For the aforementioned reasons, a carrier-based modulator is considered in this work.

The 4Q mid-point switch signals s_a, s_b, s_c are obtained by comparing the modulation references

$$m_\mathrm{x} = \frac{v_\mathrm{xm}}{V_\mathrm{dc}/2} = \frac{v_\mathrm{x}}{V_\mathrm{dc}/2} + \frac{v_\mathrm{o}}{V_\mathrm{dc}/2} \qquad \mathrm{x} = \mathrm{a, b, c,} \tag{2.35}$$

i.e.,

$$\begin{cases} m_\mathrm{a} = M\cos(\vartheta) + m_\mathrm{o} \\ m_\mathrm{b} = M\cos(\vartheta + \frac{2\pi}{3}) + m_\mathrm{o} \\ m_\mathrm{c} = M\cos(\vartheta + \frac{4\pi}{3}) + m_\mathrm{o} \end{cases} \tag{2.36}$$

with two vertically shifted PWM carriers, as illustrated in **Fig. 2.11**. In particular, $s_\mathrm{x} = 1$ (i.e., 4Q mid-point switch in the ON-state) when m_x stands between the two carriers, whereas $s_\mathrm{x} = 0$ (i.e., 4Q mid-point switch in the OFF-state) when m_x is either higher than the positive carrier or lower than the negative carrier. Notably, $m_\mathrm{o} = 2v_\mathrm{o}/V_\mathrm{dc}$ is the zero-sequence modulation reference, which contains the information related to the adopted modulation strategy.

2.3.2 Zero-Sequence Voltage Injection

The zero-sequence voltage v_o can be expressed as the sum of two contributions with different purposes: a periodic component $v_{\mathrm{o},3}$ with three-times the grid frequency (i.e., a periodicity of $2\pi/3$), representative of the selected modulation strategy, and a DC component $V_{\mathrm{o},\delta}$ reserved for control purposes (i.e., $V_{\mathrm{o},\delta} \neq 0$ only in dynamical conditions and/or under unbalanced split DC-link loading, cf. **Chapter 4**). The most adopted modulation strategies

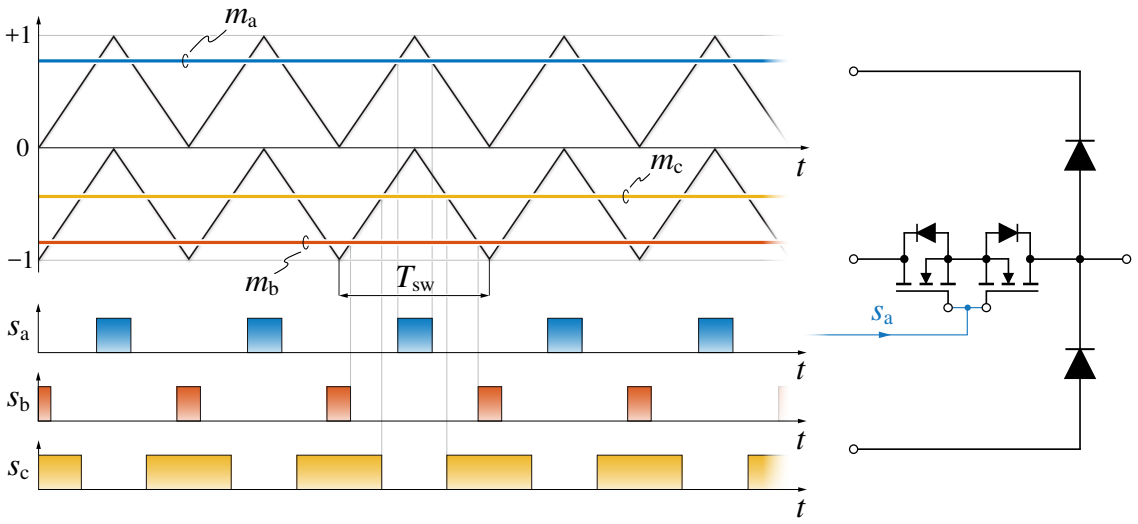


Fig. 2.11: Schematic overview of the carrier-based pulse-width modulator of the considered unidirectional three-phase three-level rectifier. The 4Q switch signals s_a, s_b, s_c are generated by comparing m_a, m_b, m_c with two vertically shifted PWM carriers.

for unidirectional three-phase three-level rectifiers are described in the following and the related expressions of $v_{o,3}$ are reported. The local average values of bridge-leg voltages v_{xm}, reference phase voltages v_x and zero-sequence voltage $v_{o,3}$ are graphically illustrated in **Fig. 2.12** for all selected modulation strategies.

Sinusoidal Modulation (SPWM)

SPWM does not inject a periodic zero-sequence component, thus resulting in the simplest modulation strategy:

$$v_{o,3} = 0. \tag{2.37}$$

However, (2.37) cannot be ensured over the complete period when $M > 1$, as the zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ cross the line defined by $v_o = 0$ (cf. **Fig. 2.4**). Therefore, SPWM does not extend the feasible modulation index region of the rectifier.

Third Harmonic Injection Modulation (THIPWM)

THIPWM injects a sinusoidal third harmonic with an amplitude equal to one-sixth of the phase voltage reference, resulting in

$$v_{o,3} = -\frac{1}{6}\frac{V_{dc}}{2} M \cos(3\vartheta). \tag{2.38}$$

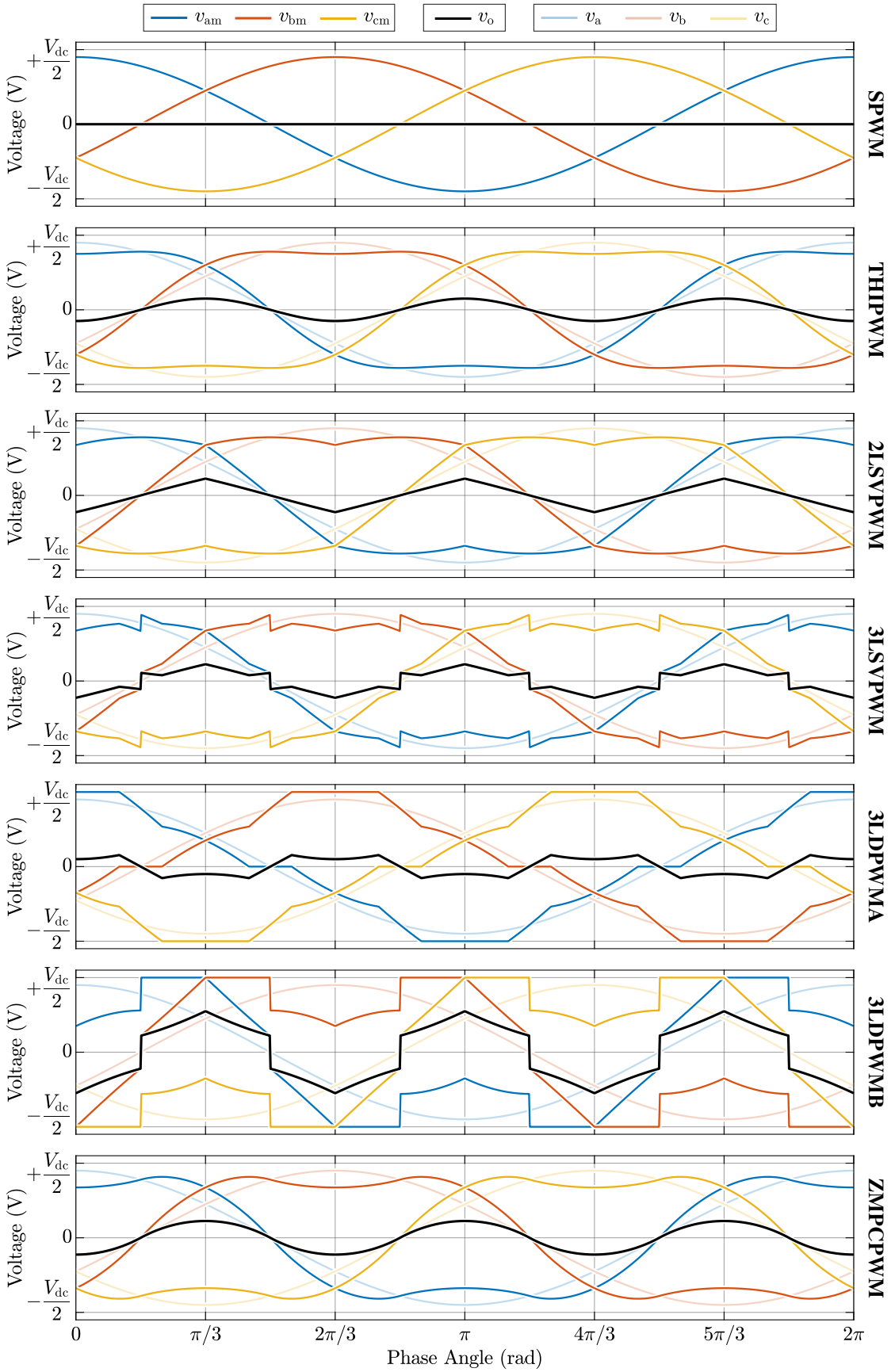


Fig. 2.12: Bridge-leg voltages v_{xm}, reference phase voltages v_x and zero-sequence voltage $v_{o,3}$ over a grid period for all modulation strategies assuming $M = 0.9$ and $\varphi = 0$.

Two-Level Space Vector Modulation (2LSVPWM)

2LSVPWM injects the same zero-sequence voltage component as a conventional two-level inverter modulated with SVPWM [62–64], namely subtracting to all phases the average of the maximum and minimum envelopes of the reference phase voltages as

$$v_{o,3} = -\frac{1}{2}\left(v_{max} + v_{min}\right), \tag{2.39}$$

where $v_{max} = \max\left[v_a, v_b, v_c\right]$ and $v_{min} = \min\left[v_a, v_b, v_c\right]$.

Three-Level Space Vector Modulation (3LSVPWM)

Similarly to 2LSVPWM, 3LSVPWM injects the same zero-sequence voltage as a three-level rectifier modulated with SVPWM [57, 66, 69], i.e. the average of the maximum and minimum zero-sequence voltage limits, as

$$v_{o,3} = \frac{1}{2}\left(v_{o,max} + v_{o,min}\right). \tag{2.40}$$

The injected zero-sequence voltage is thus always centered between $v_{o,max}$ and $v_{o,min}$.

Three-Level Discontinuous Modulation A (3LDPWMA)

Discontinuous modulation strategies, in essence, clamp each converter bridge-leg to either the high-side, the mid-point or the low-side DC-link rails for a certain time interval (i.e., a fraction of the grid period), generating discontinuous switching. This property allows either to reduce the converter switching losses or to increase the converter switching frequency at constant overall loss.

The first discontinuous modulation strategy for unidirectional three-phase three-level rectifiers is 3LDPWMA [65, 70, 71], which injects a zero-sequence voltage equal to

$$v_{o,3} = \frac{1}{2}\left(v_{o,max} + v_{o,min}\right) - \frac{1}{2}\,\mathrm{sign}\left(|v_{o,max}| - |v_{o,min}|\right)\left(v_{o,max} - v_{o,min}\right). \tag{2.41}$$

Notably, assuming unity power factor operation (i.e., $\varphi = 0$) and $M > 2/3$ (i.e., region ③, typical for grid-connected rectifiers), the clamping intervals of 3LDPWMA are located partly around phase current zero-crossings and partly around phase current peaks. Furthermore, the clamping intervals have a variable width depending on the value of M, therefore the switching loss reduction (or allowable switching frequency increase) is modulation

index dependent. In particular, increasing the value of M, the clamping interval centered around the current peak widens and the total switching losses decrease.

Three-Level Discontinuous Modulation B (3LDPWMB)

The second discontinuous modulation strategy for unidirectional three-phase three-level rectifiers is 3LDPWMB [65, 70], which injects a zero-sequence voltage equal to

$$v_{o,3} = \frac{1}{2}\left(v_{o,max} + v_{o,min}\right) + \frac{1}{2}\,\mathrm{sign}\left(|v_{o,max}| - |v_{o,min}|\right)\left(v_{o,max} - v_{o,min}\right). \tag{2.42}$$

As opposed to 3LDPWMA, the clamping intervals of 3LDPWMB have constant width (i.e., equal to $\pi/3$, for $M > 2/3$), therefore the switching loss reduction (or allowable switching frequency increase) is unaffected by the modulation index in region ③.

Zero Mid-Point Current Modulation (ZMPCPWM)

ZMPCPWM allows to achieve a zero mid-point current local average over the complete grid period when operating with unity power factor (i.e., $\varphi = 0$) [57, 60, 61, 72]. The expression of the zero-sequence voltage can be directly obtained by setting $i_m = 0$ and $v_o = v_{o,3}$ into (2.17) and rearranging it as

$$v_{o,3} = \frac{\sum\limits_{x=a,b,c} v_x\,|i_x|}{\sum\limits_{x=a,b,c} |i_x|} = \frac{v_a\,|i_a| + v_b\,|i_b| + v_c\,|i_c|}{|i_a| + |i_b| + |i_c|}. \tag{2.43}$$

Despite the complexity of (2.43), a fairly accurate approximation is obtained with [57]

$$v_{o,3} \approx -\frac{1}{4}\,\frac{V_{dc}}{2}\,M\cos\left(3\vartheta\right), \tag{2.44}$$

showing that this strategy may also be implemented in digital environment with low computational effort.

It is worth noting that (2.43) cannot be ensured over the complete period either for high values of modulation index (i.e., $M > 1.1$) or for non-unity power factor operation (i.e., $\varphi \neq 0$). At $M \approx 1.1$, in fact, $v_{o,3}$ hits the zero-sequence voltage limits and its value must be clamped to either $v_{o,max}$ or $v_{o,min}$, no longer ensuring a zero mid-point current local average. Moreover, when $\varphi \neq 0$, $i_{m,max}$ and $i_{m,min}$ cross the line defined by $i_m = 0$ (cf. **Fig. 2.7**), therefore the mid-point current local average cannot be set to zero along the complete grid period. Nonetheless, the present application must operate at unity power

factor (i.e., $\varphi = 0$) or in its vicinity, and the operating modulation index is limited between $M \approx 0.81$ (i.e., $V_{\mathrm{dc}} = 800\,\mathrm{V}$) and $M \approx 1$ (i.e., $V_{\mathrm{dc}} = 650\,\mathrm{V}$), always ensuring a mid-point current local average close to zero.

Since the minimization of the DC-link mid-point voltage oscillation is of primary importance in EV charging applications, ZMPCPWM is considered in the following as the reference modulation strategy for the design, the control and the experimental assessment of the rectifier (cf. **Chapter 3**, **Chapter 4**).

2.3.3 Zero-Sequence Voltage Saturation

To ensure that only feasible bridge-leg voltage references are passed to the modulator, the zero-sequence voltage limits (2.22) must always be enforced within the rectifier control structure by means of a saturation action (cf. **Chapter 4**), namely

$$\begin{cases} v_{\mathrm{o}} = v_{\mathrm{o,max}} & v_{\mathrm{o}} > v_{\mathrm{o,max}} \\ v_{\mathrm{o}} = v_{\mathrm{o,min}} & v_{\mathrm{o}} < v_{\mathrm{o,min}} \end{cases} . \tag{2.45}$$

This saturation process is in fact necessary to avoid large and uncontrolled phase current distortion [61, 66, 73–78], which arises when the desired zero-sequence voltage (i.e., $v_{\mathrm{o}} = v_{\mathrm{o,3}} + V_{\mathrm{o},\delta}$) exceeds either $v_{\mathrm{o,max}}$ or $v_{\mathrm{o,min}}$ if no saturation is in place (cf. **Section 4.5**).

While the saturation action always ensures the feasibility of the bridge-leg voltage references, this process can modify the periodic zero-sequence voltage injection defined by the adopted modulation strategy for certain values of M (i.e., $M > 1$ for SPWM, $M > 1.1$ for ZMPCPWM) and for $\varphi \neq 0$, as the desired $v_{\mathrm{o,3}}$ exceeds either $v_{\mathrm{o,max}}$ or $v_{\mathrm{o,min}}$. Therefore, when active, the zero-sequence voltage saturation also affects the stresses on the active and passive converter components.

2.4 Component Stresses

The current and voltage stresses on the main active and passive converter components have a direct impact on the converter design (cf. **Chapter 3**). In this section, all relevant component stresses are evaluated analytically (i.e., providing easy-to-use expressions) or numerically as functions of the operating point (i.e., M, φ), highlighting the impact of the adopted modulation strategy.

The performed analysis is based on the following simplifying assumptions:

- high switching-to-fundamental frequency ratio (i.e., $f_{\mathrm{sw}}/f > 200 = 10\,\mathrm{kHz}$);
- sinusoidal AC-side currents (i.e., the current ripple is neglected);
- constant DC-link voltage (i.e., the voltage ripple is neglected);
- discontinuous conduction mode around the current zero-crossings is disregarded.

These assumptions allow to derive analytical component stress expressions that very well approximate the real behavior of the system and are independent of the specific application (e.g., the power level) [57].

2.4.1 Semiconductor Devices

Each T-type rectifier bridge-leg consists of two diodes and two MOSFETs connected in anti-series (i.e., to form the mid-point 4Q switch, cf. **Fig. 2.1(d)**). In this converter topology, the diodes must be able to withstand the full DC-link voltage V_{dc}, whereas the MOSFETs must only be able to block half of the DC-link voltage $V_{\mathrm{dc}}/2$. Considering the maximum DC-link voltage set by the application (i.e., $V_{\mathrm{dc,max}} = 800\,\mathrm{V}$) and taking into account a typical overvoltage safety margin of 50 % (i.e., to ensure that the semiconductor safe-operating-area is not exceeded during switching events), 1200 V diodes and 600 V/650 V MOSFETs must be employed.

The current flowing through each semiconductor devices defines its conduction and switching losses and thus also determines the heat dissipation requirements. In general, both average (AVG) and root-mean-square (RMS) current stresses of all semiconductor devices are of interest, and they depend on the modulation index M, the power factor angle φ and the modulation strategy. Nevertheless, since $\varphi \neq 0$ causes the zero-sequence voltage saturation process to modify $v_{\mathrm{o,3}}$ (cf. **Section 2.3.3**), $\varphi = 0$ is considered in the following, with the goal of achieving simple and compact analytical expressions of the current stresses. Therefore, assuming ZMPCPWM (i.e., with the simplified expression in (2.44)) and unity power factor operation (i.e., $\varphi = 0$), the transistor (T) and diode (D) current stresses are derived:

$$I_{\mathrm{T,AVG}} \approx I\left(\frac{2}{\pi} - \frac{M}{2}\right), \qquad I_{\mathrm{T,RMS}} \approx I\sqrt{\frac{1}{2} - \frac{19M}{15\pi}}, \tag{2.46}$$

$$I_{\mathrm{D,AVG}} \approx I\frac{M}{4}, \qquad I_{\mathrm{D,RMS}} \approx I\sqrt{\frac{19M}{30\pi}}. \tag{2.47}$$

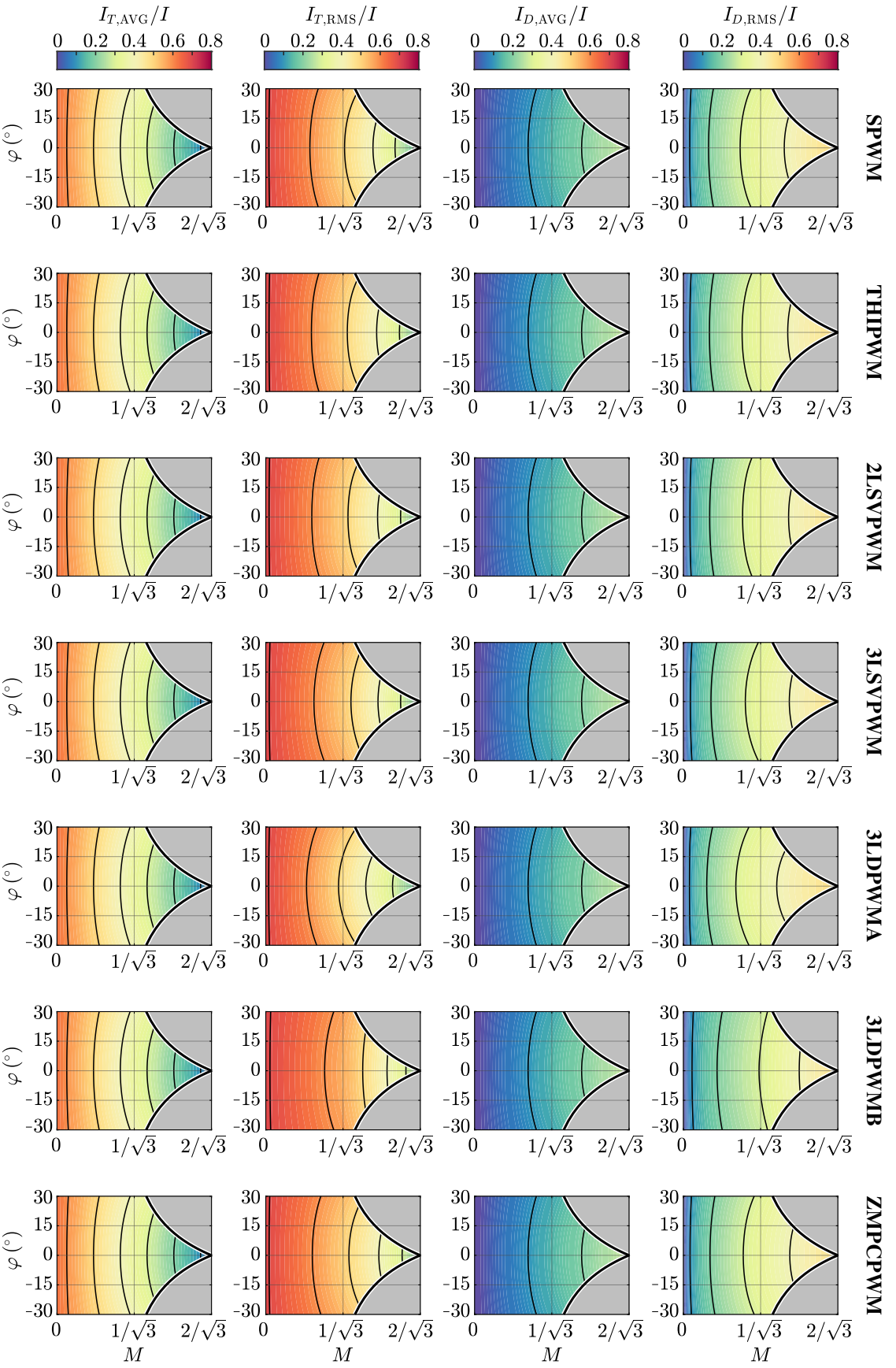


Fig. 2.13: Average and RMS current stresses on each transistor (i.e., $I_{\mathrm{T,AVG}}$, $I_{\mathrm{T,RMS}}$) and diode (i.e., $I_{\mathrm{D,AVG}}$, $I_{\mathrm{D,RMS}}$) as functions of M and φ for all modulation strategies.

Similar expressions can be obtained for each modulation strategy. For completeness, **Fig. 2.13** shows the values of $I_{\mathrm{T,AVG}}$, $I_{\mathrm{T,RMS}}$, $I_{\mathrm{D,AVG}}$ and $I_{\mathrm{D,RMS}}$ normalized with respect to the peak phase current I as functions of M and φ for all modulation strategies. Since for some values of M and φ the $v_{\mathrm{o,max}}$ and $v_{\mathrm{o,min}}$ limits are encountered (i.e., the zero-sequence voltage saturation becomes active), the stresses reported in **Fig. 2.13** are calculated numerically. It is primarily observed that while the RMS current stresses are slightly affected by the zero-sequence voltage injection, the average current stresses are totally independent of the modulation strategy.

Conduction Losses

The average conduction losses of each semiconductor device can be estimated leveraging its conduction characteristics $v(i, T_{\mathrm{j}})$ provided in the manufacturer datasheet, the instantaneous bridge-leg current i (sinusoidal, neglecting the switching ripple), the device duty-cycle d (i.e., relative ON-time, dependent on the modulation index and the modulation strategy), and the instantaneous semiconductor junction temperature T_{j}, as

$$P_{\mathrm{cond}} = \frac{1}{2\pi} \int_0^{2\pi} d\, v(i, T_{\mathrm{j}})\, i \, \mathrm{d}\vartheta. \tag{2.48}$$

It is worth noting that approximate expressions of the conduction losses can be obtained by considering simplified conduction characteristics (cf. **Fig. 2.14(a)**) for both the MOSFETs (i.e., unipolar devices with on-state resistance R_{T}) and the diodes (i.e., bipolar devices with on-state threshold voltage V_{D} and differential resistance R_{D}), as

$$v_{\mathrm{T}} \approx R_{\mathrm{T}}\, i_{\mathrm{T}}, \qquad v_{\mathrm{D}} \approx V_{\mathrm{D}} + R_{\mathrm{D}}\, i_{\mathrm{D}}, \tag{2.49}$$

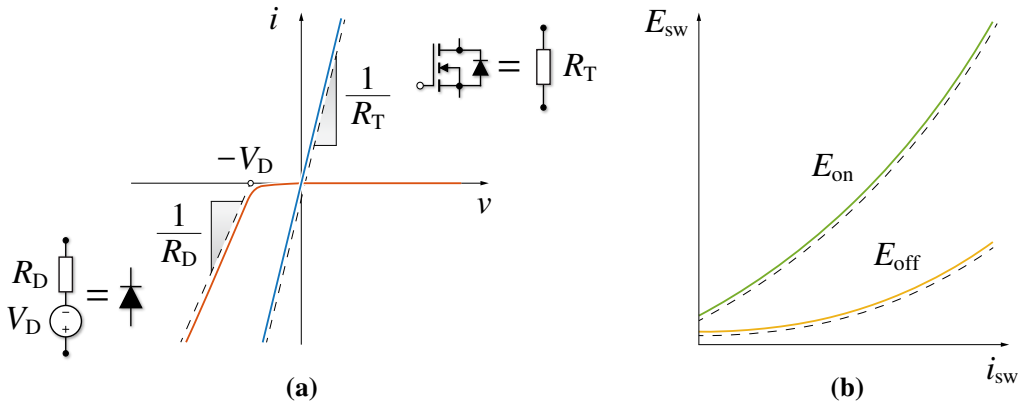


Fig. 2.14: Simplified **(a)** forward and reverse conduction characteristics of the MOSFET ($v_{\mathrm{T}} = R_{\mathrm{T}}\, i$) and the diode ($v_{\mathrm{D}} = V_{\mathrm{D}} + R_{\mathrm{D}}\, i$) and **(b)** switching energies dissipated during the turn-on transition, i.e. $E_{\mathrm{on}} = V_{\mathrm{sw}}\,(k_{0,\mathrm{on}} + k_{1,\mathrm{on}}\, i_{\mathrm{sw}} + k_{2,\mathrm{on}}\, i_{\mathrm{sw}}^2)$, and the turn-off transition, i.e. $E_{\mathrm{off}} = V_{\mathrm{sw}}\,(k_{0,\mathrm{off}} + k_{1,\mathrm{off}}\, i_{\mathrm{sw}} + k_{2,\mathrm{off}}\, i_{\mathrm{sw}}^2)$.

where R_T, R_D and V_D are temperature dependent. Substituting (2.49) into (2.48) and considering the average and RMS current stresses derived in (2.46)–(2.47), the following simplified conduction loss expressions are obtained for ZMPCPWM and $\varphi = 0$:

$$P_{\text{cond,T}} \approx R_T I_{\text{T,RMS}}^2 \approx R_T I^2 \left(\frac{1}{2} - \frac{19M}{15\pi} \right), \tag{2.50}$$

$$P_{\text{cond,D}} \approx V_D I_{\text{D,AVG}} + R_D I_{\text{D,RMS}}^2 \approx V_D I \frac{M}{4} + R_D I^2 \frac{19M}{30\pi}. \tag{2.51}$$

Similar expressions can be derived for all modulation strategies.

Therefore, the total converter conduction losses are obtained as the sum of all transistor and diode losses, i.e.

$$P_{\text{cond,tot}} = 3 \left(2P_{\text{cond,T}} + 2P_{\text{cond,D}} \right). \tag{2.52}$$

Switching Losses

The switching losses of a bridge-leg operated with a continuous modulation strategy (i.e., SPWM, THIPWM, 2LSVPWM, 3LSVPWM, ZMPCPWM) are estimated with the following relation:

$$P_{\text{sw}} = \frac{f_{\text{sw}}}{2\pi} \int_0^{2\pi} \left[E_{\text{on}}(i_{\text{sw}}, V_{\text{sw}}) + E_{\text{off}}(i_{\text{sw}}, V_{\text{sw}}) \right] \mathrm{d}\vartheta, \tag{2.53}$$

where i_{sw} is the switched current, $V_{\text{sw}} = V_{\text{dc}}/2$ is the switched voltage and E_{on}, E_{off} are the turn-on and turn-off switching energies, respectively. It is worth noting that E_{on} includes the reverse-recovery energy of the bridge diode involved in the commutation.

Similarly to conduction losses, approximate expressions of the switching losses can be derived by considering simplified switching energy characteristics (cf. **Fig. 2.14(b)**). The considered loss model is linear with respect to the switched voltage V_{sw} and quadratic with respect to the switched current i_{sw}, namely

$$E_{\text{on}} \approx V_{\text{sw}} \left(k_{0,\text{on}} + k_{1,\text{on}} i_{\text{sw}} + k_{2,\text{on}} i_{\text{sw}}^2 \right), \tag{2.54}$$

$$E_{\text{off}} \approx V_{\text{sw}} \left(k_{0,\text{off}} + k_{1,\text{off}} i_{\text{sw}} + k_{2,\text{off}} i_{\text{sw}}^2 \right), \tag{2.55}$$

where $k_{0,\text{on/off}}$, $k_{1,\text{on/off}}$ and $k_{2,\text{on/off}}$ are suitable parameters that best fit the real switching energy characteristics. Notably, since the 4Q switch consists of two anti-series MOSFETs, the bridge-leg switching losses are independent of the current direction (i.e., $i_{\text{sw}} = |i_{\text{x}}|$, where i_{x} is the phase current neglecting the switching ripple). Therefore, substituting (2.54)

and (2.55) into (2.53), the switching losses of a bridge-leg operated with a continuous modulation strategy can be expressed as

$$P_{\mathrm{sw}} \approx f_{\mathrm{sw}} V_{\mathrm{sw}} \left[\left(k_{0,\mathrm{on}} + k_{0,\mathrm{off}}\right) + \frac{2}{\pi} I \left(k_{1,\mathrm{on}} + k_{1,\mathrm{off}}\right) + \frac{1}{2} I^2 \left(k_{2,\mathrm{on}} + k_{2,\mathrm{off}}\right) \right]. \tag{2.56}$$

If a discontinuous modulation strategy (i.e., 3LDPWMA, 3LDPWMB) is considered, the clamping intervals must be omitted from the integral in (2.53). Assuming $M > 2/3$, this leads to

$$P_{\mathrm{sw}} \approx f_{\mathrm{sw}} V_{\mathrm{sw}} \left[\frac{2}{3} \left(k_{0,\mathrm{on}} + k_{0,\mathrm{off}}\right) + \frac{2}{\sqrt{3}\pi M} I \left(k_{1,\mathrm{on}} + k_{1,\mathrm{off}}\right) + \frac{(2\pi - 3\sqrt{3})M^2 + 2\sqrt{3}}{6\pi M^2} I^2 \left(k_{2,\mathrm{on}} + k_{2,\mathrm{off}}\right) \right] \tag{2.57}$$

for 3LDPWMA and

$$P_{\mathrm{sw}} \approx f_{\mathrm{sw}} V_{\mathrm{sw}} \left[\frac{2}{3} \left(k_{0,\mathrm{on}} + k_{0,\mathrm{off}}\right) + \frac{3 - \sqrt{3}}{\pi} I \left(k_{1,\mathrm{on}} + k_{1,\mathrm{off}}\right) + \frac{1}{3} I^2 \left(k_{2,\mathrm{on}} + k_{2,\mathrm{off}}\right) \right] \tag{2.58}$$

for 3LDPWMB. It is worth noting that, when adopting 3LDPWMA, the switching losses depend on the modulation index, as the clamping intervals shift with M (i.e., not the case for 3LDPWMB). To give a sense of the switching loss reduction obtained with discontinuous modulation strategies, one can assume in first approximation a switching loss model linear with the switched current (i.e., $k_{0,\mathrm{on}} = k_{0,\mathrm{off}} \approx 0$, $k_{2,\mathrm{on}} = k_{2,\mathrm{off}} \approx 0$), as in [65, 70]. By doing so, the following switching loss ratios are obtained:

$$\frac{P_{\mathrm{sw,3LDPWMA}}}{P_{\mathrm{sw,CPWM}}} \approx \frac{1}{\sqrt{3}M} \approx \frac{0.58}{M}, \qquad \frac{P_{\mathrm{sw,3LDPWMB}}}{P_{\mathrm{sw,CPWM}}} \approx \frac{3 - \sqrt{3}}{2} \approx 0.63, \tag{2.59}$$

where subscript CPWM refers to continuous modulation (i.e., SPWM, THIPWM, 2LSVPWM, 3LSVPWM, ZMPCPWM). Remarkably, at maximum modulation index (i.e., $M = 2/\sqrt{3}$), 3LDPWMA achieves a 50 % loss reduction with respect to CBPWM.

In conclusion, the total converter switching losses are obtained by adding together the switching losses of the three bridge-legs, as

$$P_{\mathrm{sw,tot}} = 3\, P_{\mathrm{sw}}. \tag{2.60}$$

2.4.2 DC-Link Capacitors

The three-level T-Type rectifier features a split DC-link capacitor that must simultaneously satisfy two main design criteria. First, it must comply with the maximum RMS current stress defined by the application, which generates losses and affects the capacitor temperature rise. Moreover, it must ensure a predefined maximum peak-to-peak voltage ripple for both V_{pm} and V_{mn}, as the ripple increases the peak voltage applied to the semiconductor devices, alters the ideal operation of the converter (i.e., the AC-side applied voltages) and may lead to unacceptable low-frequency current ripple at the battery side (i.e., if the DC/DC stage is not able to reject it). Disregarding the AC-side switching frequency current ripple, both stresses can be analytically derived.

RMS Current

For reasons of symmetry, the RMS current flowing into each DC-link capacitor in balanced load conditions is the same. Therefore, focusing on the upper half of the DC-link and leveraging the DC-side current periodicity of $\pi/3$ (i.e., one sector), the following global average and global RMS expressions of the DC-link upper-rail current i_{p} (cf. **Fig. 2.2**) are obtained:

$$I_{\mathrm{p,AVG}} = \frac{3}{\pi}\int_{0}^{\pi/3} i_{\mathrm{p,AVG}}\,\mathrm{d}\vartheta = \frac{3}{4}MI\cos\varphi, \tag{2.61}$$

$$I_{\mathrm{p,RMS}}^{2} = \frac{3}{\pi}\int_{0}^{\pi/3} i_{\mathrm{p,RMS}}^{2}\,\mathrm{d}\vartheta = \frac{\sqrt{3}}{4\pi}MI^{2}(4\cos^{2}\varphi+1), \tag{2.62}$$

where $i_{\mathrm{p,AVG}}$ and $i_{\mathrm{p,RMS}}$ are the local average and local RMS values of i_{p}, respectively. Therefore, the DC-link capacitor RMS current can be calculated by difference, as

$$I_{\mathrm{C_{dc},RMS}}^{2} = I_{\mathrm{p,RMS}}^{2} - I_{\mathrm{p,AVG}}^{2}, \tag{2.63}$$

resulting in the same DC-link capacitor RMS current stress as for conventional two-level and three-level inverters [79, 80], i.e.

$$I_{\mathrm{C_{dc},RMS}} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi}+\cos^{2}\varphi\left(\frac{\sqrt{3}}{\pi}-\frac{9}{16}M\right)\right]}. \tag{2.64}$$

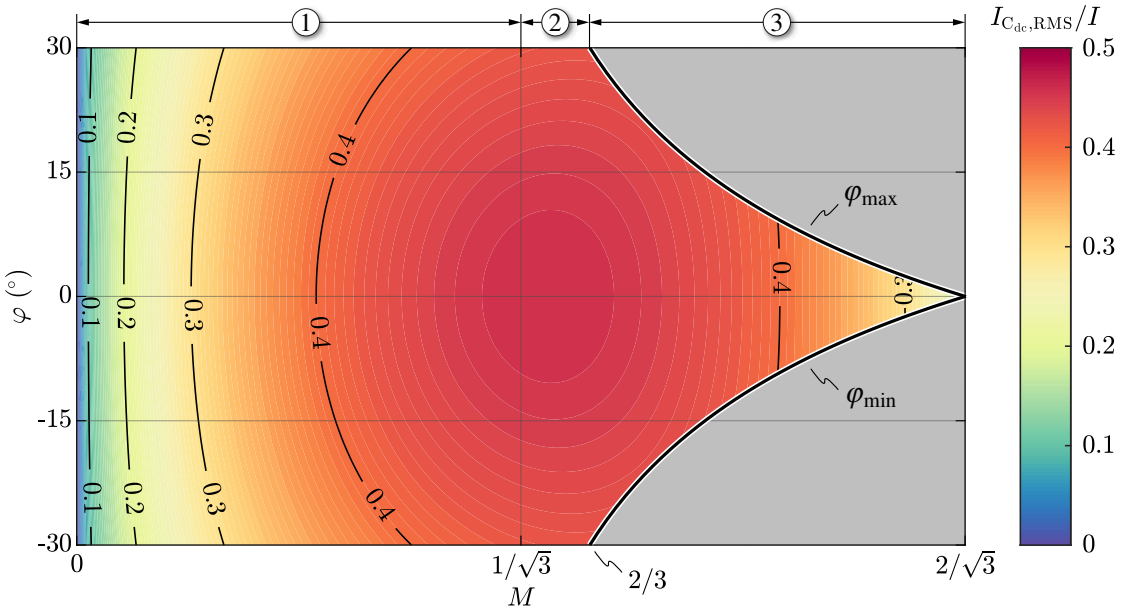


Fig. 2.15: DC-link RMS current $I_{C_{dc},RMS}$ (i.e., normalized with respect to the peak phase current I) as function of the modulation index M and the power factor angle φ. The three modulation index regions ①, ② and ③ are indicated (cf. **Fig. 2.9**).

Remarkably, (2.64) does not depend on the adopted modulation strategy, since it is not affected by the zero-sequence voltage injection. $I_{C_{dc},RMS}$ is illustrated in normalized form (i.e., divided by the peak phase current I) in **Fig. 2.15** as function of M and φ. The worst-case value of (2.64) is found for $\varphi = 0$ and $M = {}^{10\sqrt{3}}/_{9\pi} \approx 0.61$, obtaining

$$I_{C_{dc},RMS,max} = \frac{5}{2\sqrt{3}\pi} I \approx 0.46 I. \tag{2.65}$$

Peak-to-Peak Charge Ripple

The capacitor charge ripple (i.e., the high-frequency current-time area) is directly proportional to the DC-link voltage ripple, therefore it represents a relevant indicator for the sizing of the DC-link capacitance C_{dc}. In particular, being the peak-to-peak value of the voltage ripple $\Delta V_{dc,pp}$ the typical design criterion for a DC capacitor, the peak-to-peak value of the charge ripple $\Delta Q_{C_{dc},pp} = C_{dc}\,\Delta V_{dc,pp}$ results a normalized indicator of the required C_{dc}.

In three-level unidirectional rectifiers the DC-link capacitor peak-to-peak charge ripple is determined by the low-frequency harmonic components of the mid-point current i_m, which are strongly affected by the adopted modulation strategy and the operating conditions (i.e., M, φ). An overview of the mid-point current instantaneous and local average values for $M = 0.9$ and $\varphi = 0$ is provided in **Fig. 2.16** for all modulation strategies.

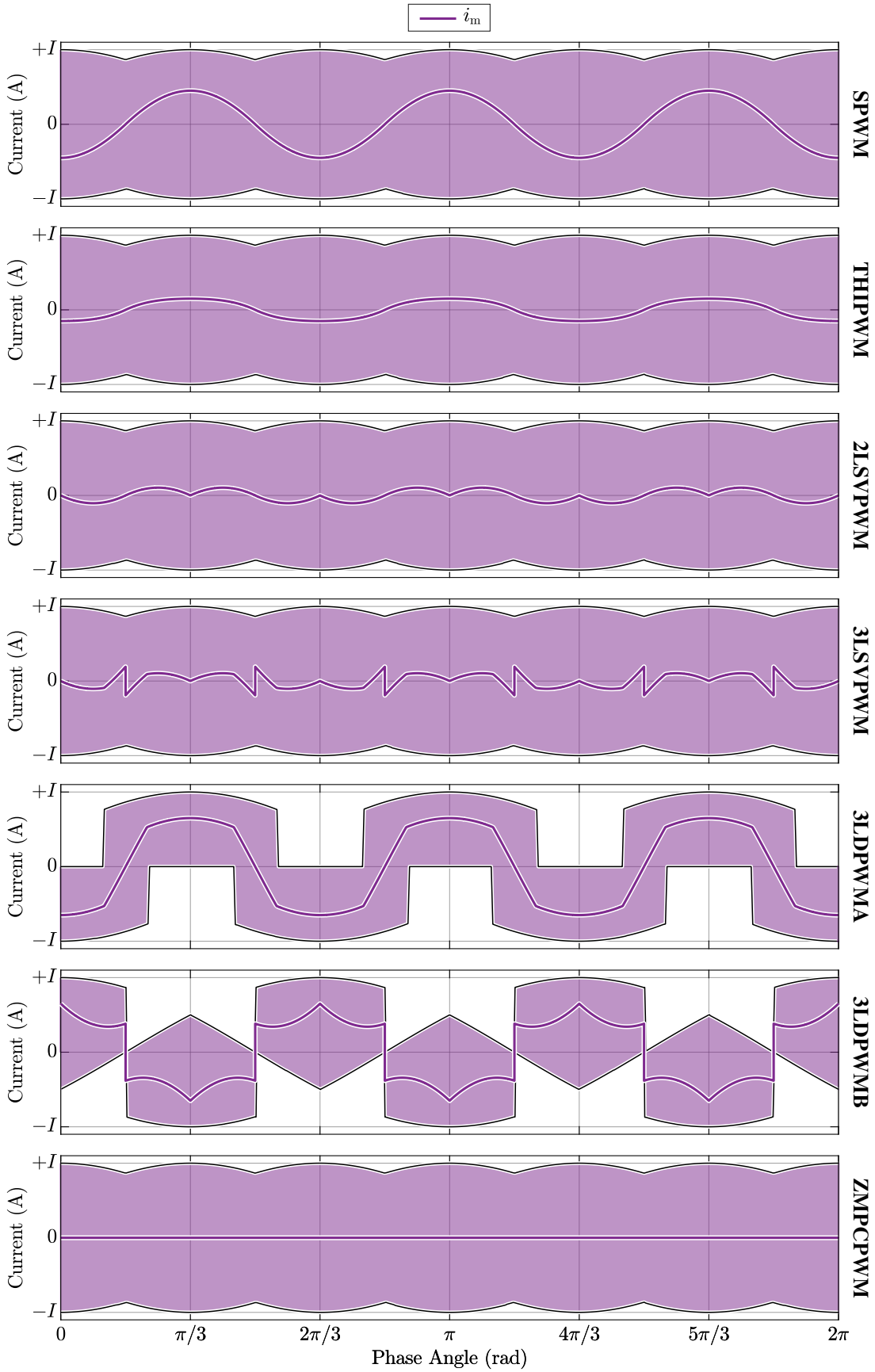


Fig. 2.16: Instantaneous and local average mid-point current i_m waveforms over a grid period for all modulation strategies assuming $M = 0.9$ and $\varphi = 0$.

The peak-to-peak charge ripple of a single DC-link capacitor is equal to

$$\Delta Q_{\mathrm{C_{dc},pp}} = \frac{\Delta Q_{\mathrm{m,pp}}}{2} \tag{2.66}$$

where $\Delta Q_{\mathrm{m,pp}}$ is the DC-link mid-point peak-to-peak charge-ripple, defined as the difference between the maximum and the minimum values achieved by the time-integral of the mid-point current local average i_{m} over $\pi/3$ (i.e., the sector periodicity):

$$\Delta Q_{\mathrm{m,pp}} = \frac{1}{2\pi f}\left(\max\left[\int_0^{\vartheta} i_{\mathrm{m}}\,\mathrm{d}\vartheta\right]_{\vartheta=0}^{\vartheta=\pi/3} - \min\left[\int_0^{\vartheta} i_{\mathrm{m}}\,\mathrm{d}\vartheta\right]_{\vartheta=0}^{\vartheta=\pi/3}\right). \tag{2.67}$$

It is worth noting that the definition in (2.67) only considers the low-frequency charge ripple contribution (i.e., defined by the mid-point current local average i_{m}), since the high-frequency component of the charge ripple directly depends on the rectifier switching frequency f_{sw} and is typically negligible in systems with high switching-to-fundamental frequency ratios [57].

The minimum value of $\Delta Q_{\mathrm{m,pp}}$ is obtained with ZMPCPWM (i.e., the selected modulation strategy), which allows to eliminate the mid-point current local average (i.e., $i_{\mathrm{m}} = 0$) when $M < 1.1$ and $\varphi = 0$. However, the adoption of ZMPCPWM cannot ensure $i_{\mathrm{m}} = 0$ over the complete grid period when $M > 1.1$ or $\varphi \neq 0$, as $v_{\mathrm{o,3}}$ encounters the zero-sequence voltage limits $v_{\mathrm{o,max}}$, $v_{\mathrm{o,min}}$ (cf. **Section 2.3.2**). This is shown in **Fig. 2.17**, where the time-domain waveforms of the zero-sequence voltage v_{o} and the mid-point current local

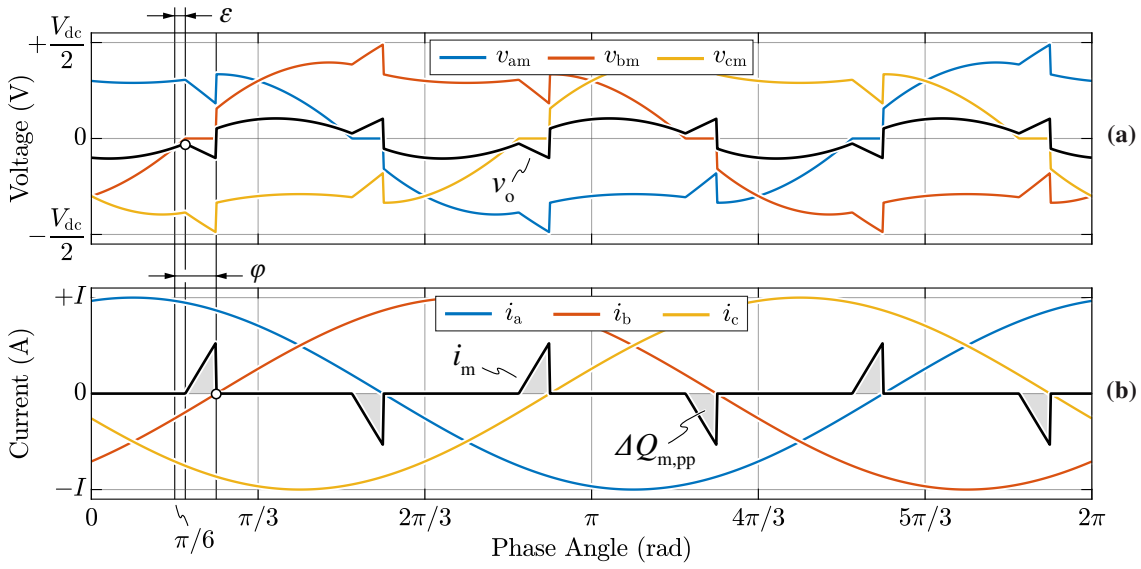


Fig. 2.17: Time-domain waveforms of **(a)** the zero-sequence voltage v_{o} and **(b)** the mid-point current local average i_{m}, assuming $M = 0.8$ (i.e., region ③), $\varphi = 15°$ and ZMPCPWM. The most relevant angle definitions for the analytical calculations (i.e., φ, ε) are indicated.

average i_{m} are shown for $M = 0.8$ and $\varphi = 15^{\circ}$: it is observed that the zero-sequence voltage saturation occurring for $\varphi \neq 0$ causes a deviation of i_{m}, which in turn leads to a non-zero $\Delta Q_{\mathrm{m,pp}}$. Nonetheless, the injection of (2.43) ensures the minimum possible value of $\Delta Q_{\mathrm{m,pp}}$ for every combination of M and φ, since the saturated zero-sequence voltage is as near as possible to the desired $v_{\mathrm{o,3}}$ value. Therefore, ZMPCPWM is particularly beneficial in three-level rectifiers and is very well suited for the considered EV charging application (i.e., which requires minimum DC-link mid-point voltage oscillation).

Fig. 2.17 also shows that when ZMPCPWM is adopted, $i_{\mathrm{m}} \geq 0$ within $0 \leq \vartheta \leq \pi/3$, thus leading to a simplified expression of (2.67):

$$\Delta Q_{\mathrm{m,pp}} = \frac{1}{2\pi f} \int_{0}^{\pi/3} i_{\mathrm{m}} \, \mathrm{d}\vartheta. \tag{2.68}$$

Therefore, due to i_{m} being null for most of the period, the minimum $\Delta Q_{\mathrm{m,pp}}$ can be calculated by restricting the integration interval to

$$\Delta Q_{\mathrm{m,pp}} = \frac{1}{2\pi f} \int_{\pi/6+\varepsilon}^{\pi/6+\varphi} i_{\mathrm{m}} \, \mathrm{d}\vartheta = -\frac{1}{\pi f V_{\mathrm{dc}}} \int_{\pi/6+\varepsilon}^{\pi/6+\varphi} \left[\sum_{\mathrm{x=a,b,c}} v_{\mathrm{x}} \left| i_{\mathrm{x}} \right| + v_{\mathrm{o,min}} \sum_{\mathrm{x=a,b,c}} \left| i_{\mathrm{x}} \right| \right] \mathrm{d}\vartheta, \tag{2.69}$$

where i_{m} has been substituted with (2.17), $v_{\mathrm{o}} = v_{\mathrm{o,min}}$ within $\pi/6 + \varepsilon \leq \vartheta \leq \pi/6 + \varphi$, and ε is obtained by setting $v_{\mathrm{o,3}} = -v_{\mathrm{b}}$, as

$$\varepsilon = \frac{1}{2} \left[\varphi - \frac{\pi}{2} + \cos^{-1}\left(\frac{1}{2} \sin\varphi \right) \right]. \tag{2.70}$$

Finally, substituting (2.4), (2.6), (2.70) into (2.69) and solving the integral terms, the analytical expression of the peak-to-peak DC-link mid-point charge ripple obtained with ZMPCPWM is derived:

$$\Delta Q_{\mathrm{m,pp}} = \frac{\sqrt{3}}{8\pi f} I M \left[\sqrt{4 - \sin^2\varphi} - 2\cos\varphi - \sin\varphi \left(\cos^{-1}\left(\frac{\sin\varphi}{2} \right) - \frac{\pi}{2} - \varphi \right) \right], \tag{2.71}$$

which is valid for $0 \leq M \leq 1.1$. Expression (2.71) is illustrated in normalized form (i.e., divided by $I/3f$) in **Fig. 2.18** as function of M and φ. For $M > 1.1$, $\Delta Q_{\mathrm{m,pp}}$ is calculated numerically. The worst-case value of (2.71) is found for $\varphi = \pm\pi/6$ and $M = 2/3 \approx 0.67$, obtaining

$$\Delta Q_{\mathrm{m,pp,max}} = \frac{\sqrt{3}}{24\pi f} I M \left[\sqrt{3} \left(\sqrt{5} - 2 \right) + \frac{2}{3}\pi - \cos^{-1}\left(\frac{1}{4} \right) \right] \approx 0.082 \, \frac{I}{3f}. \tag{2.72}$$

Analytical expressions similar to (2.71) can be derived for all modulation strategies and are illustrated graphically in **Fig. 2.19** as functions of M and φ. It is mainly observed that discontinuous modulation strategies (i.e., 3LDPWMA, 3LDPWMB) feature a significantly larger $\Delta Q_{\mathrm{m,pp}}$ value with respect to continuous modulation strategies (i.e., SPWM, THIPWM, 2LSVPWM, 3LSVPWM, ZMPCPWM).

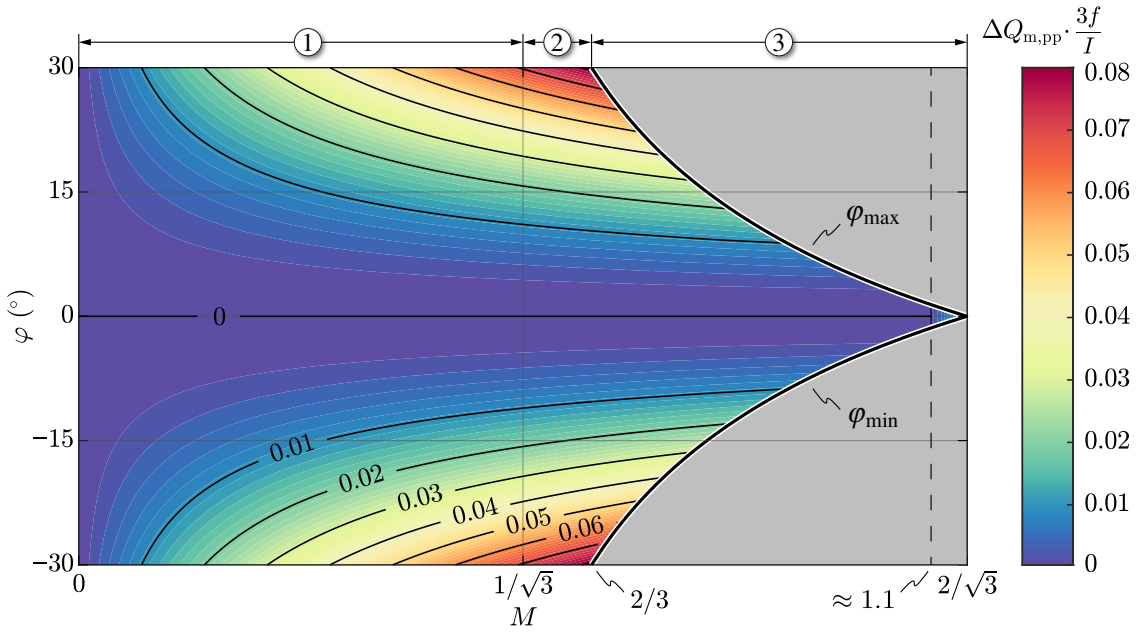


Fig. 2.18: DC-link mid-point peak-to-peak charge ripple $\Delta Q_{\mathrm{m,pp}}$ (i.e., normalized with respect to the peak phase current I and three-times the grid frequency $3f$) as function of the modulation index M and the power factor angle φ for ZMPCPWM (i.e., the selected modulation strategy). The three modulation index regions ①, ② and ③ are indicated (cf. **Fig. 2.9**).

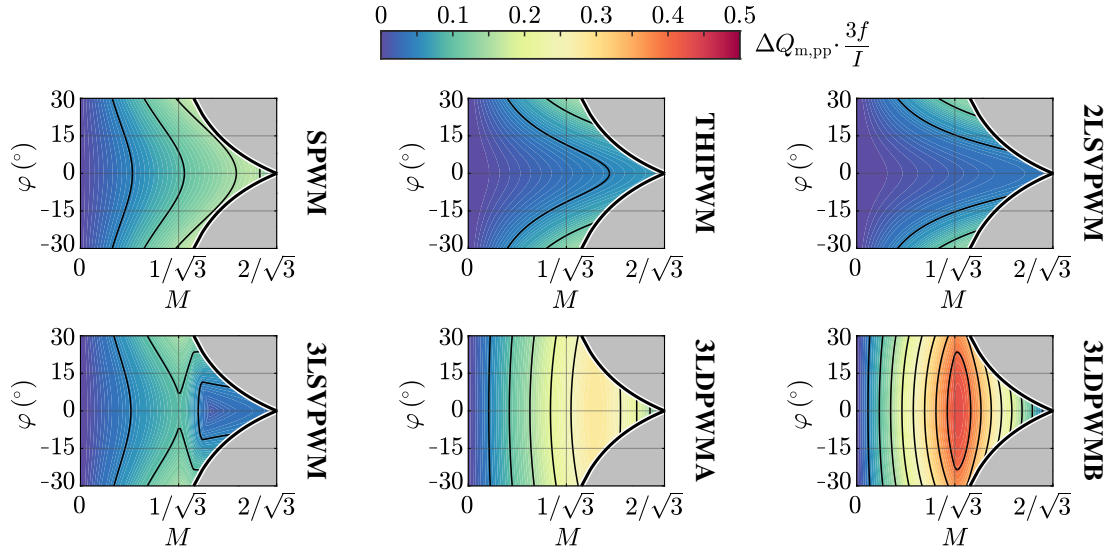


Fig. 2.19: DC-link mid-point peak-to-peak charge ripple $\Delta Q_{\mathrm{m,pp}}$ (i.e., normalized with respect to the peak phase current I and three-times the grid frequency $3f$) as function of the modulation index M and the power factor angle φ for all modulation strategies (except for ZMPCPWM, cf. **Fig. 2.18**).

2.4.3 AC-Side Inductors

The AC-side inductors are critical components of an active rectifier, as they typically represent a large fraction of the total system volume and loss. These components are subject to several current/voltage stresses and must satisfy two main design criteria. First, they must ensure a switching current ripple amplitude below a predefined value, as this affects both the peak current switched by the transistors and the RMS current conducted by all semiconductor devices. Moreover, they must withstand the peak phase current without saturating the magnetic core, as an excessive core saturation would cause a sharp drop of the inductance value, leading to large peak-to-peak current ripple and significant control challenges. Both design criteria must be addressed while ensuring minimum size and loss.

In particular, the inductor losses are determined by the winding current and the flux density swing within the magnetic core. The low-frequency (i.e., 50 Hz) component of both winding current and inductor flux linkage is unrelated to the rectifier topology, modulation strategy and switching frequency, as it only depends on the required power level. Therefore, this section only focuses on the inductor stresses related to the high-frequency current/flux component, which determines the high-frequency winding and core losses.

RMS Flux Ripple

In general, there is a direct relation between the inductor high-frequency losses and its flux linkage ripple $\Delta\psi$ (i.e., the high-frequency voltage-time area applied to the inductor), as it directly determines the winding current ripple $\Delta i \propto \Delta\psi$ (i.e., inversely proportional to the inductance value) and the high-frequency core flux density swing $\Delta B \propto \Delta\psi$. The instantaneous phase flux linkage ripple is mathematically defined as the time integral of the high-frequency component of the phase voltage $v_{\mathrm{x,HF}}$ (i.e., assuming that it is completely applied across the inductor) as

$$\Delta\psi_{\mathrm{x}} = \int_0^t v_{\mathrm{x,HF}}\,\mathrm{d}t \qquad \mathrm{x} = \mathrm{a, b, c.} \tag{2.73}$$

This modeling approach has been adopted and experimentally validated in [70], demonstrating a high level of accuracy. The three-level rectifier time-domain waveforms of $\Delta\psi$ are shown in **Fig. 2.20** for all modulation strategies assuming $M = 0.9$ and $\varphi = 0$. It is mainly observed that, for fixed rectifier switching frequency and DC-link voltage values, the discontinuous modulation strategies (i.e., 3LDPWMA, 3LDPWMB) feature a larger flux ripple with respect to their continuous counterparts (i.e., SPWM, THIPWM, 2LSVPWM, 3LSVPWM, ZMPCPWM).

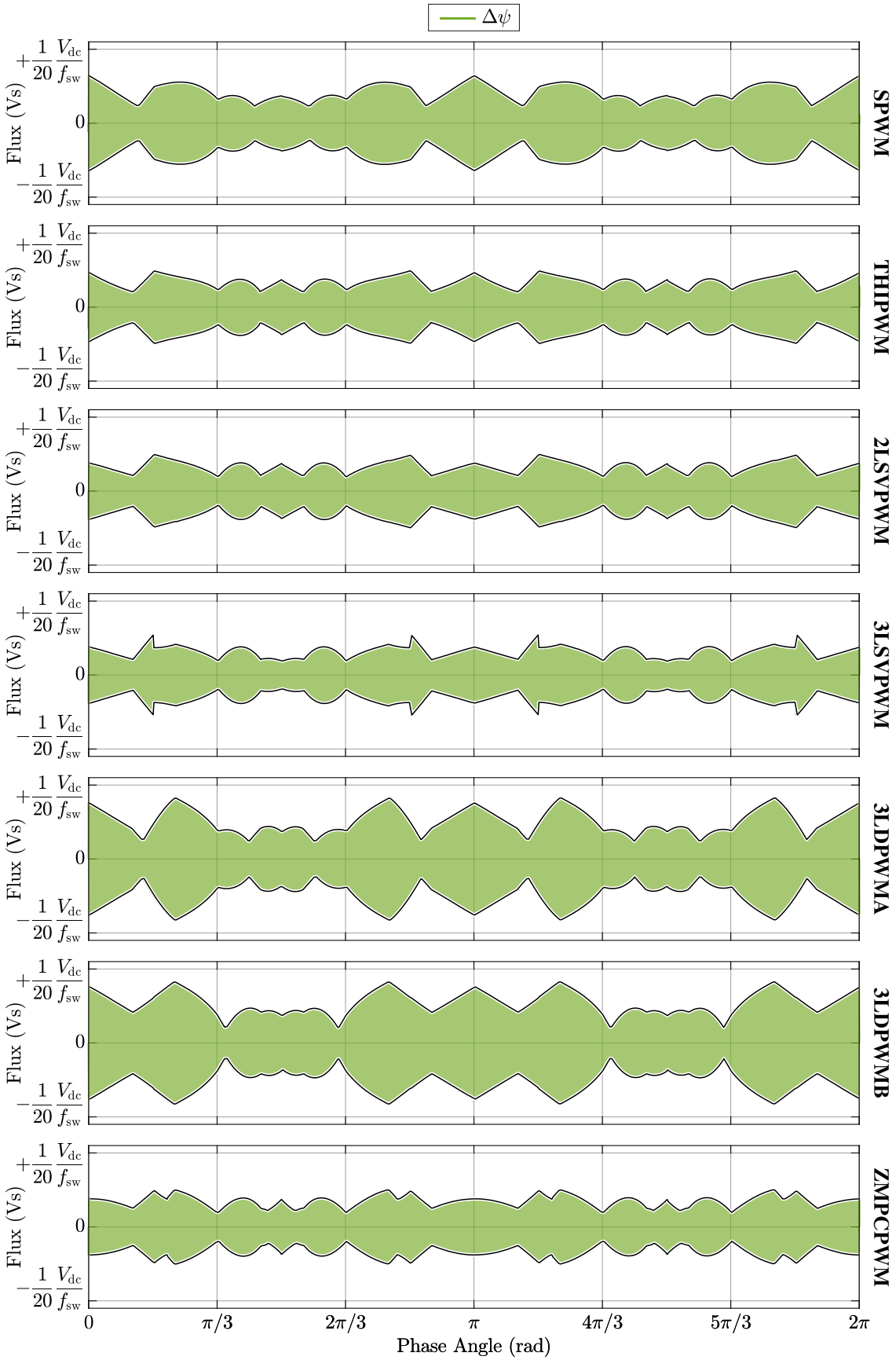


Fig. 2.20: Instantaneous phase flux ripple $\Delta\psi$ waveforms over a grid period for all modulation strategies assuming $M = 0.9$ and $\varphi = 0$.

Since the high-frequency winding losses are $\propto \Delta i^2$ (i.e., for a given switching frequency) and the high-frequency core losses are approximately $\propto \Delta B^2$ (i.e., assuming a core material with a Steinmetz loss coefficient ≈ 2), the total inductor high-frequency losses are approximately proportional to the square of the local RMS phase flux linkage ripple [81], defined as

$$\Delta\psi^2_{\mathrm{x,RMS}} = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} \Delta\psi^2_{\mathrm{x}}\, \mathrm{d}t \qquad \mathrm{x} = \mathrm{a, b, c}, \tag{2.74}$$

where $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$ is the switching period. The global RMS value of $\Delta\psi$, which can be obtained by averaging the local RMS flux ripple contributions of all three phases over one sector (i.e., $\pi/3$) as

$$\Delta\Psi^2_{\mathrm{RMS}} = \frac{1}{2\pi} \int_0^{2\pi} \Delta\psi^2_{\mathrm{x,RMS}}\, \mathrm{d}\vartheta = \frac{3}{\pi} \int_0^{\pi/3} \frac{\Delta\psi^2_{\mathrm{a,RMS}} + \Delta\psi^2_{\mathrm{b,RMS}} + \Delta\psi^2_{\mathrm{c,RMS}}}{3}\, \mathrm{d}\vartheta, \tag{2.75}$$

is therefore a key performance indicator for the design of the inductive components.

To simplify the analytical derivation of $\Delta\Psi^2_{\mathrm{RMS}}$, a unified local RMS flux ripple (i.e., taking into account all three phases) is defined as

$$\Delta\psi^2_{\mathrm{RMS}} = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} \frac{\Delta\psi^2_{\mathrm{a}} + \Delta\psi^2_{\mathrm{b}} + \Delta\psi^2_{\mathrm{c}}}{3}\, \mathrm{d}t = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} \frac{3}{2} \frac{\Delta\psi^2_{\alpha} + \Delta\psi^2_{\beta}}{3}\, \mathrm{d}t = \frac{1}{2}\Delta\psi^2_{\alpha\beta,\mathrm{RMS}}, \tag{2.76}$$

where $\Delta\psi_\alpha$ and $\Delta\psi_\beta$ are the flux ripple components with respect to the $\alpha\beta$-axes defined in space vector theory. The expressions of $\Delta\psi_\alpha$ and $\Delta\psi_\beta$ can be obtained by integration of the high-frequency $\alpha\beta$ component of the AC-side voltage, resulting in a piece-wise linear function. Being N the total number of transitions in the switching sequence, the flux ripple values at each state transition are defined as

$$\begin{cases} \Delta\vec{\psi}_{0,\alpha\beta} = -\Delta\vec{\psi}_{\alpha\beta,\mathrm{AVG}} \\ \Delta\vec{\psi}_{\mathrm{k},\alpha\beta} = \Delta\vec{\psi}_{\mathrm{k}-1,\alpha\beta} + \left(\vec{V}_{\mathrm{k},\alpha\beta} - \vec{V}_{\alpha\beta}\right) \delta_{\mathrm{k}}\, T_{\mathrm{sw}} \qquad \mathrm{k} = 1,..,N+1 \end{cases} \tag{2.77}$$

where $\vec{V}_{\mathrm{k},\alpha\beta}$ is the applied space vector (cf. **Fig. 2.3**), $\vec{V}_{\alpha\beta}$ is the reference voltage vector defined in (2.5) and $\delta_{\mathrm{k}}\, T_{\mathrm{sw}}$ is the space vector dwell-time. The space vector and the reference voltage vector are both are expressed in the $\alpha\beta$ coordinates.

In general, in order to obtain a flux ripple waveform with zero average over a switching period, the starting value $\Delta\vec{\psi}_{0,\alpha\beta}$ must be equal to the ripple average changed in sign,

which can be derived in a first iteration considering $\vec{\Delta\psi}_{0,\alpha\beta} = 0$ as

$$\vec{\Delta\psi}_{\alpha\beta,\mathrm{AVG}} = \frac{1}{2}\sum_{\mathrm{k}=1}^{N+1} \delta_{\mathrm{k}} \left(\vec{\Delta\psi}_{\mathrm{k}-1,\alpha\beta} + \vec{\Delta\psi}_{\mathrm{k},\alpha\beta} \right). \tag{2.78}$$

A zero flux ripple average is already ensured by symmetric pulse patterns (i.e., the present case), but it is not guaranteed for asymmetric ones [82]. The RMS value of $\vec{\Delta\psi}_{\alpha\beta}$ can be thus calculated by exploiting its piece-wise linear properties:

$$\Delta\psi^2_{\alpha\beta,\mathrm{RMS}} = \frac{1}{3}\sum_{\mathrm{k}=1}^{N+1} \delta_{\mathrm{k}} \Bigg[\left(\Delta\psi^2_{\mathrm{k}-1,\alpha} + \Delta\psi^2_{\mathrm{k},\alpha} + \Delta\psi_{\mathrm{k}-1,\alpha}\Delta\psi_{\mathrm{k},\alpha} \right) + \left(\Delta\psi^2_{\mathrm{k}-1,\beta} + \Delta\psi^2_{\mathrm{k},\beta} + \Delta\psi_{\mathrm{k}-1,\beta}\Delta\psi_{\mathrm{k},\beta} \right) \Bigg]. \tag{2.79}$$

Therefore, substituting (2.79) into (2.76) and averaging $\Delta\psi^2_{\mathrm{RMS}}$ over a single sector (i.e., $\pi/3$), the global RMS flux ripple is obtained as

$$\Delta\Psi^2_{\mathrm{RMS}} = \frac{3}{\pi}\int_0^{\pi/3} \Delta\psi^2_{\mathrm{RMS}}\, \mathrm{d}\vartheta. \tag{2.80}$$

The presented procedure is valid for all modulation strategies and is here applied to ZMPCPWM for demonstration purposes (i.e., exploiting the approximated zero-sequence voltage expression in (2.44)), resulting in two different expressions of the global RMS flux ripple for region ① and regions ②, ③:

$$\Delta\Psi^2_{\mathrm{RMS},①} \approx \frac{V_{\mathrm{dc}}^2}{128 f_{\mathrm{sw}}^2} \left[\frac{7}{8}M^4 - \frac{112\sqrt{3}+45}{63\pi}M^3 + \frac{34\pi - 33\sqrt{3}}{36\pi}M^2 \right], \tag{2.81}$$

$$\Delta\Psi^2_{\mathrm{RMS},②} = \Delta\Psi^2_{\mathrm{RMS},③} \approx \frac{V_{\mathrm{dc}}^2}{64 f_{\mathrm{sw}}^2} \Bigg[\frac{7}{16}M^4 - \frac{112\sqrt{3}+45}{126\pi}M^3 + \Bigg(\frac{34\pi - 33\sqrt{3}}{36\pi} + \frac{4}{\pi}\cos^{-1}\left(\frac{1}{\sqrt{3M}}\right) - \frac{16}{9\pi}\sqrt{3M^2-1} \Bigg) M^2 + \frac{8}{9\pi}\cos^{-1}\left(\frac{1}{\sqrt{3}M}\right) - \frac{44}{27\pi}\sqrt{3M^2-1} \Bigg], \tag{2.82}$$

It is worth noting that (2.81) and (2.82) are valid for $0 \leq M \leq 1.1$ and $\varphi = 0$, as they do not account for the zero-sequence voltage saturation. For completeness, the global RMS flux ripple is calculated numerically for all modulation strategies as function of M and φ and is illustrated in normalized form (i.e., divided by $V_{\mathrm{dc}}/f_{\mathrm{sw}}$) in **Fig. 2.21** for ZMPCPWM and in **Fig. 2.22** for the remaining modulation strategies. As expected,

it is observed that discontinuous modulation strategies (i.e., 3LDPWMA, 3LDPWMB) feature a larger flux ripple stress with respect to their continuous counterparts (i.e., SPWM, THIPWM, 2LSVPWM, 3LSVPWM, ZMPCPWM). Nonetheless, they provide a switching loss advantage (cf. **Section 2.4.1**), which may be exploited to increase the switching frequency and thus reduce the global RMS flux ripple [70].

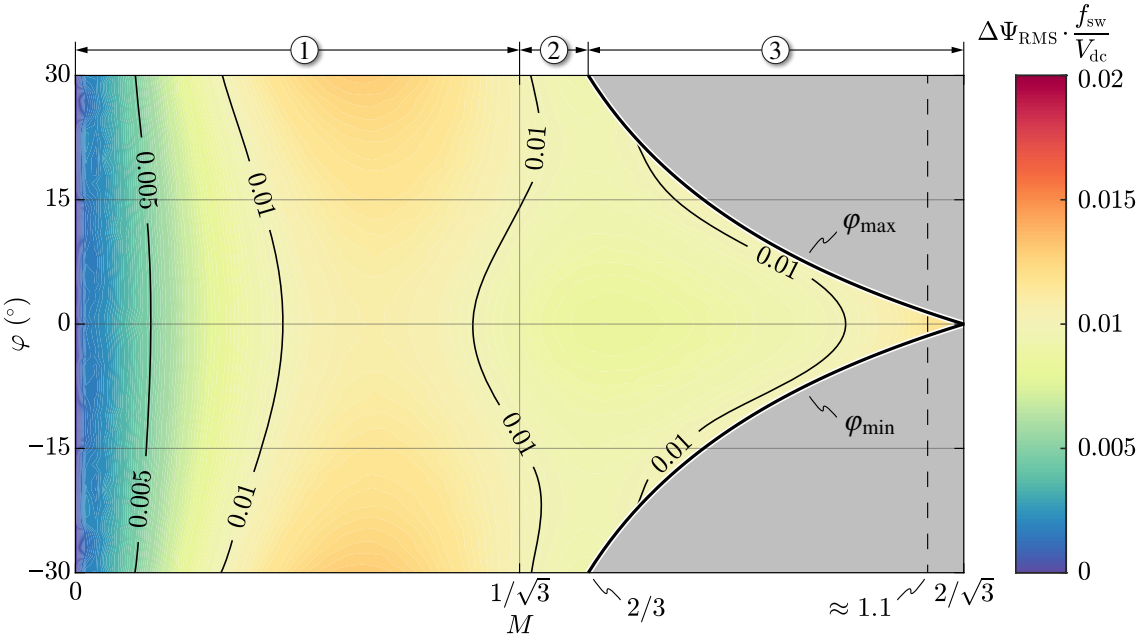


Fig. 2.21: Global RMS phase flux ripple $\Delta\Psi_{\mathrm{RMS}}$ (i.e., normalized with respect to the DC-link voltage V_{dc} and the switching frequency f_{sw}) as function of the modulation index M and the power factor angle φ for ZMPCPWM (i.e., the selected modulation strategy). The three modulation index regions ①, ② and ③ are indicated (cf. **Fig. 2.9**).

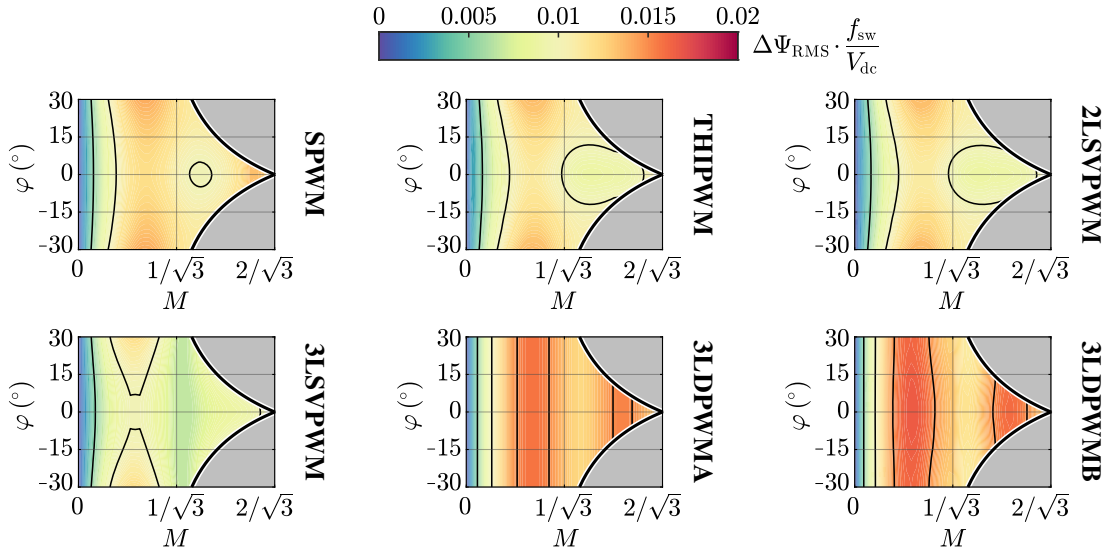


Fig. 2.22: Global RMS phase flux ripple $\Delta\Psi_{\mathrm{RMS}}$ (i.e., normalized with respect to the DC-link voltage V_{dc} and the switching frequency f_{sw}) as function of the modulation index M and the power factor angle φ for all modulation strategies (except for ZMPCPWM, cf. **Fig. 2.21**).

Peak-to-Peak Flux Ripple

The inductor peak-to-peak flux ripple is directly proportional to the peak-to-peak phase current ripple (i.e., $\Delta i = \Delta\psi/L$) and thus determines the required minimum inductance value. The peak-to-peak flux ripple is defined as the difference between the maximum and the minimum values of the instantaneous phase flux ripple $\Delta\psi$ over the complete grid period, as

$$\Delta\Psi_{\mathrm{pp}} = \max\left[\Delta\psi_{\mathrm{x}}\right]_{\vartheta=0}^{\vartheta=2\pi} - \min\left[\Delta\psi_{\mathrm{x}}\right]_{\vartheta=0}^{\vartheta=2\pi} \qquad \mathrm{x} = \mathrm{a},\,\mathrm{b},\,\mathrm{c}, \tag{2.83}$$

which is independent of the selected phase (i.e., for symmetry reasons).

However, the closed-form analytical derivation of $\Delta\Psi_{\mathrm{pp}}$ is extremely complicated, resulting in complex piece-wise defined expressions with little practical value. Therefore, a numerical approach is adopted herein to determine the value of $\Delta\Psi_{\mathrm{pp}}$ as function of M, φ and the modulation strategy. The results are illustrated in normalized form (i.e., divided by $V_{\mathrm{dc}}/f_{\mathrm{sw}}$) in **Fig. 2.23** for ZMPCPWM and in **Fig. 2.24** for the remaining modulation strategies. As opposed to $\Delta\Psi_{\mathrm{RMS}}$, it is observed that the worst-case value of $\Delta\Psi_{\mathrm{pp}}$ is similar among continuous and discontinuous modulation strategies. However, 3LDPWMA and 3LDPWMB still feature significantly worse performance than continuous modulation strategies (i.e., SPWM, THIPWM, 2LSVPWM, 3LSVPWM, ZMPCPWM) in the typical rectifier operating range (i.e., $M \geq 2/3$, region ③).

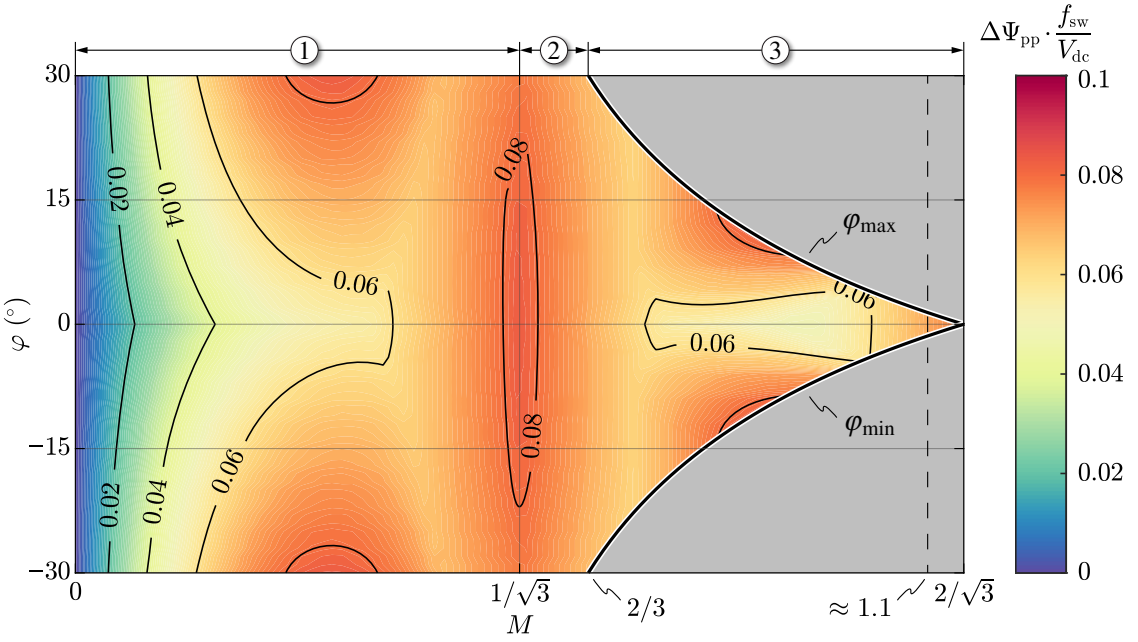


Fig. 2.23: Global peak-to-peak phase flux ripple $\Delta\Psi_{\mathrm{pp}}$ (i.e., normalized with respect to the DC-link voltage V_{dc} and the switching frequency f_{sw}) as function of the modulation index M and the power factor angle φ for ZMPCPWM (i.e., the selected modulation strategy). The three modulation index regions ①, ② and ③ are indicated (cf. **Fig. 2.9**).

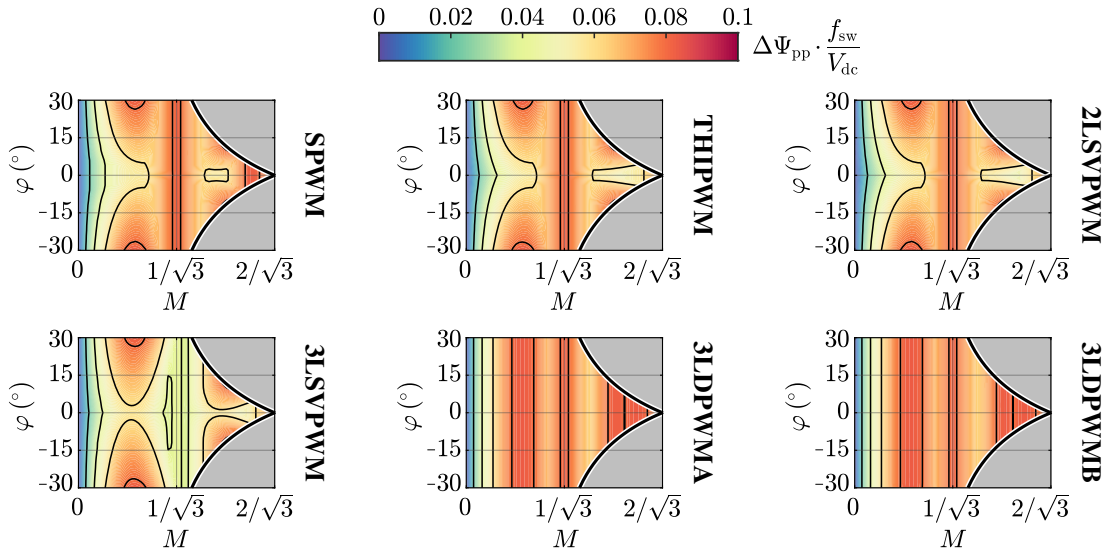


Fig. 2.24: Global peak-to-peak phase flux ripple $\Delta\Psi_{pp}$ (i.e., normalized with respect to the DC-link voltage V_{dc} and the switching frequency f_{sw}) as function of the modulation index M and the power factor angle φ for all modulation strategies (except for ZMPCPWM, cf. **Fig. 2.23**).

2.5 Summary

In this chapter, a comprehensive analysis of the grid-connected AC/DC conversion stage of an electric vehicle (EV) ultra-fast battery charger has been provided. A unidirectional three-level T-type converter topology has been selected for the present 60 kW application, owing to its promising features such as low semiconductor count, active switches with reduced voltage rating, three-level AC voltage waveforms and split DC-link output. The operational basics of three-level unidirectional rectifiers have been described with a particular focus on the zero-sequence voltage injection limits, which have been shown to determine the maximum modulation index (i.e., defining the minimum DC-link voltage for a given grid voltage amplitude), the feasible power factor angle range (i.e., the maximum reactive power capability) and the mid-point current generation limits (i.e., affecting the ability to tolerate an unbalance between the two split DC-link loads). The three-level pulse-width modulation process has been described and seven different modulation strategies have been introduced. In particular, the zero mid-point current modulation (ZMPCPWM) has been selected as the most suited modulation strategy for the present application, as it ensures minimum low-frequency DC-link mid-point voltage oscillation, which is critical for EV charging. Finally, with the goal of providing straightforward tools for the design of the rectifier, the converter active and passive component stresses have been extensively assessed analytically and/or numerically, including the semiconductor losses, the DC-link RMS current and charge ripple, and the AC-side inductor RMS and peak-to-peak flux ripple. Such comprehensive analytical assessment is currently not available in literature and is thus a contribution of this work.

Chapter 3

AC/DC Converter – Design

Abstract

The AC/DC stage of an electric vehicle (EV) ultra-fast battery charger must simultaneously achieve high conversion efficiency and high power density, leading to a challenging power converter design. This chapter outlines the complete design methodology of the considered 60 kW three-phase three-level T-type rectifier. In view of the high target nominal power, a six-leg (i.e., dual three-phase) converter structure is adopted, halving the current rating of each bridge-leg and thus allowing for the adoption of discrete Si semiconductor devices (i.e., MOSFETs and diodes). Therefore, the step-by-step converter design procedure is described, including the selection, sizing and/or optimization of all main converter active and passive components, i.e. the semiconductor devices, the DC-link capacitors, the AC-side inductors and the heat dissipation system (i.e., heatsink and fans). Finally, the realized 60 kW converter prototype is shown and its performance in terms of loss and efficiency is assessed experimentally leveraging a purposely developed automated test setup.

3.1 Introduction

As outlined in **Section 2.1**, an active front-end for EV ultra-fast charging must simultaneously ensure sinusoidal input current shaping (i.e., with low harmonic content), regulated output voltage, ohmic grid behavior (i.e., with a desirable option of generating/absorbing reactive power), high conversion efficiency and high power density. In particular, the last two requirements demand for an accurate topology selection and a proper converter design.

Since DC fast chargers typically require unidirectional power flow from the grid to the battery, three-level rectifiers are an attractive candidate for this application, due to their excellent trade-off among semiconductor cost, control/modulation complexity and

achievable performance. In particular, the T-type topology provides the most promising converter-level performance among three-level unidirectional rectifiers (cf. **Section 2.1.2**), featuring the lowest semiconductor device and gate driver count (i.e., with two transistors and two fast-recovery diodes per bridge-leg) and ensuring minimum conduction losses (i.e., with either one diode or two transistors in the conduction path).

Even though the design and assessment of three-level T-type inverters (i.e., with bidirectional power capability) has already been extensively reported in literature [53, 83, 84], only few unidirectional T-type rectifier designs have been published. For instance, [85] describes the design of a 20 kW, 140 kHz all-SiC T-type rectifier achieving a peak efficiency $> 98.5\,\%$. However, the design process is not fully described and no details are given on the design of the converter AC-side inductors and DC-link capacitors. Another T-type rectifier prototype is reported in [86], where a 3 kW 22 kHz six-leg interleaved converter is implemented with SiC MOSFETs and SiC diodes. This converter achieves a peak efficiency $> 99\,\%$ due to the relatively low switching frequency, the adoption of SiC devices and the use of coupled inductors between parallel bridge-legs. Nevertheless, also in this case the design/selection criteria for the passive components and the thermal dissipation system are not described. Therefore, the goal of this chapter is to describe a complete methodology for the design of the considered 60 kW three-phase three-level unidirectional T-type rectifier for EV ultra-fast battery charging. In particular, the proposed step-by-step procedure includes the description of the adopted analytical/numerical models and provides the criteria for the selection, design and/or optimization of all main active and passive converter components, including the semiconductor devices, the DC-link capacitors, the AC-side inductors and the loss dissipation system (i.e., heatsink and fans). It is worth noting that the AC-side filter (i.e., necessary to satisfy the grid-code and/or EMI requirements) is not designed here, since it is outside of the scope of the project.

3.1.1 Specifications and Performance Targets

The specifications and the performance targets of the considered AC/DC converter are reported in **Tab. 3.1**. In particular, the ability to operate at different DC-link voltage levels between 650 V and 800 V is required, as this allows to narrow the input/output voltage regulation interval of the subsequent DC/DC stage, enabling enhanced performance at the system level (cf. **Chapter 6**). Furthermore, a nominal efficiency $\geq 98.5\,\%$ (i.e., at 60 kW and 650 V) is targeted.

Tab. 3.1: AC/DC converter specifications and performance targets.

Parameter	Description	Value
P	nominal power	60 kW
f	grid frequency	50 Hz
V	peak phase voltage	325 V
I	peak phase current	123 A
V_{dc}	DC-link voltage range	650… 800 V
M	modulation index range	0.81… 1.0
η	target nominal efficiency	$\geq 98.5\,\%$

In view of the advantages presented in **Section 2.1.2**, the three-level unidirectional T-type rectifier topology is selected. Moreover, due to the large input phase current requirement (i.e., $I = 123\,\mathrm{A}$ peak, cf. **Tab. 3.1**), a modular approach to the full power is adopted by paralleling two bridge-legs per phase, allowing for the utilization of discrete Si semiconductor components. The schematic of the considered six-leg three-level unidirectional T-type rectifier is illustrated in **Fig. 3.1**.

The modular approach leads to several benefits with respect to simply hard-paralleling MOSFETs and diodes, namely the avoidance of static and dynamic current sharing issues

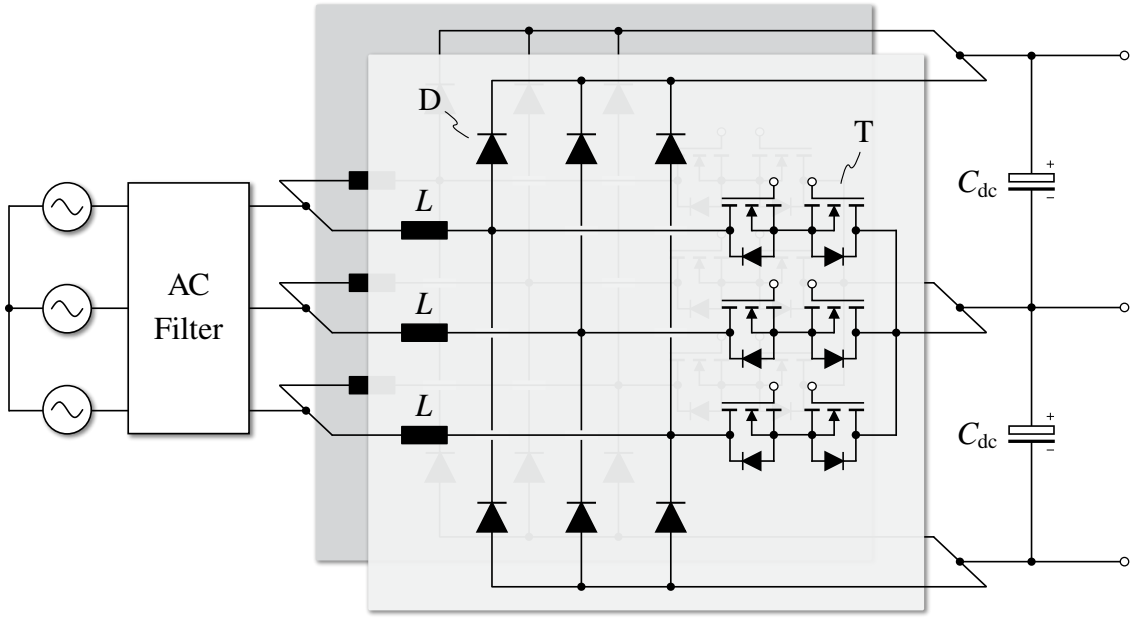


Fig. 3.1: Equivalent circuit schematic of the considered six-leg three-level unidirectional T-type rectifier connected to the three-phase grid. The design of the AC filter is not included in this work.

among semiconductor devices, the reduction of the single AC-side inductor size (i.e., broadening the core availability and simplifying the winding arrangement) and the ability to interleave the bridge-leg switching signals. In particular, even though the PWM interleaving of parallel bridge-legs reduces both the RMS current stress on the DC-link capacitors [87] and the grid-side current harmonics [88], the phase shift between the PWM carriers in three-phase systems leads to the appearance of additional harmonics across the phase inductors, thus negatively affecting their performance in terms of size and loss [88]. Moreover, if not properly addressed, the additional recirculating current ripple flowing between parallel bridge-legs can generate a large modulation error in unidirectional rectifier, particularly at light load [86]. Although the aforementioned issues may be addressed by adopting coupled inductors (i.e., inter-phase transformers) [86, 88, 89], PWM interleaving is not considered in this work to reduce the overall system complexity.

Part of the content of this chapter has been published in [90].

3.2 Component Design/Selection

In this section, the main converter active and passive components are designed or selected, either exploiting the stresses derived in **Section 2.4** (i.e., semiconductor devices, DC-link capacitors, heat dissipation system) or as the outcome of an optimization procedure (i.e., AC-side inductors). Moreover, the adopted models for the estimation of the component losses and the converter efficiency are described.

3.2.1 Semiconductor Devices

Targeting a full-Si converter realization (cf. **Chapter 1**) and aiming to minimize the semiconductor losses, the best performing commercially available 600/650 V Si MOSFETs and 1200 V Si fast-recovery diodes (i.e., in a discrete package) are selected. Since the switching transitions within a unidirectional T-type rectifier bridge-leg only take place between a MOSFET (i.e., the mid-point switch) and a diode, the transistor should feature minimum resistance per-unit of chip area (i.e., optimized for low conduction losses), being its switching characteristics of secondary importance as the MOSFET body-diode is not involved in the commutation process. The bridge diodes, instead, require the best possible trade-off between switching and conduction characteristics, as their reverse-recovery charge largely affects the converter switching losses. Therefore, the Infineon IPW65R019C7 Si Superjunction MOSFET (650 V, 19 mΩ) is selected as mid-point switch, featuring the

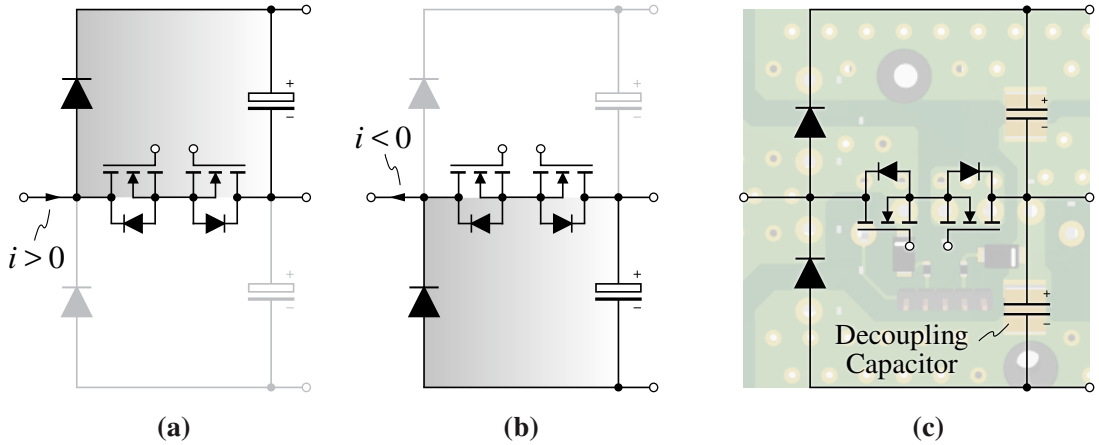


Fig. 3.2: Equivalent circuit schematic of the unidirectional T-type rectifier bridge-leg, with highlight of the commutation loop for **(a)** $i > 0$ and **(b)** $i < 0$. **(c)** overview of the realized commutation loop and component layout on the printed circuit board (PCB), with highlight of the semiconductor devices and decoupling capacitors.

lowest on-state resistance among all commercially available TO-247 650 V Si MOSFETs, whereas the Vishay VS-E5PH6012L-N3 Hyperfast diode (1200 V, 60 A) is selected for the input diode bridge.

A challenging task related to the practical implementation of a T-type rectifier is the minimization of the commutation loop stray inductance, which negatively affects the switching performance of the converter by increasing both turn-on and turn-off voltage overshoots and thus limiting the feasible switching speed. In fact, the commutation loop of a T-type rectifier bridge-leg includes three semiconductor devices (i.e., two transistors and one diode, cf. **Fig. 3.2(a)–(b)**), therefore their placing is of primary importance to ensure minimum overall stray inductance [85]. An overview of the realized bridge-leg layout is shown in **Fig. 3.2(c)**, where a planar commutation loop has been designed: the location of the semiconductor devices and the decoupling capacitors is highlighted.

As outlined in **Section 2.4.1**, the most accurate way to estimate the average conduction losses of each semiconductor device is by directly exploiting its conduction characteristics $v(i, T_\mathrm{j})$ (i.e., provided in the manufacturer datasheet), the instantaneous bridge-leg current i, the device duty-cycle d, and the semiconductor junction temperature T_j, as

$$P_\mathrm{cond} = \frac{1}{T} \int_0^T d\, v(i, T_\mathrm{j})\, i \, \mathrm{d}t, \tag{3.1}$$

where $T = 1/f$ is the grid fundamental period. The conduction characteristics of the selected MOSFET and diode are illustrated in **Fig. 3.3** for both $T_\mathrm{j} = 25\,^\circ\mathrm{C}$ and $T_\mathrm{j} = 125\,^\circ\mathrm{C}$.

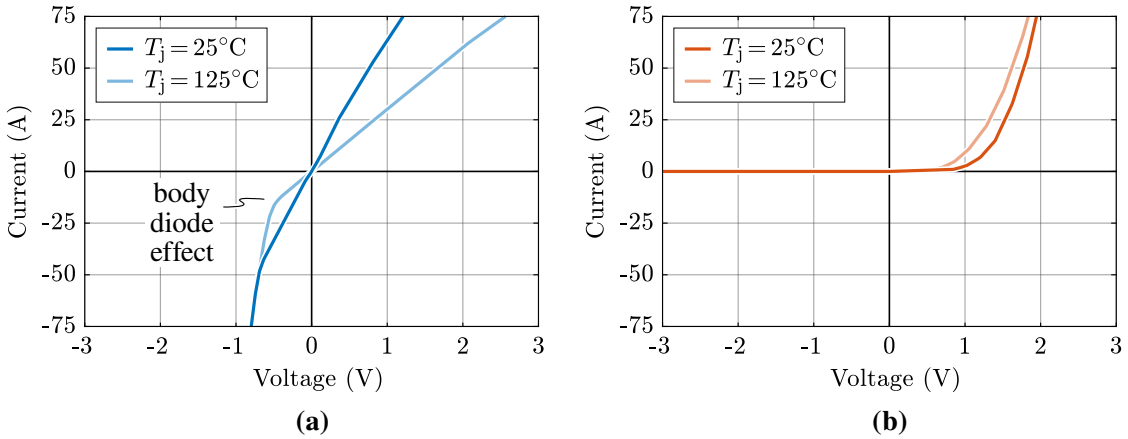


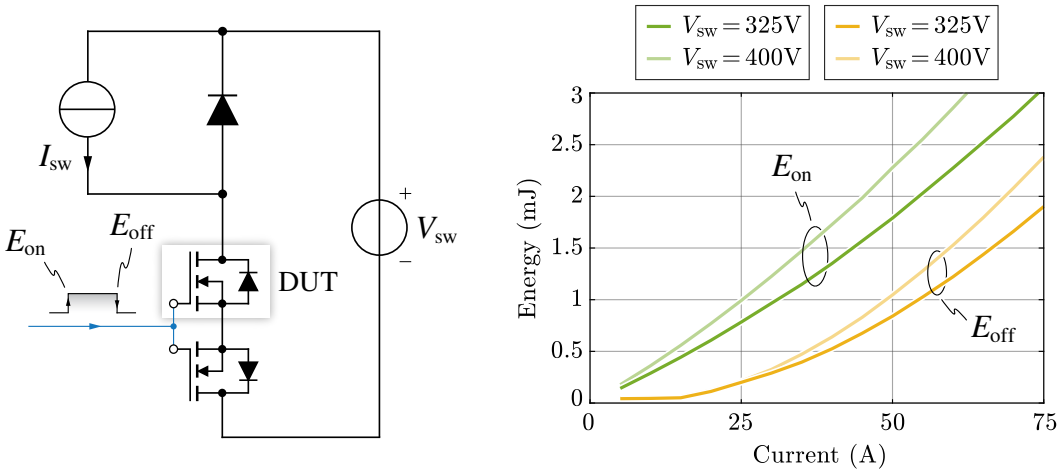
Fig. 3.3: Conduction characteristics of **(a)** Infineon IPW65R019C7 650 V Si Superjunction MOSFET and **(b)** Vishay VS-E5PH6012L-N3 1200 V Si Hyperfast diode, for $T_j = 25\,°C$ and $T_j = 125\,°C$.

In order to estimate the instantaneous value of T_j and thus P_{cond}, a combined iterative electro-thermal model is implemented, based on the thermal data reported in **Section 3.2.4**.

Similarly, the switching losses of one bridge-leg are estimated numerically with the following relation, i.e.

$$P_{sw} = \frac{f_{sw}}{T} \int_0^T \left[E_{on}(i_{sw}, V_{sw}) + E_{off}(i_{sw}, V_{sw}) \right] \mathrm{d}t, \tag{3.2}$$

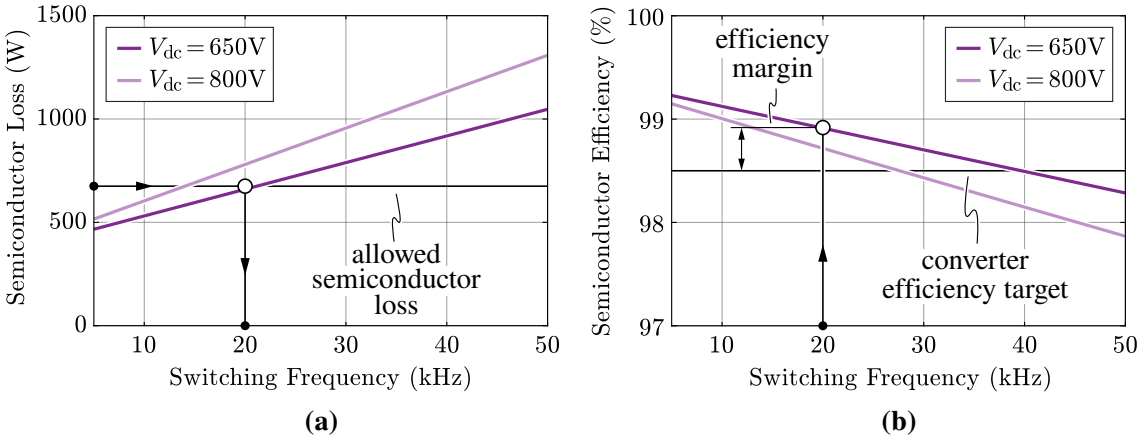
where i_{sw} is the switched current, $V_{sw} = V_{dc}/2$ is the switched voltage and E_{on}, E_{off} are the turn-on and turn-off switching energies, respectively. In particular, both E_{on} and E_{off} are obtained with a set of circuit simulations at different current and voltage levels in Spice environment (cf. **Fig. 3.4(a)**), exploiting the equivalent circuit models provided by the semiconductor device manufacturers, which also include package-related parasitic elements (e.g., stray inductance). The gate resistance value recommended in the MOSFET datasheet is used for the loss extraction. The results are shown in **Fig. 3.4(b)** for $V_{sw} = 325\,V$ and $V_{sw} = 400\,V$. It is worth noting that E_{on} includes the reverse-recovery energy of the bridge diode involved in the commutation and is therefore junction temperature dependent. Nevertheless, the available VS-E5PH6012L-N3 diode Spice model does not feature thermal properties and/or dependencies, therefore the switching losses are only extracted for $T_j = 25\,°C$.



(a) **(b)**

Fig. 3.4: **(a)** equivalent circuit schematic of the simulation implemented in Spice for the switching loss extraction and **(b)** turn-on and turn-off switching energy results for $V_{sw} = 325\,V$ and $V_{sw} = 400\,V$.

The worst-case total converter losses are estimated assuming a maximum operating junction temperature of $T_j = 125\,°C$. The results are illustrated in **Fig. 3.5(a)** for $V_{dc} = 650\,V$ and $V_{dc} = 800\,V$ as functions of the rectifier switching frequency f_{sw}. In order to achieve the target converter efficiency $\geq 98.5\,\%$ (i.e., $\leq 900\,W$ loss) at $P = 60\,kW$ and $V_{dc} = 650\,V$, only 75 % of the allowed loss is assigned to the semiconductor devices (675 W), leaving a 225 W margin for the remaining loss components, mostly determined by the AC-side inductors and the DC-link capacitors. According to **Fig. 3.5(a)**, the maximum f_{sw} value that allows to satisfy the semiconductor loss budget is $\approx 20\,kHz$, which is selected as design value.



(a) **(b)**

Fig. 3.5: Estimated **(a)** semiconductor loss and **(b)** semiconductor efficiency at $P = 60\,kW$ and $T_j = 125\,°C$ for $V_{dc} = 650\,V$ and $V_{dc} = 800\,V$. The allowed semiconductor loss leads to the selection of $f_{sw} = 20\,kHz$.

3.2.2 DC-Link Capacitors

The total DC-link capacitance C_{dc} required by the application (i.e., for each split DC-link) is obtained as the value that satisfies both the RMS current and peak-to-peak voltage ripple constraints.

The analytical expression of the DC-link RMS current stress is reported in (2.64) and is graphically illustrated in **Fig. 3.6(a)**. In the present case, the converter operation is restricted within $0.81 \leq M \leq 1$ (cf. **Tab. 3.1**) and, due to the unidirectional nature of the rectifier, within $|\varphi| \leq \sin^{-1}(1/\sqrt{3}M) - \pi/6$ (cf. **Section 2.2.4**). Therefore the maximum DC-link RMS current value is obtained for $M = 0.81$ and $\varphi = 0$, resulting in $I_{\mathrm{C_{dc},RMS,max}} \approx 54\,\mathrm{A}$.

The minimum DC-link capacitance value that ensures a predefined maximum peak-to-peak voltage ripple $\Delta V_{\mathrm{dc,pp,max}}$ (i.e., across one DC-link half) can be calculated as

$$C_{\mathrm{dc}} \geq \frac{\Delta Q_{\mathrm{C_{dc},pp,max}}}{\Delta V_{\mathrm{dc,pp,max}}} = \frac{\Delta Q_{\mathrm{m,pp,max}}}{2\,\Delta V_{\mathrm{dc,pp,max}}}, \tag{3.3}$$

where $\Delta Q_{\mathrm{m,pp,max}}$ is the worst-case peak-to-peak DC-link mid-point charge ripple within the considered operating range. Since zero mid-point current modulation (ZMPCPWM) is considered, $\Delta Q_{\mathrm{m,pp,max}} \approx 22.4\,\mathrm{V\,mF}$ is obtained for $M = 0.81$ and $\varphi = 15.5°$ as shown in **Fig. 3.6(b)**. Therefore, assuming $\Delta V_{\mathrm{dc,pp,max}} = 10\,\mathrm{V}$, the minimum required capacitance becomes $C_{\mathrm{dc}} \geq 1120\,\mu\mathrm{F}$.

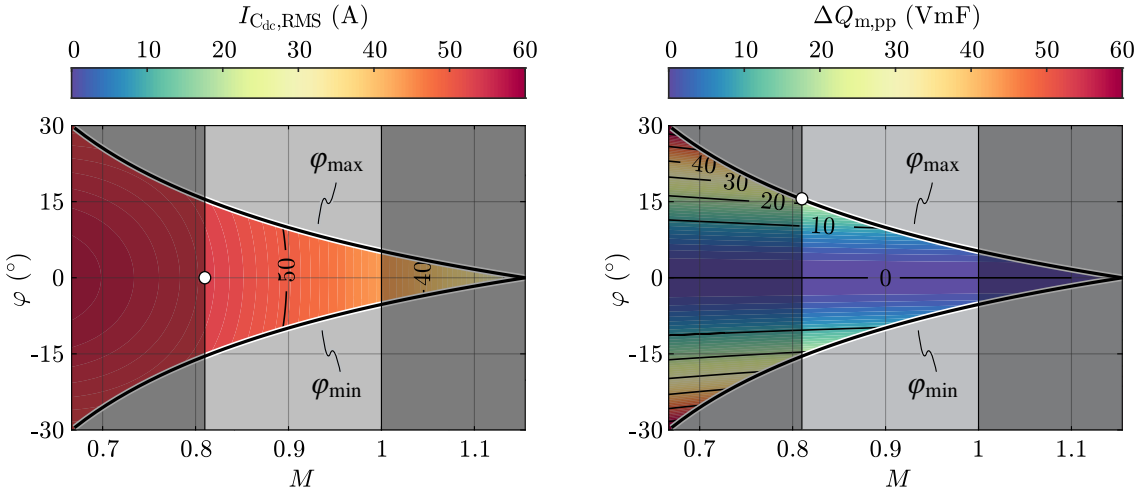


Fig. 3.6: DC-link capacitor **(a)** RMS current stress $I_{\mathrm{C_{dc},RMS}}$ and **(b)** peak-to-peak mid-point charge ripple $\Delta Q_{\mathrm{m,pp}}$ for the considered 60 kW three-phase three-level unidirectional T-type rectifier. The modulation index operating region $0.81 \leq M \leq 1$ is highlighted, the power factor angle limits φ_{max}, φ_{min} are marked and the worst-case operating point is indicated (○).

Due to the considerable capacitance requirement, electrolytic capacitors are employed. In particular, in view of the large DC-link RMS current stress, high-performance capacitors for photovoltaic applications from Vishay-Roederstein (i.e., 259 PHM-SI 450 V series) are selected, due to their large specific current capability. Nonetheless, in the present application the limiting factor for the DC-link capacitor sizing remains the total RMS current stress, leading to the selection of six 680 µF capacitors (i.e., carrying $\approx 9.5\,\mathrm{A}$ with an ambient temperature of 70 °C and a 20 kHz switching frequency) for each DC-link half. This results in a DC-link capacitance value $C_{\mathrm{dc}} = 4080\,\mu\mathrm{F}$, significantly higher than strictly required by the maximum voltage ripple constraint.

To evaluate the impact of the DC-link capacitors on the converter efficiency, the losses induced by the RMS current stress can be estimated as

$$P_{\mathrm{C_{dc}}} \approx 2\,R_{\mathrm{C_{dc}}}\,I^2_{\mathrm{C_{dc},RMS}}, \tag{3.4}$$

where $R_{\mathrm{C_{dc}}}$ is the temperature/frequency-dependent equivalent series resistance of each split DC-link capacitor bank. Since the most significant DC-link current harmonics are located around integer multiples of f_{sw} when adopting ZMPCPWM (i.e., virtually no 150 Hz component flows for $\varphi = 0$), the high-frequency value of $R_{\mathrm{C_{dc}}}$ should be employed for a preliminary estimation of the capacitor losses.

3.2.3 AC-Side Inductors

The design of the rectifier AC-side inductors is of critical importance, as these magnetic components represent a large fraction of the overall system volume and loss. Moreover, the inductance value L affects the phase current peak-to-peak ripple ΔI_{pp} and thus the overall RMS current value processed by the semiconductor devices. Therefore, a maximum 30 % peak-to-peak current ripple constraint is enforced within the optimization procedure, namely $\Delta I_{\mathrm{pp,max}} = 0.3 \cdot I/2 \approx 18.5\,\mathrm{A}$ (i.e., being $I/2$ the peak value of the current flowing through a single inductor). This results in a minimum inductance value $L_{\mathrm{min}} = \Delta\Psi_{\mathrm{pp,max}}/\Delta I_{\mathrm{pp,max}} \approx 117\,\mu\mathrm{H}$, where $\Delta\Psi_{\mathrm{pp,max}} \approx 2.16\,\mathrm{mVs}$ is the maximum peak-to-peak flux ripple adopting ZMPCPWM at $V_{\mathrm{dc}} = 800\,\mathrm{V}$ and $\varphi = 0$ (cf. **Fig. 2.23**).

The adopted inductor optimization routine is illustrated in **Fig. 3.7** and aims to identify the optimal winding arrangement (i.e., number of turns N, wire cross section A_{w}, wire type, etc.) and air gap length l_{g} for a selected core geometry and material, taking into account several design constraints (e.g., core saturation flux density, maximum core/winding temperatures, etc.). In particular, the inductance value L is not fixed and is thus subject to

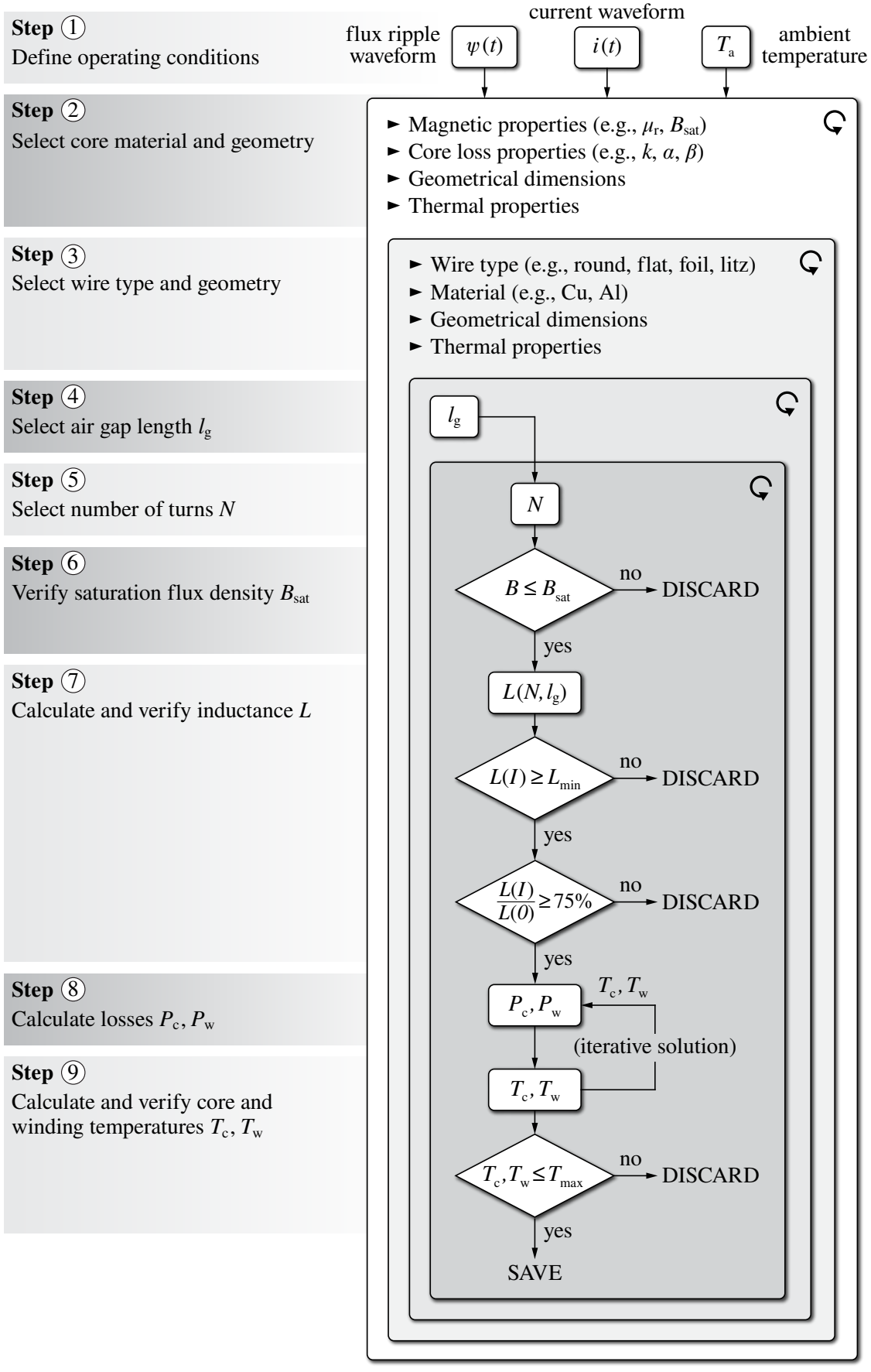


Fig. 3.7: Flowchart of the adopted AC-side inductor design/optimization routine.

the optimization, as each combination of core geometry and material features a different optimal inductance value (e.g., larger cores favor higher inductance values) [61].

In the following, the adopted reluctance model, loss model and thermal model, based on [21, 61, 91, 92], are described.

Reluctance Model

This model allows to accurately estimate the inductance of a certain core/winding configuration by calculating the overall reluctance of magnetic core and air gap (if present).

The core reluctance can be expressed as

$$\mathcal{R}_{\mathrm{c}} = \frac{l_{\mathrm{c}}}{\mu_0 \, \mu_{\mathrm{r}}(B) A_{\mathrm{c}}}, \tag{3.5}$$

where l_{c} is the average core path length, A_{c} is the core cross-sectional area, μ_0 is the vacuum permeability and μ_{r} is the relative permeability of the core material, which depends on the core flux density B.

The air gap reluctance is modeled as

$$\mathcal{R}_{\mathrm{g}} = \frac{l_{\mathrm{g}}}{\mu_0 A_{\mathrm{g}}}, \tag{3.6}$$

where l_{g} is the total air gap length along the flux path and $A_{\mathrm{g}} = k_{\mathrm{g}} A_{\mathrm{c}}$ is the equivalent air gap cross-section. In particular, $k_{\mathrm{g}} \geq 1$ is the air gap fringing factor, obtained with the 3D estimation procedure described in [93].

Therefore, the inductance value is obtained as

$$L = \frac{N^2}{\mathcal{R}_{\mathrm{c}} + \mathcal{R}_{\mathrm{g}}}, \tag{3.7}$$

where N is the winding number of turns.

Loss Model

The inductor losses are divided in two contributions, namely the core loss component and the winding (i.e., ohmic) loss component.

The core losses can be estimated leveraging the improved generalized Steinmetz equation (iGSE) [94] as

$$P_{\mathrm{c}} = \frac{1}{T}\int_0^T k_{\mathrm{i}} \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\,\mathrm{d}t, \tag{3.8}$$

where

$$k_{\mathrm{i}} = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\vartheta|^{\alpha}\,2^{\beta-\alpha}\,\mathrm{d}\vartheta}, \tag{3.9}$$

ΔB is the peak-to-peak flux density ripple within the considered minor-loop and k, α, β are obtained by fitting the specific core losses provided in the manufacturer datasheet (i.e., for sinusoidal excitation) with $k\,f^{\alpha}B^{\beta}$, where B is the sinusoidal peak flux density. The solution of (3.8) for a generic piece-wise linear waveform is obtained with the minor-loop separation approach reported in [61].

The winding losses can be further separated in two components, namely the DC-related losses and the AC-related losses. Even though the considered inductor is only subject to AC current components, the DC winding resistance is calculated as a basis for the AC loss calculation, as

$$R_{\mathrm{dc}} = \frac{l_{\mathrm{w}}}{\sigma(T_{\mathrm{w}})A_{\mathrm{w}}} = \frac{N\,l_{\mathrm{MLT}}}{\sigma(T_{\mathrm{w}})A_{\mathrm{w}}}, \tag{3.10}$$

where l_{w} is the wire length, A_{w} is the wire cross-section, σ is the copper conductivity (i.e., function of the winding temperature T_{w}) and l_{MLT} is the mean length per turn defined by the core geometry. The winding AC resistance is directly obtained by adjusting R_{dc} with two frequency-dependent correction factors F and G, respectively taking into account skin and proximity effects, as

$$R_{\mathrm{ac}} = R_{\mathrm{dc}}\left(2F + 2G\,\frac{H_{\mathrm{w,RMS}}^2}{I^2}\right), \tag{3.11}$$

where $H_{\mathrm{w,RMS}}$ is the spatial RMS magnetic field acting on the winding volume V_{w} [95],

$$H_{\mathrm{w,RMS}} = \sqrt{\frac{1}{V_{\mathrm{w}}}\int_{V_{\mathrm{w}}} H_{\mathrm{w}}^2\,\mathrm{d}V}. \tag{3.12}$$

In particular, the spatial RMS magnetic field can be analytically estimated as in [61]. The expressions of F and G are also reported in [61] for round and foil wire shapes. Nevertheless, the adopted modeling approach has broader applicability, as the rectangular wire can be assumed as a particular case of foil wire with a different aspect ratio, and litz wire can be considered as a particular case of round wire with multiple strands. The

winding losses can therefore be estimated leveraging the harmonic superposition principle:

$$P_{\mathrm{w}} = \frac{1}{2}\sum_{h=0}^{\infty} R_{\mathrm{ac}}(f_{\mathrm{h}})\, I_{\mathrm{h}}^2 = R_{\mathrm{dc}} \sum_{h=0}^{\infty} \left[F(f_{\mathrm{h}}) + G(f_{\mathrm{h}}) \frac{H_{\mathrm{w,RMS}}^2}{I^2} \right] I_{\mathrm{h}}^2 \tag{3.13}$$

where I_{h} is the peak amplitude of the h-th current harmonic and f_{h} is the h-th harmonic frequency.

Thermal Model

The modeling approach adopted herein is described in detail in [92] and is not reported here for reasons of conciseness. It is worth noting that the inductors are designed to be placed in front of the heatsink air stream, therefore they are assumed to be actively cooled (cf. **Fig. 3.11**).

The inputs of the optimization routine are the inductor nominal operating conditions, the complete powder core database from Magnetics (i.e., for the core geometry and material selection) and a customized wire shape and size database (i.e., for the winding design). In particular, powder cores are selected due to their excellent performance in low AC-ripple, high DC-bias applications such as the present one. A large number of designs is assessed by sweeping the values of N and l_{g} for each combination of core geometry/material and wire type/size, and the results are finally filtered according to the following constraints:

- minimum inductance value: $L(I) \geq L_{\mathrm{min}} \approx 117\,\mu\mathrm{H}$;
- maximum inductance drop: $L(I)/L(0) \geq 75\,\%$;
- maximum core flux density: $B \leq B_{\mathrm{sat}}$;
- maximum core/winding temperatures: $T_{\mathrm{c}}, T_{\mathrm{w}} \leq 100\,^{\circ}\mathrm{C}$;

where B_{sat} is the saturation flux density of the selected core material. The results of the optimization procedure are illustrated in **Fig. 3.8(a)**, where the feasible inductor designs are reported in the loss-volume performance space. The final design is selected according to geometrical size considerations, in order to fit the AC-side inductors in front of the semiconductor heatsink, and is schematically illustrated in **Fig. 3.8(b)**. **Fig. 3.8(c)** shows that the inductance value drops from 191 µH in no load conditions to 151 µH at full load (i.e., a 21 % drop).

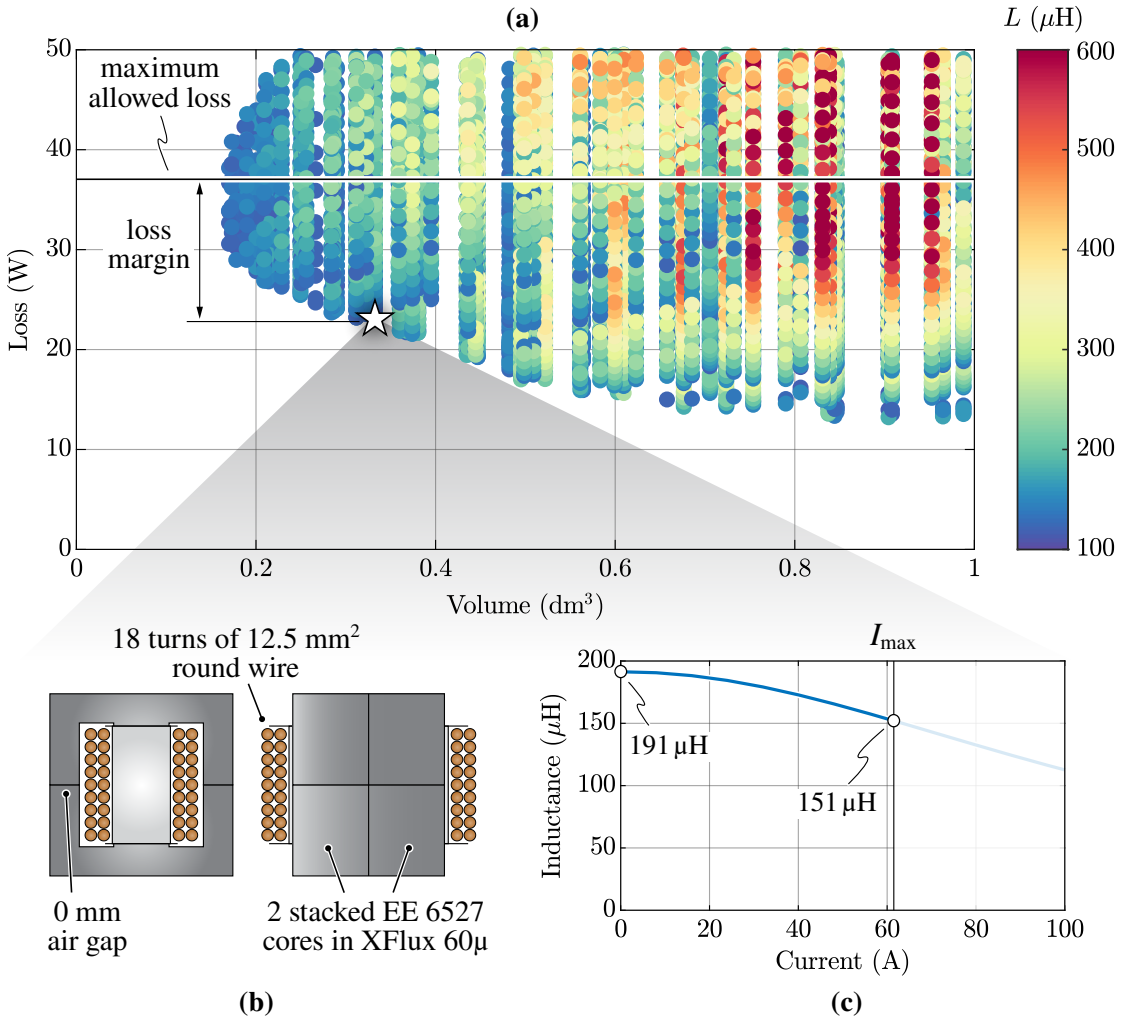


Fig. 3.8: **(a)** loss-volume performance space resulting from the adopted AC-side inductor optimization procedure and **(b)–(c)** highlight of the selected design and its differential inductance value as function of the bias current.

3.2.4 Heat Dissipation System

To dissipate the power losses, the discrete semiconductor devices are connected to a forced air cooled heatsink by means of an electrically insulating, heat conducting thermal interface material (TIM). The thermal equivalent circuit of the adopted setup is illustrated in **Fig. 3.9(a)**, where the ambient temperature T_a, the semiconductor junction temperature T_j, the discrete device case temperature T_c and the heatsink temperature T_{hs} are indicated. The aim of the heat dissipation system is to ensure that the semiconductor junction temperature of all devices complies with the maximum rating (i.e., $T_{j,max} = 150\,°C$ in the present case). Moreover, a lower junction temperature allows for a more efficient operation, due to the positive temperature coefficients of the MOSFET and diode on-state resistances. Therefore,

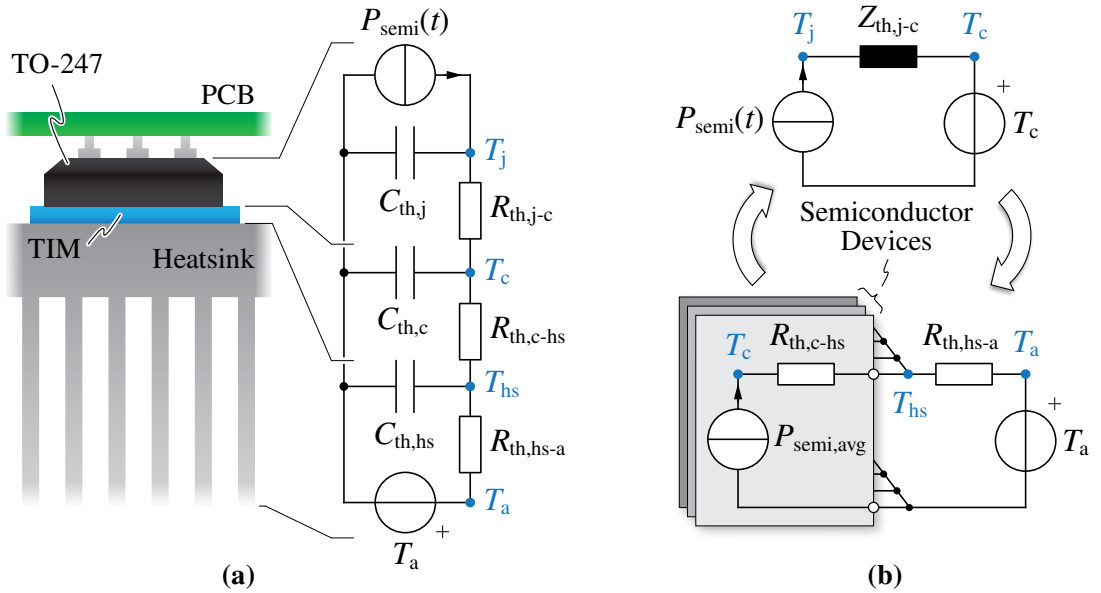


Fig. 3.9: **(a)** Schematic and thermal equivalent circuit of the adopted semiconductor loss dissipation setup and **(b)** simplified equivalent circuits for the estimation of the node temperatures.

the maximum target operating junction temperature is set to 125 °C, ensuring a reasonable temperature margin (i.e., to address modeling errors) and lower semiconductor losses.

Besides the maximum target value of T_j, the heatsink temperature T_{hs} must be limited, as its value affects the temperature of the surrounding components (e.g., PCB, auxiliary circuits, etc.). Therefore, $T_{hs,max} = 70\,°C$ is selected. It is worth noting that the heatsink top surface is assumed to be isothermic (i.e., valid approximation for thick baseplates) and its temperature is determined by the losses of all semiconductor devices, as shown in **Fig. 3.9(b)**. Assuming a maximum ambient (i.e., air) temperature $T_{a,max} = 40\,°C$, the maximum heatsink-to-ambient resistance is calculated as

$$R_{th,hs\text{-}a} \leq \frac{T_{hs,max} - T_{a,max}}{\sum P_{semi,max}} \approx 0.041\,°C/W, \tag{3.14}$$

where $\sum P_{semi,max} \approx 735\,W$ represents the maximum converter semiconductor loss at $T_j = 125\,°C$ and $V_{dc} = 800\,V$ (cf. **Fig. 3.5(a)**).

Due to the large difference in response dynamics (i.e., time constants) between the junction-to-case and case-to-heatsink thermal circuits, the equivalent circuit in **Fig. 3.9(a)** can be simplified as two independent circuits, as illustrated in **Fig. 3.9(b)**. In particular, the junction-to-case thermal circuit features small time constants (i.e., $< 100\,ms$) and is completely defined in the manufacturer datasheet as a Foster-equivalent thermal impedance $Z_{th,j\text{-}c}$. This information can be leveraged to estimate the 50 Hz T_j ripple in the time domain and thus identify the peak T_j value, assuming a constant case temperature T_c. The value

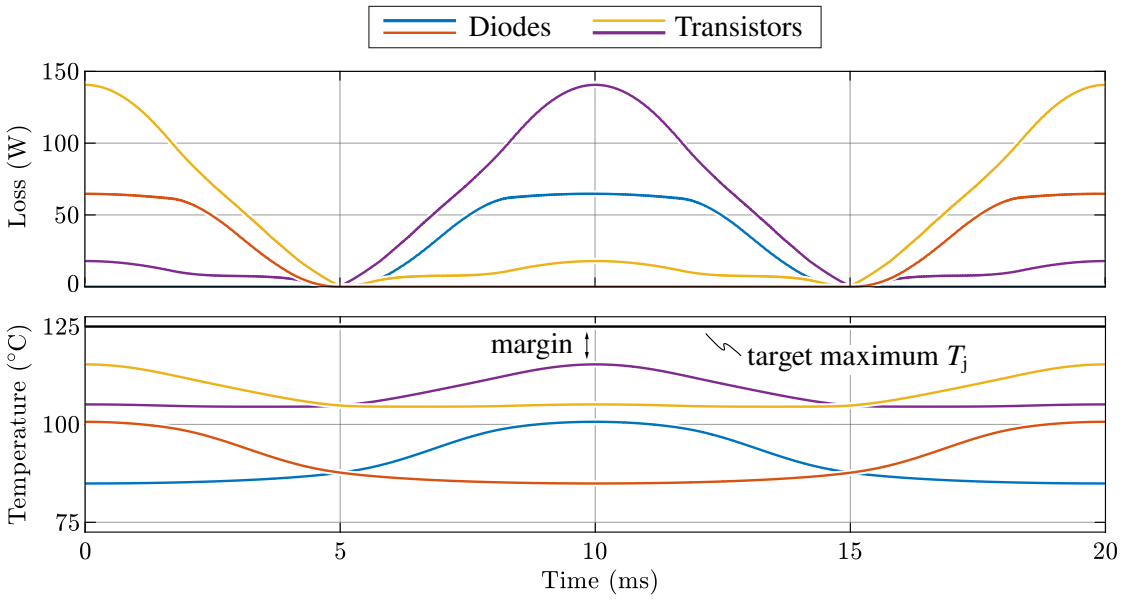


Fig. 3.10: Estimated semiconductor loss and junction temperature of the mid-point transistors (i.e., MOSFETs) and bridge diodes over one grid period, assuming $T_{hs} = T_{hs,max} = 70\,°C$ and $V_{dc} = 800\,V$.

of T_c can then be determined by averaging the semiconductor loss over the fundamental period and evaluating the temperature drop across the case-to-heatsink resistance $R_{th,c\text{-}hs}$ (i.e., the TIM layer), which can be calculated as

$$R_{th,c\text{-}hs} = \frac{r_{th,TIM}}{A_{TO\text{-}247}} \approx 0.675\,°C/W, \tag{3.15}$$

where $r_{th,TIM} \approx 135\,mm^2\,°C/W$ is the specific thermal resistance of the selected TIM (i.e., Bergquist Sil-Pad 1500ST at 100 psi of contact pressure) and $A_{TO\text{-}247} \approx 200\,mm^2$ is the TO-247 thermal interface area. Due to the temperature dependence of semiconductor losses, an iterative procedure is implemented and the worst-case junction temperature (i.e., assuming $T_{hs} = T_{hs,max}$) is calculated for all semiconductor devices, to check the compliance with the desired $T_{j,max}$ value. The results are illustrated in **Fig. 3.10**, which shows that the worst-case peak value of T_j is below $T_{j,max}$ with a margin of 10 °C for the mid-point MOSFETs and 25 °C for the bridge diodes.

Finally, the heatsink and the forced air cooling system (i.e., the fans) are sized to comply with (3.14). The PA8-62 series from MeccAl is selected to size the heatsink, featuring a 62 mm height (i.e., compatible with the AC-side inductor design, cf. **Section 3.2.3**) and a 13.5 mm thick baseplate for enhanced thermal spreading. The width of the heatsink is selected to fit the power PCBs, for a total of 500 mm, while the heatsink length and the fan selection represent the degrees of freedom to achieve the desired value of $R_{th,hs\text{-}a}$. Leveraging the thermal resistance curve as a function of heatsink length and air speed

provided by the heatsink manufacturer, deriving the static pressure drop characteristic of the heatsink according to [96] and combining this information with a database of commercially available fan performance curves, the optimization procedure outlined in [97] is carried out and a Pareto-optimal design (i.e., with respect to volume and fan consumption) is selected. This design features a 100 mm heatsink length and eight 2.9 W 60x25 mm fans from Orion Fans, yielding a thermal resistance value $R_{\text{th,hs-a}} \approx 0.037\,^{\circ}\text{C/W}$ and ensuring a 10 % margin with respect to (3.14).

3.3 Experimental Results

The realized 60 kW three-phase six-leg unidirectional three-level T-type rectifier prototype is illustrated in **Fig. 3.11**. In this section, the converter steady-state operation and loss/efficiency performance are experimentally assessed leveraging the automated test setup shown in **Figure 3.12**. It is worth noting that, even though the rectifier practically consists of two 30 kW three-phase converter units operated in parallel, due to the power limitation of the two electronic loads (i.e., 15 kW each), the experimental tests are limited to a single converter unit. Nonetheless, being the two units identical, all results obtained in the following (e.g., current waveforms, loss, efficiency) can be extended to the whole converter by a two-times rescaling.

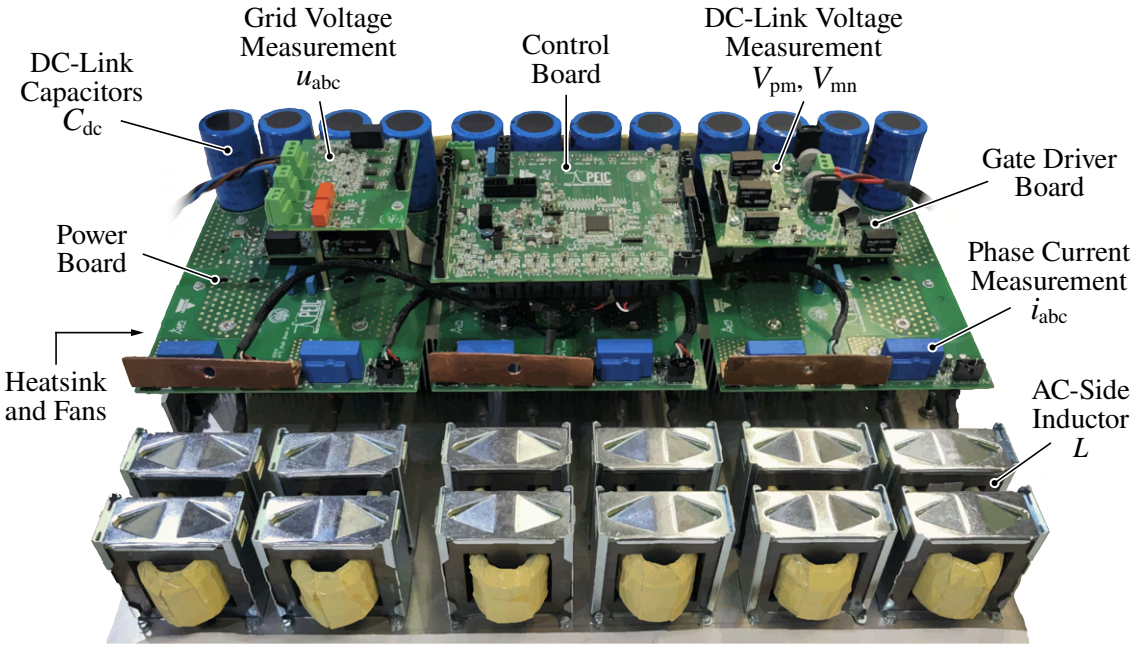


Fig. 3.11: Picture of the 60 kW three-phase six-leg unidirectional three-level T-type rectifier prototype. Due to the maximum power limitation of the available equipment, only one of the two paralleled 30 kW units is exploited for the experimental verification.

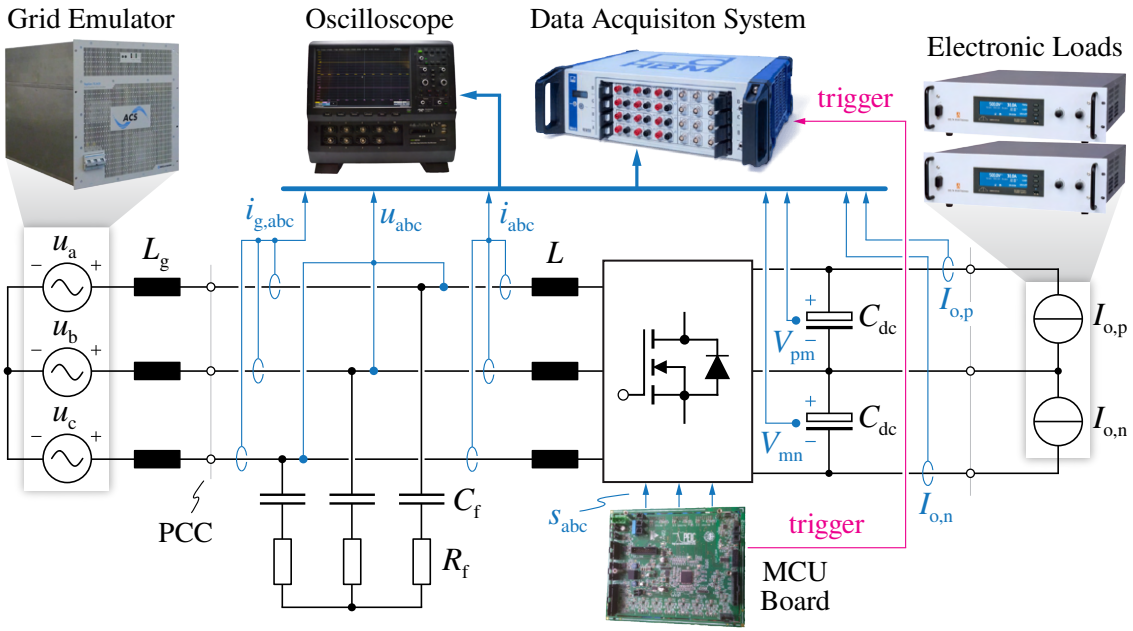


Fig. 3.12: Schematic diagram of the automated test setup used for the characterization of the converter.

At the AC-side, the rectifier is connected to a grid emulator (i.e., emulating the 50 Hz, 400 V European low-voltage grid) by means of an *LCL* filter, which consists of the converter-side inductors (L), filter capacitors ($C_f = 15\,\mu F$) equipped with series damping resistors ($R_f = 0.8\,\Omega$), and grid-side inductors ($L_g = 100\,\mu H$). In general, the goal of the *LCL* filter in a grid-connected rectifier is to eliminate the switching-frequency harmonic content from the grid currents $i_{g,abc}$ [98, 99], so that a lower current total harmonic distortion (THD) is achieved and the converter may comply with grid-code standards [10, 11]. In the present case, the *LCL* filter is specifically employed to isolate the low-frequency component of the distortion (i.e., flowing into the grid), which depends on the converter control, from the switching-frequency one (i.e., flowing into the filter capacitors), which only depends on the selected modulation strategy. This separation allows for a proper assessment of the converter closed-loop control performance in **Chapter 4**. The values of C_f and R_f are selected according to [90], whereas the value of L_g is representative of an equivalent inner grid impedance of ≈ 0.02 pu. On the DC-side, the converter is connected to two independent electronic loads, which emulate the rectifier split DC-link loads. The parameters and component values of the realized three-level T-type rectifier prototype are reported in **Table 3.2**.

Tab. 3.2: Parameters and component values of the realized three-level T-type rectifier prototype.

Parameter	Description	Value
f_{sw}	switching frequency	20 kHz
L	converter-side inductance	151–191 µH
C_f	filter capacitance	15 µF
R_f	filter damping resistance	0.8 Ω
L_g	grid-side inductance	100 µH
C_{dc}	DC-link capacitance	4080 µF

The measurements are performed both with a Teledyne LeCroy 500 MHz, 12-bit, 10 $^{\mathrm{GS}}/_{\mathrm{s}}$, 8-channel oscilloscope, and with an HBM GEN4tB 2 $^{\mathrm{MS}}/_{\mathrm{s}}$ data acquisition system. In particular, the latter approach leverages current and voltage sensors with high rated accuracy (i.e., $< 0.1\,\%$) and is exploited to automatically map the rectifier design-related and control-related performance over its complete operating range. The automated test procedure is managed by the microcontroller unit (MCU), which sets the reference operating point, controls the rectifier and sends the trigger signals to the data acquisition system.

3.3.1 AC-Side Inductor Currents

The AC-side rectifier waveforms in stationary conditions are illustrated in **Fig. 3.13**, where the measured capacitor voltages u_{abc} and inductor currents i_{abc} are shown for different values of transferred power at $V_{\mathrm{dc}} = 800\,\mathrm{V}$. It is observed that the inductor currents are in all cases in phase with the capacitor voltages (i.e., unity power factor operation) and the current quality improves for higher loads. At 10 % of the rated power (cf. **Fig. 3.13(b)**), the large ripple-to-average current ratio and the unidirectional nature of the rectifier lead to pronounced zero-crossing distortion. The current waveform quality improves dramatically at 50 % and 100 % of the rated power (cf. **Fig. 3.13(c)–(d)**), as the relative current ripple decreases and the DCM-related zero-crossing distortion becomes negligible.

3.3.2 DC-Link Mid-Point Current

Both instantaneous and local average values of the DC-link mid-point current i_{m} adopting ZMPCPWM are illustrated in **Fig. 3.14(a)** for $V_{\mathrm{dc}} = 800\,\mathrm{V}$ ($M \approx 0.81$), $\varphi = 0$ and $P = 30\,\mathrm{kW}$. It is observed that, although the instantaneous value of i_{m} jumps between the AC-side inductor current values $\pm i_{\mathrm{a}}$, $\pm i_{\mathrm{b}}$, $\pm i_{\mathrm{c}}$ and 0 (i.e., visible from the current envelopes), the local average value of i_{m} remains approximately 0 along the complete grid period, due to the adopted modulation strategy. A focus of the instantaneous values of i_{a}, i_{b}, i_{c} and i_{m} towards the end of current sector Ⅰ is provided in **Fig. 3.14(b)**, where the mid-point current is shown to jump between $+i_{\mathrm{a}}$ (state 100), $-i_{\mathrm{a}}$ (state 011), $+i_{\mathrm{b}}$ (state 010) and $-i_{\mathrm{c}}$ (state 110), as expected from space vector theory (cf. **Fig. 2.3**).

It is worth noting that the measurement of the instantaneous mid-point current value is not common in literature, as it represents a challenging task to achieve. In practice, the current measurement must be placed within the commutation loop of all bridge-legs, thus negatively affecting the switching performance of the rectifier. In the present case, the measurement of i_{m} has been achieved by placing the current probe between the bridge-leg decoupling capacitors (i.e., 220 nF ceramic capacitors) and the DC-link capacitors (i.e., 4080 µF electrolytic capacitors), as schematically illustrated in **Fig. 3.15**. Even

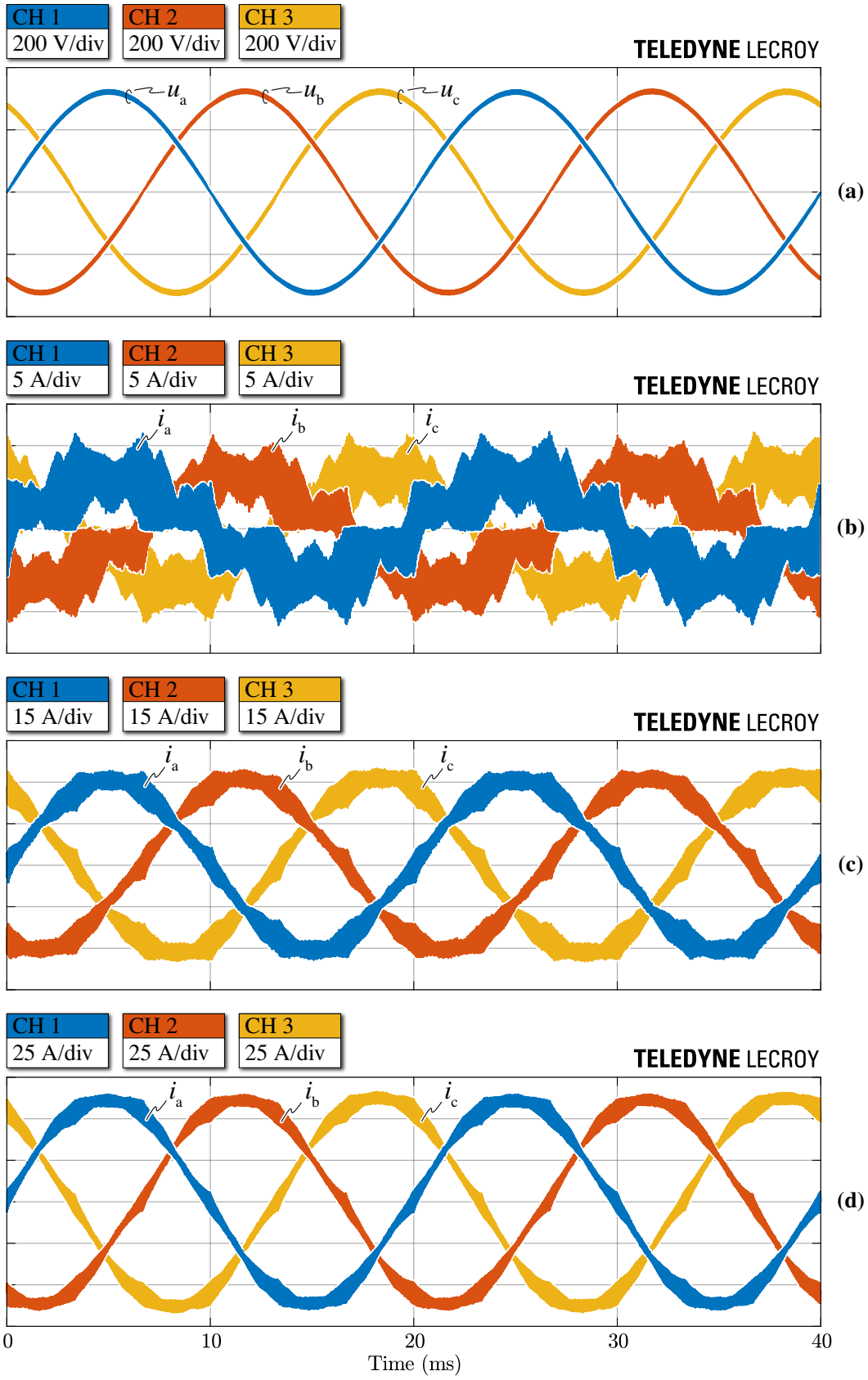


Fig. 3.13: Experimental **(a)** capacitor voltage waveforms u_{abc} and **(b)–(d)** inductor current waveforms i_{abc} in steady-state conditions with ZMPCPWM, $V_{dc} = 800\,\text{V}$ and $\varphi = 0$ at **(b)** 10 %, **(c)** 50 % and **(d)** 100 % of the nominal power (i.e., $P = 30\,\text{kW}$).

though the decoupling capacitors are placed in parallel to the DC-link capacitors, their small capacitance value does not substantially affect the mid-point current, especially considering the relatively low switching frequency of the rectifier.

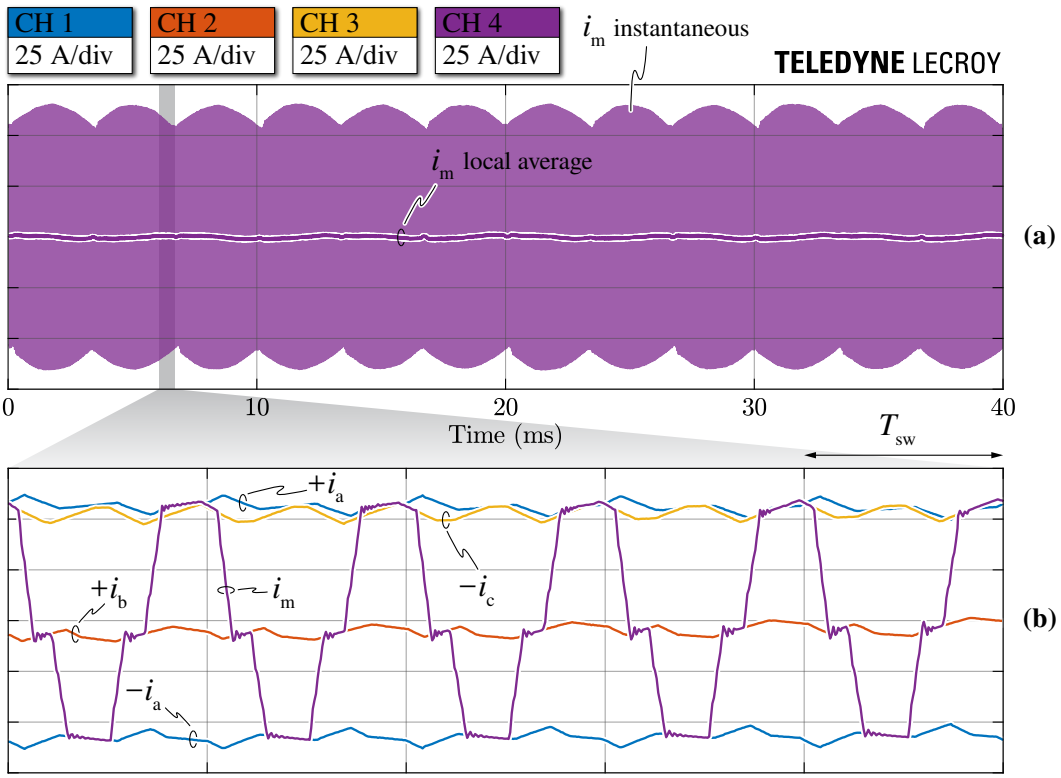


Fig. 3.14: **(a)** experimental waveforms of the mid-point current i_m instantaneous and local average values in steady-state conditions with ZMPCPWM, $V_{dc} = 800\,V$, $\varphi = 0$ and $P = 30\,kW$. **(b)** focus of the instantaneous mid-point current waveform at the end of current sector Ⓘ (cf. **Fig. 2.3**), with highlight of the AC-side inductor current values $\pm i_a$, $+i_b$, $-i_c$.

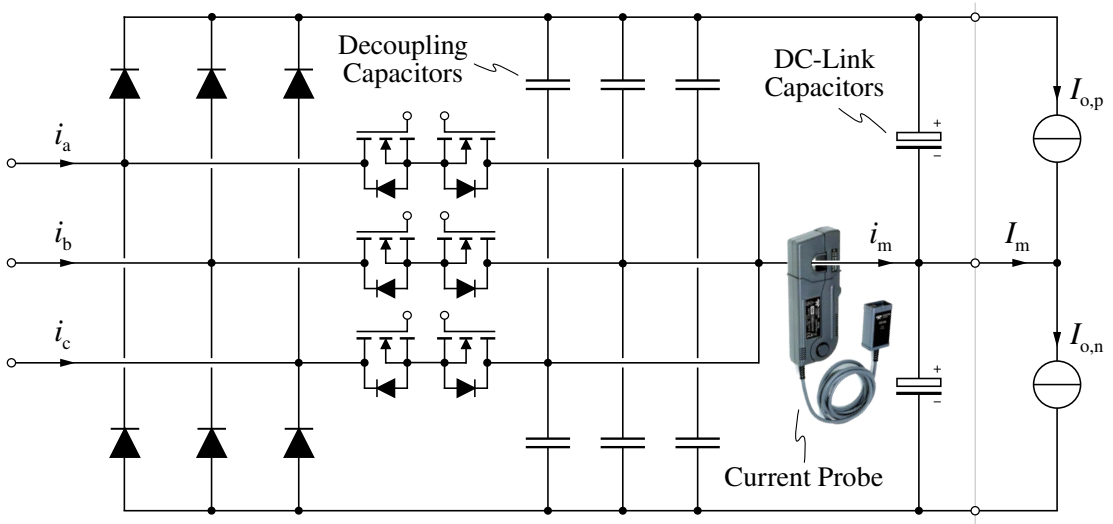


Fig. 3.15: Schematic diagram of the DC-link mid-point current i_m measurement setup. The current probe is placed between the bridge-leg decoupling capacitors and the DC-link capacitors.

3.3.3 Loss and Efficiency

To obtain the converter loss and efficiency, the AC input power $P_\mathrm{i} = u_\mathrm{a}\, i_\mathrm{a} + u_\mathrm{b}\, i_\mathrm{b} + u_\mathrm{c}\, i_\mathrm{c}$ and the DC output power $P_\mathrm{o} = V_\mathrm{pm}\, I_\mathrm{o,p} + V_\mathrm{mn}\, I_\mathrm{o,n}$ are measured with the automated test setup of **Fig. 3.12** and are then averaged over ten grid periods (i.e., 200 ms).

The rectifier loss (i.e., $P_\mathrm{i} - P_\mathrm{o}$) and efficiency (i.e., $P_\mathrm{o}/P_\mathrm{i}$) are shown for $V_\mathrm{dc} = 650\,\mathrm{V}$ and $V_\mathrm{dc} = 800\,\mathrm{V}$ in **Fig. 3.16**, where they are compared to the analytical/numerical estimations based on the models presented in **Section 3.2**. It is observed that the converter features $\geq 98.5\,\%$ efficiency at $V_\mathrm{dc} = 650\,\mathrm{V}$ (i.e., nominal conditions) for all power levels greater than 20 % of the rated power, satisfying the initial design target (cf. **Tab. 3.1**). Moreover, a peak efficiency value of 98.8 % is achieved. At $V_\mathrm{dc} = 800\,\mathrm{V}$ a lower efficiency is obtained, as the losses in all components increase (i.e., higher RMS current in the DC-link capacitors, higher flux ripple in the inductors and higher semiconductor switched voltage. Overall, excellent agreement is observed between the analytical/numerical estimations and the experimental results, thus supporting the validity of the proposed design procedure and the accuracy of the adopted loss models.

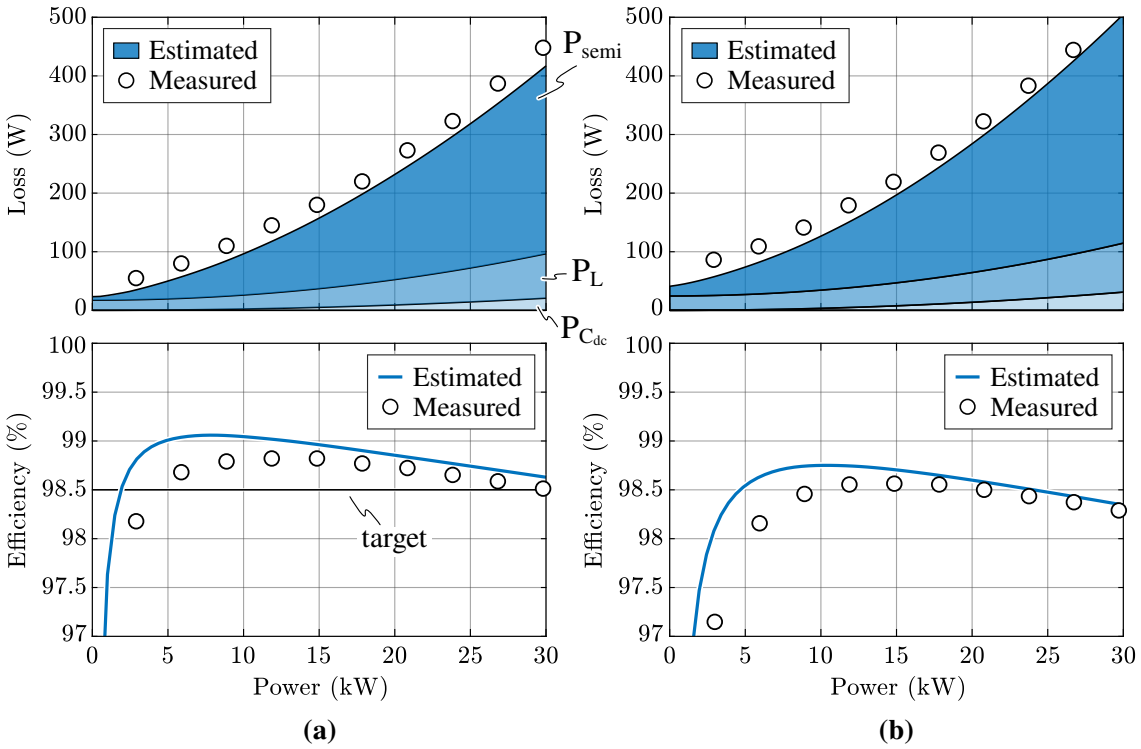


Fig. 3.16: Comparison between estimated and measured converter losses and efficiency as functions of the DC output power of a single converter unit for **(a)** $V_\mathrm{dc} = 650\,\mathrm{V}$ (i.e., nominal conditions) and **(b)** $V_\mathrm{dc} = 800\,\mathrm{V}$. The estimated losses are separated into DC-link capacitor loss ($P_{\mathrm{C_{dc}}}$), AC-side inductor loss (P_L) and semiconductor loss (P_semi).

3.4 Summary

This chapter has presented a complete design methodology for the AC/DC converter stage of the considered 60 kW electric vehicle (EV) ultra-fast battery charger. A unidirectional three-level T-type converter topology has been selected and, in view of the high target nominal power, a six-leg (i.e., dual three-phase) converter structure has been adopted, halving the current rating of each bridge-leg and thus allowing for the adoption of discrete Si semiconductor devices (i.e., MOSFETs and diodes). Therefore, a step-by-step converter design procedure has been proposed, describing the selection, sizing and/or optimization of all main converter active and passive components, including the semiconductor devices, the DC-link capacitors, the AC-side inductors and the heat dissipation system (i.e., heatsink and fans). Furthermore, the adopted models for the estimation of the component losses have been reported. Finally, a 60 kW AC/DC converter prototype has been built and its performance in terms of loss and efficiency has been assessed experimentally, successfully achieving the required 98.5 % efficiency in nominal operating conditions. The validity of the proposed design procedure and the adopted loss models has been supported by the excellent agreement between analytical/numerical estimations and experimental results.

Chapter 4

AC/DC Converter – Control

Abstract

The AC/DC converter stage of an electric vehicle (EV) ultra-fast battery charger must ensure sinusoidal input current shaping with low harmonic content, fast control dynamics and strong disturbance rejection capability (i.e., as the following DC/DC stage may act as a fast-varying and/or unbalanced load). The unidirectional nature of the considered three-phase three-level rectifier negatively affects its steady-state operation, e.g., distorting the input currents around the zero-crossings, limiting the feasible power factor angle and reducing the maximum DC-link mid-point current (i.e., the ability to work with unbalanced split DC-link loading). In particular, the rectifier operation under non-unity power factor and/or under unbalanced loading (i.e., with constant zero-sequence voltage injection) typically yields large and uncontrolled input current distortion, effectively limiting the acceptable operating region of the converter. Although high bandwidth current controllers and enhanced phase current sampling strategies may improve the rectifier input current distortion, especially at light load, these approaches lose effectiveness when significant phase-shift between voltage and current is required and/or a constant zero-sequence voltage must be injected. Therefore, this chapter focuses on the design, tuning and experimental assessment of a high-performance digital multi-loop control strategy for the considered three-level unidirectional T-type rectifier, aiming at minimum phase current distortion under all operating conditions (e.g., non-unity power factor, unbalanced split DC-link loading), fast response dynamics and strong disturbance rejection. To accurately design the four control loops (i.e., dq-currents, DC-link voltage, DC-link mid-point voltage deviation), the system state-space equations are described and the small-signal model of the three-level rectifier is derived. The controllers are then tuned leveraging analytical expressions, taking into account the delays and the discretization introduced by the digital control implementation. Finally, the steady-state and dynamical performance of the proposed multi-loop control strategy is verified in circuit simulation and experimentally on the T-type rectifier prototype, adopting a general purpose microcontroller unit (MCU) for the digital control implementation.

4.1 Introduction

The digital control of power converters has recently become an industry standard, mainly due to the advent of modern, powerful, reliable and low-cost digital signal processors (DSPs). The well-known benefits of digital controllers reside in excellent reproducibility, noise immunity and flexibility, allowing for the implementation of complex control strategies [100]. Despite these advantages, the digital control implementation is also affected by limited computational capabilities and sampling, quantization and zero-order hold (ZOH) effects that may negatively impact the control performance and must therefore be taken into account during the controller design.

The control requirements of the considered unidirectional three-level rectifier can be summarized in

- sinusoidal input current shaping, with low total harmonic distortion (THD);
- regulation of the DC-link voltage according to the desired reference value (i.e., determined by the DC/DC stage, cf. **Chapter 6**) and strong disturbance rejection against load steps;
- limited steady-state and dynamical DC-link mid-point voltage deviation, even under unbalanced split DC-link loading (i.e., as separate DC/DC units are connected to the two DC-link halves, cf. **Section 1.3**);
- operation under non-unity power factor, either to compensate the reactive power introduced by the filter capacitors (cf. **Fig. 3.12**) or to support the reactive energy flows in distribution grids [13].

All of these tasks require a proper converter control strategy with adequate dynamical performance, which is therefore the subject of this chapter. In particular, the operation of unidirectional rectifiers under non-unity power factor has not been well explored in literature and is increasingly becoming a desired feature of modern rectifiers, as distribution system operators (DSOs) are starting to charge end consumers for the injection/withdrawal of reactive energy into/from the grid [101]. If properly controlled, existing unidirectional rectifiers could in fact actively compensate this reactive power excess and/or substitute traditional power factor correction capacitor banks, benefiting the DSO and improving the system power quality.

The main challenges in achieving the mentioned control requirements are mostly related to the unidirectional nature of three-level rectifiers. One major issue is the discontinuous conduction mode (DCM) operation of the converter around the current zero-crossings,

which, if not correctly addressed, can lead to unacceptable phase current distortion in light load conditions [54]. Moreover, unidirectional rectifiers are characterized by narrower power factor angle operating limits and lower DC-link mid-point current generation capability with respect to their three-level bidirectional counterparts. In particular, the rectifier operation under non-unity power factor and/or under split DC-link load unbalance (i.e., requiring constant zero-sequence voltage injection [55]) typically yields large and uncontrolled input current distortion, as reported in several past works [73, 102–106], thus practically limiting even further the acceptable operating region of the converter. Although high current control loop bandwidth and enhanced phase current sampling strategies may improve the rectifier input current distortion, especially in light load conditions, these approaches are not sufficient to ensure low current distortion when significant voltage-to-current phase-shift and/or zero-sequence voltage injection are required.

Mainly because of the aforementioned reason, several papers dealing with the analysis and the control of three-level unidirectional rectifiers under diverse operating conditions have been published in the literature [52, 55, 57, 60, 61, 66, 73, 75, 102–108]. Nevertheless, a simple, clear and exhaustive control loop design and tuning procedure, taking into account the converter zero-sequence voltage and mid-point current limits, has not been provided [109]. Moreover, a complete analysis of the effects of non-unity power factor operation and constant zero-sequence voltage injection (i.e., operation under unbalanced split DC-link loading) is still missing [58]. In particular, no simple and unified carrier-based PWM approach ensuring undistorted operation of unidirectional rectifiers across their entire operating region has been proposed and verified experimentally.

Therefore, this chapter describes in detail the design, tuning, simulation and experimental verification of the adopted three-level rectifier multi-loop control strategy, providing and assessing a straightforward design procedure of all controllers. In particular, leveraging the zero-sequence voltage limits derived in **Section 2.2.2** and applying them within the modulator, a unified carrier-based PWM approach is proposed, ensuring undistorted operation of the rectifier in every feasible operating condition (i.e., for variable power factor and unbalanced split DC-link loading). Furthermore, the fast response dynamics and the strong disturbance rejection capability of the control loops are ensured by proper feedforward contributions, open-loop gain adaptations and high control bandwidths.

Part of the content of this chapter has been published in [110], [109] and [58].

4.2 System Small-Signal Model

The small-signal model of the system is of primary importance for the proper design of the closed loop control (cf. **Section 4.3**) and is therefore derived in this section. As previously outlined in Section 2.2, the considered system consists of a unidirectional three-level rectifier connected to the three-phase grid (i.e., three sinusoidal voltage sources) supplying two independent loads (i.e., equivalent current sources), as illustrated in **Fig. 2.2**. Even though the T-type converter topology is specifically selected in the present work, the following considerations remain valid for all unidirectional three-level topologies with a split DC-link (cf. **Fig. 2.1**). Furthermore, to simplify the analysis, no inner grid impedance and no AC-side filter are considered: both elements do not affect the general control considerations of this work, particularly when the voltage across the AC filter capacitors is fed forward within the current controllers (cf. **Section 4.3.1**) and/or the AC-side filter is properly damped [90, 98, 99].

The converter passive components define the system state-variables, namely the AC-side inductor currents i_a, i_b, i_c and the DC-link capacitor voltages V_pm and V_mn. In particular, the three-wire nature of the system (i.e., lacking the neutral conductor) implies $i_\mathrm{a}+i_\mathrm{b}+i_\mathrm{c}=0$ as in (2.1), such that only two inductor currents are independent. Moreover, V_pm and V_mn can be rearranged to obtain the total DC-link voltage $V_\mathrm{dc}=V_\mathrm{pm}+V_\mathrm{mn}$ and the DC-link mid-point voltage deviation $V_\mathrm{m}=V_\mathrm{pm}-V_\mathrm{mn}$ as in (2.2)–(2.3).

With the adoption of a dq reference frame synchronized with the grid voltage vector $\vec{U}$ (i.e., in the direction of the d-axis), the system state-space equations can be expressed in a compact form, as

$$\begin{cases} L\dfrac{\mathrm{d}I_\mathrm{d}}{\mathrm{d}t}=U-V_\mathrm{d}+\omega L I_\mathrm{q} & (4.1)\\ L\dfrac{\mathrm{d}I_\mathrm{q}}{\mathrm{d}t}=-V_\mathrm{q}-\omega L I_\mathrm{d} & (4.2)\\ \dfrac{C_\mathrm{dc}}{2}\dfrac{\mathrm{d}V_\mathrm{dc}}{\mathrm{d}t}=\dfrac{I_\mathrm{p}-I_\mathrm{n}}{2}-\dfrac{I_\mathrm{o,p}+I_\mathrm{o,n}}{2} & (4.3)\\ C_\mathrm{dc}\dfrac{\mathrm{d}V_\mathrm{m}}{\mathrm{d}t}=-I_\mathrm{m}-(I_\mathrm{o,p}-I_\mathrm{o,n}) & (4.4) \end{cases}$$

where U is the grid phase voltage peak, $\omega=2\pi f$ is the grid frequency, I_p, I_m, I_n are the periodical averages of the DC-link rail currents (with $I_\mathrm{p}+I_\mathrm{m}+I_\mathrm{n}=0$), $I_\mathrm{o,p}$, $I_\mathrm{o,n}$ are the split DC-link load currents and I_d, I_q, V_d, V_q are respectively the phase currents and phase voltages applied by the rectifier in the dq reference frame. The derived state-space equations can be expressed with an equivalent circuit representation, as illustrated in **Fig. 4.1**. In order to solve the fourth order state-space system (4.1)–(4.4), the relationship between the DC-side currents I_p, I_m, I_n and the state variables must be identified.

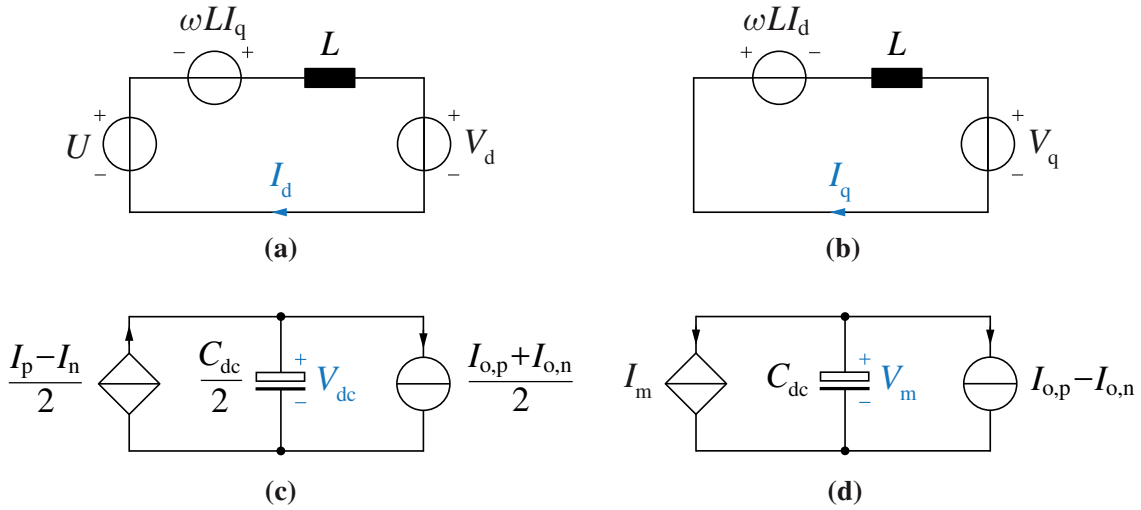


Fig. 4.1: Equivalent circuit representation of the system state-space equations: **(a)** d-axis current, **(b)** q-axis current, **(c)** DC-link voltage, and **(d)** DC-link mid-point voltage deviation.

Assuming balanced DC-link voltages (i.e., $V_{\mathrm{pm}} = V_{\mathrm{mn}} = V_{\mathrm{dc}}/2$), a first relation between AC-side and DC-side quantities is obtained leveraging the input/output power balance as in (2.12). The DC-link voltage state-space equation can therefore be expressed as

$$\frac{C_{\mathrm{dc}}}{2}\frac{\mathrm{d}V_{\mathrm{dc}}}{\mathrm{d}t} = \frac{3}{2}\frac{V_{\mathrm{d}}I_{\mathrm{d}} + V_{\mathrm{q}}I_{\mathrm{q}}}{V_{\mathrm{dc}}} - \frac{I_{\mathrm{o,p}} + I_{\mathrm{o,n}}}{2} = \frac{3}{2}\frac{U\,I_{\mathrm{d}}}{V_{\mathrm{dc}}} - \frac{I_{\mathrm{o,p}} + I_{\mathrm{o,n}}}{2}, \tag{4.5}$$

which is non-linear with respect to V_{dc}.

A second relation between AC-side and DC-side quantities can be derived leveraging the mid-point current i_{m} generation process, described in detail in **Section 2.2.1**. By averaging the value of i_{m} over one-third of the fundamental period (i.e., the DC-side current periodicity), expression (2.19) is derived, linking the zero-sequence voltage v_{o} injection level to the mid-point current periodical average I_{m}. Furthermore, subdividing v_{o} into a periodic component $v_{\mathrm{o,3}}$ with three-times the grid frequency, representative of the selected modulation strategy (cf. **Section 2.3**), and a DC component $V_{\mathrm{o},\delta}$ reserved for control purposes, the following expression of I_{m} is obtained from (2.19):

$$I_{\mathrm{m}} = -\frac{3}{\pi V_{\mathrm{dc}}}\int_{0}^{2\pi/3}\left[v_{\mathrm{o,3}}\sum_{\mathrm{x=a,b,c}}|i_{\mathrm{x}}| + V_{\mathrm{o},\delta}\sum_{\mathrm{x=a,b,c}}|i_{\mathrm{x}}|\right]\mathrm{d}\vartheta. \tag{4.6}$$

Since the first term is characterized by a $2\pi/3$ periodicity, its integral is null, therefore I_{m} can be expressed as

$$I_{\mathrm{m}} = -\frac{3}{\pi V_{\mathrm{dc}}}\int_{0}^{2\pi/3} V_{\mathrm{o},\delta}\sum_{\mathrm{x=a,b,c}}|i_{\mathrm{x}}|\,\mathrm{d}\vartheta. \tag{4.7}$$

This equation can be used to estimate the effect of a constant $V_{o,\delta}$ contribution (i.e., added to all phase voltage references) on the generated average mid-point current. However, the solution of (4.7) is not straightforward, as the instantaneous zero-sequence voltage $v_o = v_{o,3} + V_{o,\delta}$ is dynamically limited with a $2\pi/3$ periodicity (cf. **Section 2.2.2**), directly affecting the applied $V_{o,\delta}$. Nonetheless, even though $v_{o,max}$ and $v_{o,min}$ modify the shape of the applied $V_{o,\delta}$ (i.e., effectively reducing its average value) a simple expression of I_m can be obtained by neglecting the zero-sequence voltage limits and solving (4.7):

$$I_m \approx -\frac{12}{\pi}\frac{I_d}{V_{dc}} V_{o,\delta}. \tag{4.8}$$

It is worth noting that this expression overestimates the mid-point current value, particularly for high values of $V_{o,\delta}/V_{dc}$, as shown in **Fig. 4.2**. Nevertheless, (4.8) sets an upper limit for $I_m(V_{o,\delta})$, which is of practical interest in ensuring the stability of the mid-point voltage control loop. The state-space equation of the DC-link mid-point voltage deviation V_m can therefore be expressed as

$$C_{dc}\frac{dV_m}{dt} = \frac{12}{\pi}\frac{I_d}{V_{dc}} V_{o,\delta} - (I_{o,p} - I_{o,n}), \tag{4.9}$$

which is the last equation required to solve system (4.1)–(4.4).

Fig. 4.2 also shows that the $I_m(V_{o,\delta})$ relation depends on the adopted modulation strategy, as the shape of $v_{o,3}$ affects the mid-point current generation. Nonetheless, the maximum mid-point current periodical average $I_{m,max}$ (i.e., the maximum split DC-link load unbalance that can be tolerated by the rectifier) only depends on the modulation index M and the power factor angle φ, as explained in **Section 2.2.5**.

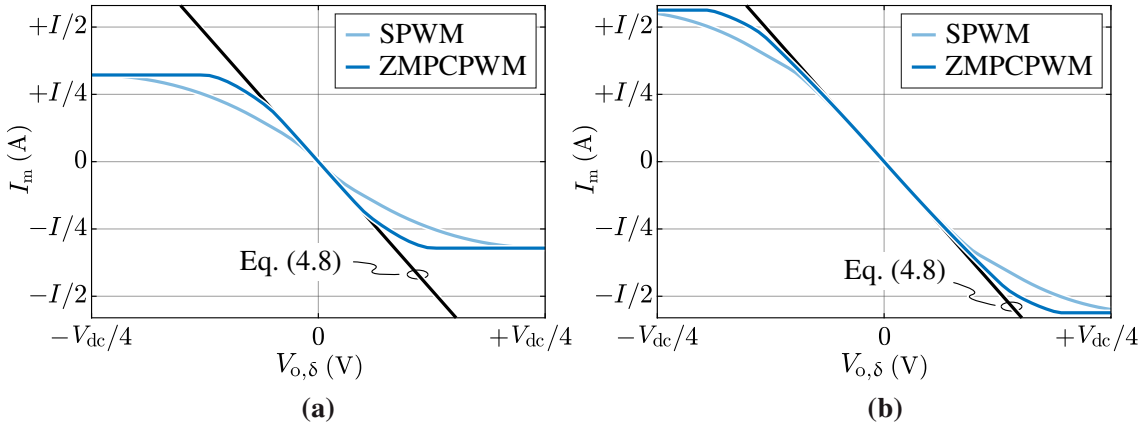


Fig. 4.2: Mid-point current periodical average I_m as function of the zero-sequence voltage injection $V_{o,\delta}$ for **(a)** $V_{dc} = 650\,V$ (i.e., $M \approx 1.0$) and **(b)** $V_{dc} = 800\,V$ (i.e., $M \approx 0.81$). The results obtained with SPWM and ZMPCPWM are compared to (4.8).

4.3 Controller Design

The three-level rectifier is controlled by means of a cascaded multi-loop structure consisting of four loops, which correspond to the state-space variables in (4.1)–(4.4), namely the DC-link voltage loop, the mid-point voltage balancing loop and the phase current loops in the dq frame, as illustrated in **Fig. 4.3**.

A conventional voltage-oriented control is adopted [99, 111, 112], where the grid synchronization is obtained with a phase-locked loop (PLL) [113, 114], aligning the d-axis of the rotating dq frame with the phase voltage vector $\vec{U}$ measured at the point of common coupling (PCC). The outer V_{dc} loop is responsible for controlling the DC-link capacitor voltage according to the reference value required by the DC/DC stage, ensuring the power balance between the grid and the load. As a consequence, the output of this controller is the d-axis current reference I_d^* (i.e., responsible for the power transfer), whereas the q-axis current reference I_q^* is typically controlled to compensate the reactive power injected by the filter capacitors C_f (cf. **Fig. 3.12**) to ensure unity power factor operation at the PCC. Nonetheless, I_q^* can be set to any value that complies with the converter-side power factor angle limitations of the rectifier (cf. **Section 2.2.4**), being $\varphi = \tan^{-1}(I_q/I_d)$. Finally, the role of the V_m loop is to control the mid-point voltage deviation to zero, thus ensuring the voltage balance between the two series-connected DC-link capacitors (i.e., $V_{pm} \approx V_{mn} \approx V_{dc}/2$). The V_m loop operates in parallel to the cascaded V_{dc}, I_{dq} loops (i.e.,

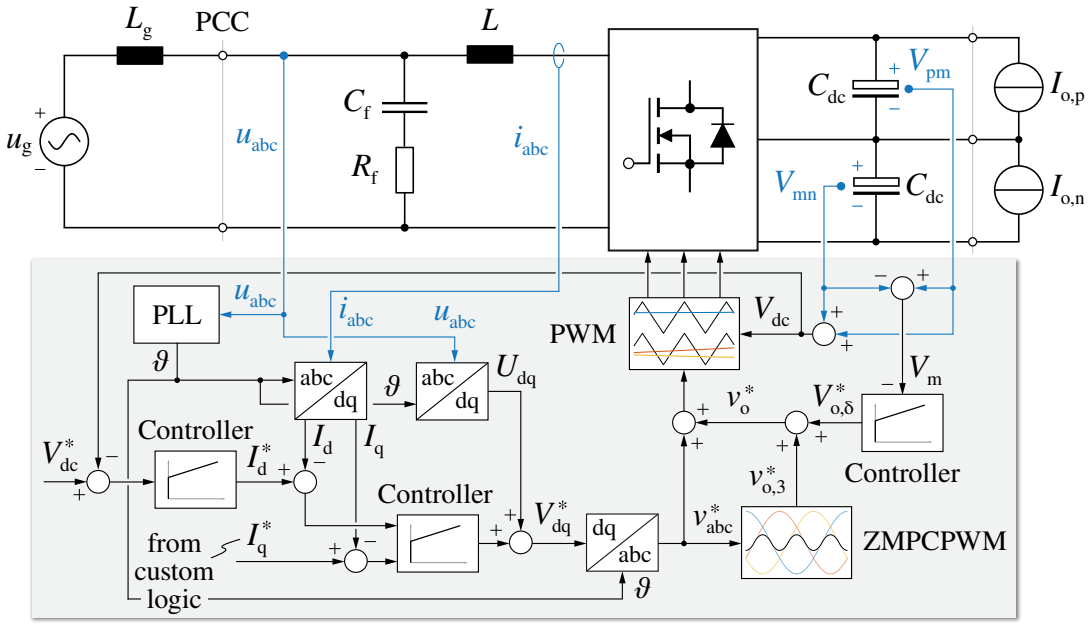


Fig. 4.3: Simplified control diagram of the three-level rectifier, including the dq current I_{dq}, DC-link voltage V_{dc} and mid-point voltage V_m controllers. Detailed schematics of the control loops are provided in **Fig. 4.4**, **Fig. 4.5** and **Fig. 4.6**, respectively.

without interference), since it acts on the zero-sequence voltage injection, which does not affect the phase currents and thus the overall power transfer (cf. **Section 2.2.1**). It is worth highlighting that the V_{m} loop acts on the mid-point current I_{m} generation process and thus allows for the operation of the rectifier with a certain degree of load unbalance between the two DC-link halves, being $I_{\mathrm{m}} = I_{\mathrm{o,n}} - I_{\mathrm{o,p}}$ in steady-state.

4.3.1 dq Current Control Loops

The current control is implemented in the rotating dq frame to achieve zero steady-state tracking error with a simple proportional-integral (PI) regulator and maximize the disturbance rejection performance of the control loops. The measured PCC voltages u_{abc} (cf. **Figure 4.3**) are fed into the PLL, achieving the reference frame synchronization with the grid (i.e., angle ϑ). Even though only two-phase currents are independent, all three of them are measured for redundancy reasons, enhancing the measurement offset and gain compensations. The d-axis reference current I_{d}^{*} (i.e., responsible for the active power transfer) is provided by the DC-link voltage control loop, whereas the q-axis reference I_{q}^{*} (i.e., regulating the reactive power generation) can be set to any value that complies with the converter-side power factor angle limitations of the rectifier (cf. **Section 2.2.4**). The detailed schematic diagram of the closed-loop current control in the dq frame is illustrated in **Fig. 4.4**.

Due to the unidirectional nature of the rectifier, the phase currents encounter discontinuous conduction mode (DCM) operation around the current zero-crossings [54]. In particular, DCM operation poses two major control challenges, which may lead to steady-state and dynamical issues, if not properly addressed. First, conventional synchronous/asynchronous sampling does not provide the average phase current value under

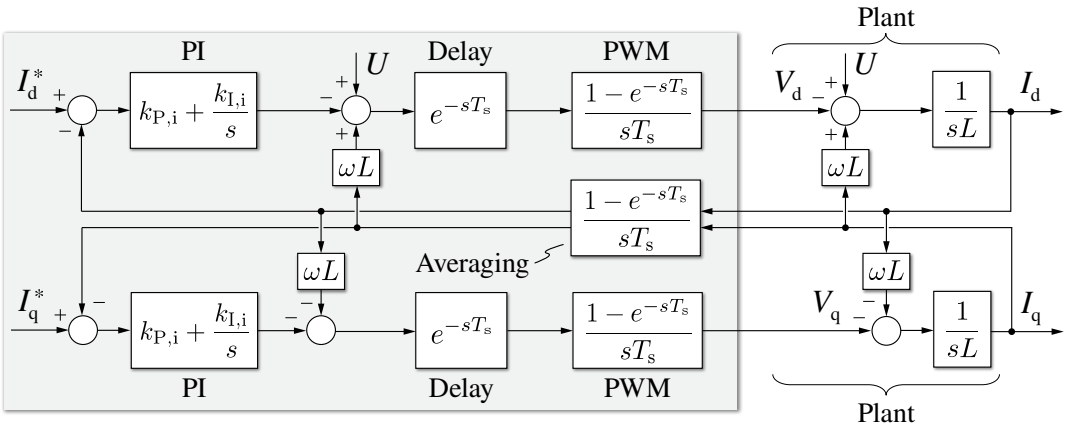


Fig. 4.4: Detailed block diagram of the I_{d} and I_{q} current control loops.

DCM conditions, due to the discontinuous nature of the current ripple [115]. This may lead to noticeable current distortion around the zero crossings, due to the variable current feedback error. The second challenge is represented by the system transfer function (i.e., duty-to-current) becoming non-linear in DCM and thus translating in a variable open-loop gain [115]. The gain is typically much lower than in continuous conduction mode (CCM) and thus reduces the control-loop bandwidth, inevitably leading to additional input current distortion. In the present case, the first issue is tackled by oversampling the measured currents and averaging the sampled values, thus obtaining a moving average of the phase currents, whereas the second issue is not directly addressed. Nonetheless, the effects of the system gain drop in DCM are limited by maximizing both the control bandwidth and the low-frequency open-loop gain (i.e., by means of the integral part of the PI regulator).

The digital implementation of the current control loop introduces three main delay components, which negatively affect the achievable control bandwidth and/or decrease the closed loop stability margin [116, 117]. The current oversampling and averaging process introduces the first delay component, i.e., a moving average delay of $T_\mathrm{s}/2$ (where T_s is the sampling/control period). The second delay contribution is related to the digital processing, which yields a pure delay of one sampling period T_s between the measured quantities and the control signal output. Finally, the PWM modulator introduces a zero-order hold (ZOH) effect of one sampling period, which may be treated as a $T_\mathrm{s}/2$ delay if the control bandwidth is sufficiently lower than the Nyquist frequency. Overall, the total resulting delay of $2T_\mathrm{s}$ can be expressed with the transfer function:

$$G_{\mathrm{d,i}}(s) = e^{-s\,2T_\mathrm{s}} \approx \frac{1 - s\,T_\mathrm{s}}{1 + s\,T_\mathrm{s}}, \tag{4.10}$$

where the exponential term is rationalized with a first-order Padè approximation. In this work, the digital sampling and update process is performed once per switching period (i.e., $f_\mathrm{s} = f_\mathrm{sw} = 20\,\mathrm{kHz}$).

The voltage-to-current plant transfer functions in the dq frame can be derived from (4.1), (4.2) by disregarding the disturbance components (i.e., easily compensated by suitable feed-forward terms) as

$$G_{\mathrm{p,i}}(s) = \frac{I_\mathrm{d}(s)}{V_\mathrm{d}(s)} = \frac{I_\mathrm{q}(s)}{V_\mathrm{q}(s)} = \frac{1}{s\,L}. \tag{4.11}$$

The integral nature of the plant allows for a zero steady-state tracking error with a proportional regulator. Nevertheless, a PI controller is adopted to achieve better disturbance rejection performance and higher low-frequency open-loop gain, especially required to counteract the DCM-induced distortion around the current zero-crossings. Therefore, the

controller transfer function is

$$G_{\mathrm{c,i}}(s) = k_{\mathrm{P,i}} + \frac{k_{\mathrm{I,i}}}{s}, \tag{4.12}$$

where $k_{\mathrm{P,i}}$ and $k_{\mathrm{I,i}}$ are the proportional and integral coefficients of the regulator, respectively.

To improve the dynamical performance of the control loops and ensure the small-signal operation of the PI regulator, the PCC voltages and the current cross-coupling terms are fed forward (cf. **Fig. 4.4**). The open-loop control transfer function is therefore:

$$G_{\mathrm{ol,i}}(s) = G_{\mathrm{d,i}}(s)\, G_{\mathrm{p,i}}(s)\, G_{\mathrm{c,i}}(s). \tag{4.13}$$

Since simplified rational transfer functions have been derived for every component of $G_{\mathrm{ol,i}}(s)$, the tuning of the PI regulator can be performed in the continuous time domain leveraging conventional techniques. Therefore, the PI coefficients can be directly set to achieve the desired value of open-loop 0 dB cross-over frequency $\omega_{\mathrm{c,i}}$, substituting (4.10)–(4.12) into (4.13) and setting $|G_{\mathrm{ol,i}}(j\omega_{\mathrm{c,i}})| = 1$. Being k_{z} the ratio between the PI zero $\omega_{\mathrm{z,i}} = k_{\mathrm{I,i}}/k_{\mathrm{P,i}}$ and $\omega_{\mathrm{c,i}}$, if $\omega_{\mathrm{z,i}}$ is located sufficiently below $\omega_{\mathrm{c,i}}$ (i.e., $k_{\mathrm{z}} \ll 1$), the following approximate relations hold:

$$\begin{cases} k_{\mathrm{P,i}} = \omega_{\mathrm{c,i}} L \dfrac{1}{\sqrt{1+k_{\mathrm{z}}^2}} \overset{k_{\mathrm{z}} \ll 1}{\approx} \omega_{\mathrm{c,i}} L \\ k_{\mathrm{I,i}} = \omega_{\mathrm{z,i}}\, k_{\mathrm{P,i}} \end{cases}. \tag{4.14}$$

In the present case, the tuning of the PI coefficients is performed with a phase margin criterion, therefore $\omega_{\mathrm{c,i}}$ is expressed as function of the desired phase margin in radians m_φ by solving $\underline{/G_{\mathrm{ol,i}}(j\omega_{\mathrm{c,i}})} = -\pi + m_\varphi$:

$$\omega_{\mathrm{c,i}} = \frac{1}{T_{\mathrm{s}}} \frac{\sqrt{\left[1+k_{\mathrm{z}}^2\right]\left[1+\tan^2\left(m_\varphi\right)\right]} - k_{\mathrm{z}} - \tan\left(m_\varphi\right)}{1 - k_{\mathrm{z}} \tan\left(m_\varphi\right)} \tag{4.15}$$

Therefore, when $k_{\mathrm{z}} \ll 1$ the following approximate relation is obtained:

$$\omega_{\mathrm{c,i}} \overset{k_{\mathrm{z}} \ll 1}{\approx} \frac{1}{T_{\mathrm{s}}} \left[-\tan(m_\varphi) + \sqrt{1+\tan^2(m_\varphi)} \right]. \tag{4.16}$$

In this work, $m_\varphi = 60^\circ$ and $k_{\mathrm{z}} = 1/5$ are considered, ensuring a good compromise among reference tracking speed, step response overshoot and disturbance rejection capability. For the system considered herein (i.e., with $f_{\mathrm{s}} = 20\,\mathrm{kHz}$, $T_{\mathrm{s}} = 50\,\mu\mathrm{s}$), an open-loop cross-over frequency $f_{\mathrm{c,i}} \approx 850\,\mathrm{Hz}$ is obtained.

It is worth mentioning that, since soft-saturating powder core inductors have been adopted for the experimental prototype (cf. **Section 3.2.3**), the worst-case value of L must be considered to calculate $k_{\mathrm{P,i}}$ and $k_{\mathrm{I,i}}$ in (4.14), corresponding to the minimum inductance value at the nominal peak current (i.e., $L = 151\,\mu\mathrm{H}$ at $I = 61.5\,\mathrm{A}$). This approach ensures that the minimum phase margin is never exceeded, however it does not compensate for the differential inductance variation, leading to variable control bandwidth along the grid fundamental period (i.e., depending on the instantaneous phase current value) and lower dynamical performance at low current levels. Another possible approach would be to control the three phase currents in the abc stationary frame and compensate for the phase inductance variation with three independent time-varying open-loop gain adjustments, as in [118]. Nevertheless, this approach lacks the benefits related to the dq frame current control implementation (e.g., ideally zero steady-state reference-tracking error) and is therefore not adopted in this work.

4.3.2 DC-Link Voltage Control Loop

In general, the DC-link voltage controller of an active rectifier is responsible to adjust the active power absorbed from the grid to balance the power absorbed from the load. In the present case, the load is represented by the isolated DC/DC stage of the ultra-fast battery charger, and the DC-link voltage reference V_{dc}^{*} is set according to the strategy reported in **Section 7.5** (i.e., to narrow the design/operating range of the DC/DC converter). To regulate the DC-link voltage, the control loop acts on the d-axis current reference I_{d}^{*}, which directly adjusts the active power transfer. Assuming the DC-side load currents $I_{\mathrm{o,p}}$, $I_{\mathrm{o,n}}$ as disturbance components, the current-to-voltage plant transfer function is obtained from (4.5) as

$$G_{\mathrm{p,v}}(s) = \frac{V_{\mathrm{dc}}(s)}{I_{\mathrm{d}}(s)} = \frac{3}{2}\,\frac{U}{V_{\mathrm{dc}}}\,\frac{2}{sC_{\mathrm{dc}}}. \tag{4.17}$$

The DC-link voltage control loop is illustrated in **Fig. 4.5** and consists of a PI regulator, an optional feed-forward contribution, two gain adjustment blocks, the current control loop and the plant transfer function.

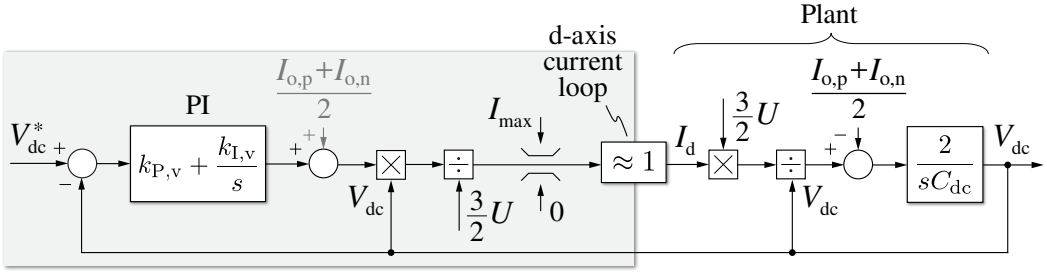


Fig. 4.5: Detailed block diagram of the V_{dc} voltage control loop.

Even though the plant has an integral behavior, a PI regulator is selected to improve the load disturbance rejection capabilities of the control loop. Therefore, the controller transfer function is

$$G_{\mathrm{c,v}}(s) = k_{\mathrm{P,v}} + \frac{k_{\mathrm{I,v}}}{s}, \tag{4.18}$$

where $k_{\mathrm{P,v}}$ and $k_{\mathrm{I,v}}$ are the proportional and integral coefficients of the regulator, respectively.

As the power absorbed by the DC/DC stage is generally known with reasonable accuracy (i.e., the reference charging power), $I_{\mathrm{o,p}}$ and $I_{\mathrm{o,n}}$ can easily be estimated and their values can be fed forward (cf. **Fig. 4.5**) to unburden the integral part of the PI regulator.

The plant non-linearity in (4.17) is compensated by multiplying the regulator output with the measured DC-link voltage V_{dc}. Moreover, the controller gain is adapted to compensate for the dependence of the plant transfer function on the grid phase voltage peak U.

The output of the regulator (i.e., after the gain adjustments) is limited between 0 and the maximum phase current value $I_{\max} = 61.5\,\mathrm{A}$, becoming the reference setpoint for the d-axis current control loop. Since this loop is characterized by much faster dynamics with respect to the voltage control one, the current loop can be considered as an ideal actuator (i.e., a unity gain block). Therefore, the V_{dc} control open-loop transfer function can be expressed as

$$G_{\mathrm{ol,v}}(s) = \frac{2}{3}\frac{V_{\mathrm{dc}}}{U} G_{\mathrm{p,v}}(s)\, G_{\mathrm{c,v}}(s). \tag{4.19}$$

The tuning of the PI regulator is performed assuming that the open-loop 0 dB cross-over frequency of the voltage control loop $\omega_{\mathrm{c,v}}$ is set sufficiently below the current control loop one $\omega_{\mathrm{c,i}}$. With this assumption, the inner loop does not dynamically affect the outer one (i.e., unity-gain block approximation). Therefore, the PI coefficients can be obtained substituting (4.17)–(4.18) into (4.19) and setting $|G_{\mathrm{ol,v}}(j\omega_{\mathrm{c,v}})| = 1$, leading to simple tuning expressions:

$$\begin{cases} k_{\mathrm{P,v}} \approx \omega_{\mathrm{c,v}} \dfrac{C_{\mathrm{dc}}}{2} \\ k_{\mathrm{I,v}} = \omega_{\mathrm{z,v}}\, k_{\mathrm{P,v}} \end{cases}. \tag{4.20}$$

In this work, $\omega_{\mathrm{c,v}}$ is set to $\omega_{\mathrm{c,i}}/10$, resulting in an open-loop cross-over frequency $f_{\mathrm{c,v}} \approx 85\,\mathrm{Hz}$. Moreover, the PI zero $\omega_{\mathrm{z,v}} = k_{\mathrm{I,v}}/k_{\mathrm{P,v}}$ is set to $\omega_{\mathrm{c,v}}/2$, to maximize the disturbance rejection capabilities of the control loop.

4.3.3 DC-Link Mid-Point Voltage Balancing Loop

Since three-level rectifiers are characterized by a split DC-link (cf. **Fig. 2.2**), a voltage unbalance between the upper and lower capacitors may either appear under normal operating conditions, due to device and/or control non-idealities, or under unbalanced load conditions (i.e., $I_{\mathrm{o,p}} \neq I_{\mathrm{o,n}}$). In particular, steady-state and/or dynamical load unbalances can appear in battery charging applications when separate DC/DC units are connected to the two DC-link halves, as in the present case (cf. **Section 1.3**). In all cases, the closed-loop control of the DC-link mid-point voltage deviation V_{m} is required, both to limit the voltage stress on the semiconductor devices to $V_{\mathrm{dc}}/2$ and to ensure the symmetry between the AC-side voltages applied by the rectifier during the positive and negative grid half-cycles.

The control of V_{m} is achieved by acting on the zero-sequence voltage injection level $V_{\mathrm{o},\delta}$ to vary the mid-point current periodical average I_{m}, as explained in **Section 2.2.5** and **Section 4.2**. Since the zero-sequence voltage does not affect the AC-side currents, and thus the active power transfer, the V_{m} control loop does not directly interfere with the other closed-loop controllers. The plant transfer function is therefore obtained from (4.9), by considering the DC-side load currents $I_{\mathrm{o,p}}$, $I_{\mathrm{o,n}}$ as disturbance components:

$$G_{\mathrm{p,b}}(s) = \frac{V_{\mathrm{m}}(s)}{V_{\mathrm{o},\delta}(s)} = -\frac{12}{\pi}\frac{I_{\mathrm{d}}}{V_{\mathrm{dc}}}\frac{1}{sC_{\mathrm{dc}}}. \tag{4.21}$$

The DC-link mid-point voltage balancing loop is illustrated in **Fig. 4.6** and consists of a moving average filter (MAF), a PI regulator, two gain adjustment blocks, the zero-sequence voltage saturation and the plant transfer function.

The DC-link mid-point voltage deviation is obtained by the V_{pm}, V_{mn} measurements and is passed through a MAF running at three times the grid frequency, to prevent any feedback of the 150 Hz voltage oscillation (i.e., also present with ZMPCPWM when $\varphi \neq 0$,

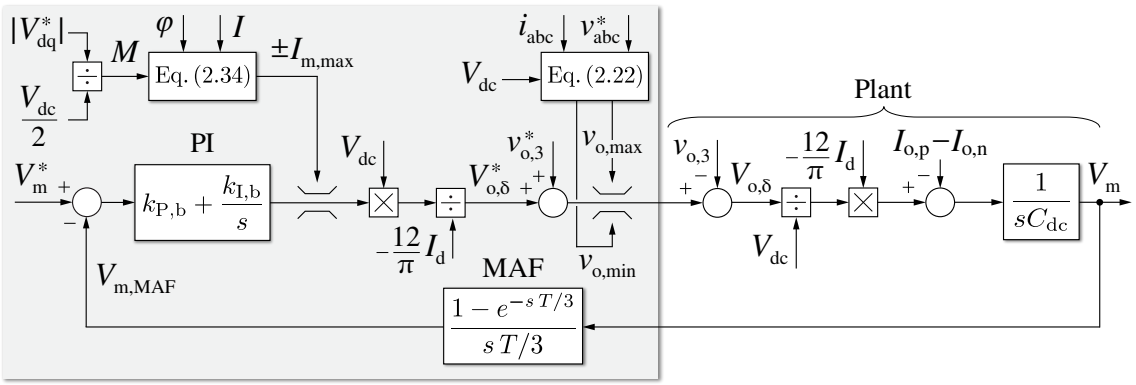


Fig. 4.6: Detailed block diagram of the V_{m} voltage control loop.

cf. **Fig. 2.18**). Therefore, V_{m} is sampled at the sampling frequency $f_{\mathrm{s}} = 20\,\mathrm{kHz}$ and averaged with three times the grid periodicity, introducing a moving average delay of $T/6$, where $T = 1/f$ is the grid fundamental period. The resulting delay transfer function is therefore expressed as

$$G_{\mathrm{d,b}}(s) = \frac{1 - e^{-sT/3}}{sT/3} \approx e^{-sT/6} \approx \frac{1 - sT/12}{1 + sT/12}. \tag{4.22}$$

Also for this control loop, a PI regulator is adopted to enhance the disturbance rejection capabilities:

$$G_{\mathrm{c,b}}(s) = k_{\mathrm{P,b}} + \frac{k_{\mathrm{I,b}}}{s} \tag{4.23}$$

where $k_{\mathrm{P,b}}$ and $k_{\mathrm{I,b}}$ are the proportional and integral coefficients of the regulator, respectively.

The output of the regulator, corresponding to the desired mid-point current reference, is saturated according to the minimum/maximum mid-point current limits $I_{\mathrm{m,max/min}}(M, \varphi)$ expressed by (2.34). In this way, a successful anti-wind-up scheme can be implemented, so that the integral action of the regulator is stopped once the current limits are hit.

Since the plant transfer function $G_{\mathrm{p,b}}(s)$ depends on other state variables (i.e., I_{d}, V_{dc}), these are actively compensated by adjusting the open loop gain with the measured quantities. In this way, consistent controller dynamics are maintained for all operating conditions.

Finally, the resulting zero-sequence voltage reference $V^*_{\mathrm{o},\delta}$ is added to $v_{\mathrm{o},3}$ (i.e., defined by selected modulation strategy) and is then saturated according to the upper and lower zero-sequence voltage limits $v_{\mathrm{o,max/min}}$ reported in (2.22). This saturation process is of extreme importance, as a large input current distortion would arise without it (cf. **Section 4.5**).

Overall, the V_{m} open-loop control transfer function is expressed by

$$G_{\mathrm{ol,b}}(s) = -\frac{\pi}{12}\frac{V_{\mathrm{dc}}}{I_{\mathrm{d}}} G_{\mathrm{d,b}}(s)\, G_{\mathrm{p,b}}(s)\, G_{\mathrm{c,b}}(s). \tag{4.24}$$

To prevent dynamical interference with the MAF, the DC-link mid-point voltage balancing loop 0 dB cross-over frequency $\omega_{\mathrm{c,b}}$ is set one decade lower than $3f$ (i.e., $f_{\mathrm{c,b}} \approx 15\,\mathrm{Hz}$). The PI regulator coefficients are thus obtained as

$$\begin{cases} k_{\mathrm{P,b}} \approx \omega_{\mathrm{c,b}} C_{\mathrm{dc}} \\ k_{\mathrm{I,b}} = \omega_{\mathrm{z,b}} k_{\mathrm{P,b}} \end{cases}, \tag{4.25}$$

where the PI zero $\omega_{\mathrm{z,b}} = k_{\mathrm{I,b}}/k_{\mathrm{P,b}}$ is set to $\omega_{\mathrm{c,b}}/2$.

4.4 Simulation Results

The converter small-signal behavior is verified in circuit simulation, where the proposed control strategy is implemented by means of a custom C-code script in PLECS environment. To accurately simulate the discretized nature of the digital system, the control execution is triggered once every control period $T_s = 50\,\mu s$ (i.e., $f_s = 20\,kHz$), while the control outputs are updated at the following trigger instant. Furthermore, the current oversampling and averaging process is performed with 32 samples per control period.

Several simulations are performed by setting sinusoidal references with different frequencies at the input of each control loop, measuring the system response and calculating its magnitude and phase. In particular, to comply with the unidirectional nature of the rectifier, a DC offset is added to the dq current references.

The simulation results, expressed as magnitude/phase Bode plots of the open-loop and closed-loop transfer functions, are reported in **Fig. 4.7–4.9** and compared to their corresponding analytical expressions derived in **Sections 4.3.1–4.3.3**. It is observed that the simplified analytical models show a high-level of correspondence with circuit simulations over the complete control bandwidth, demonstrating the validity and accuracy of the proposed controller design/tuning procedure.

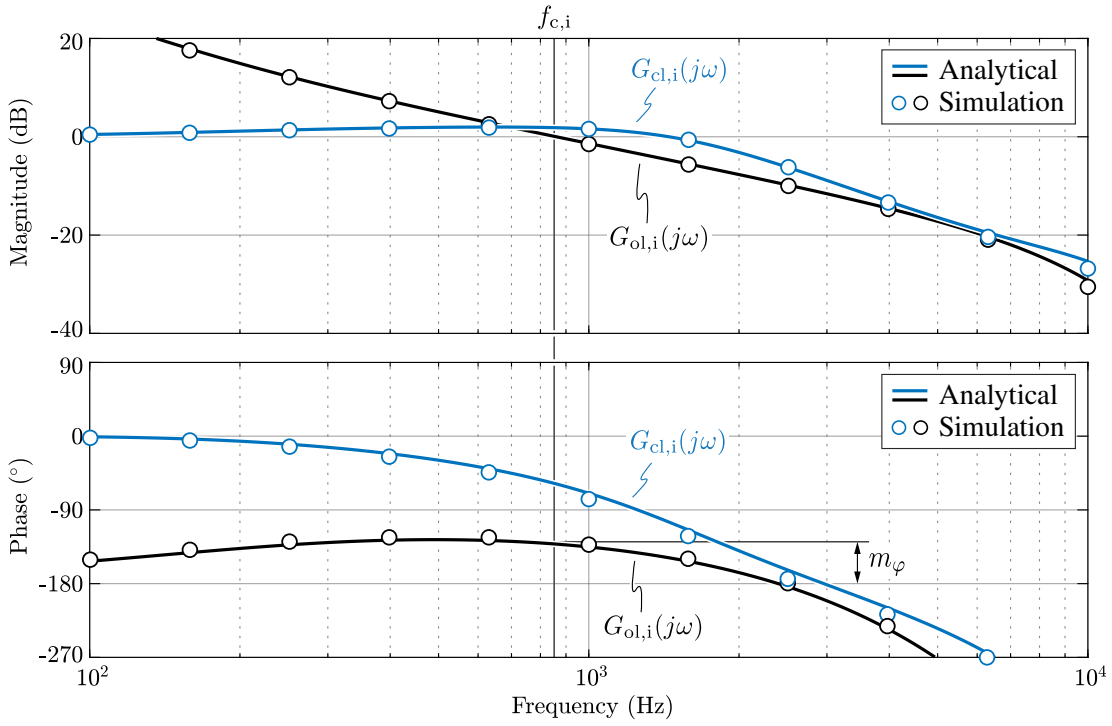


Fig. 4.7: Comparison between analytically derived and simulated dq axis current I_{dq} control open-loop transfer function $G_{ol,i}$ and closed-loop transfer function $G_{cl,i}$.

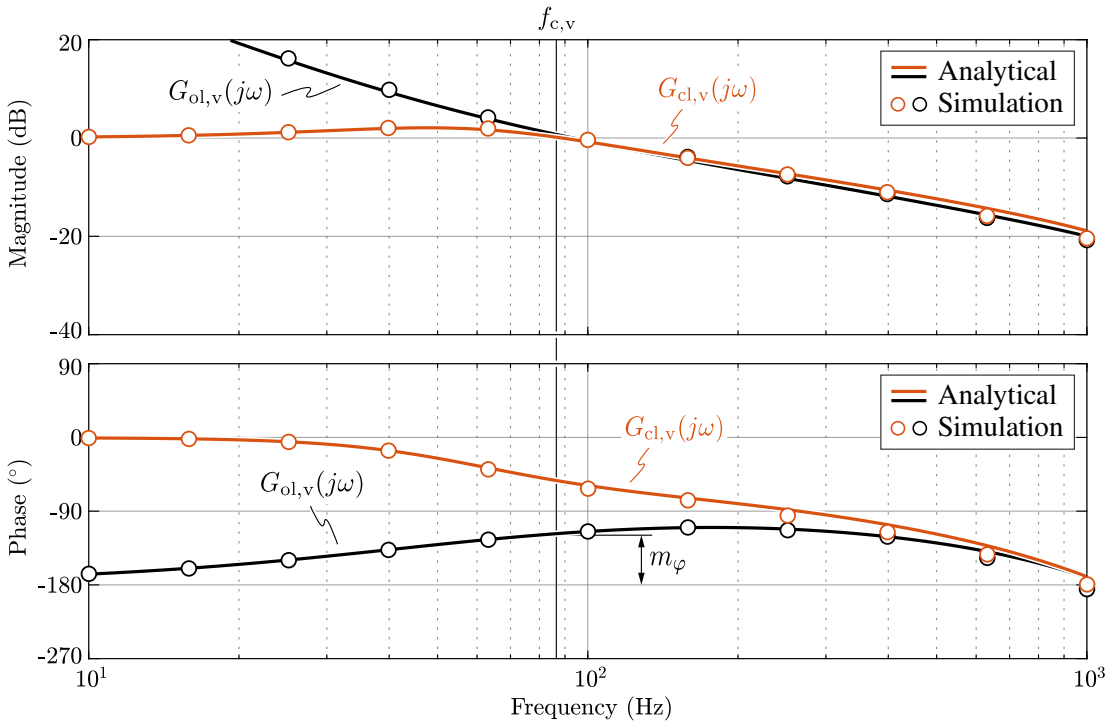


Fig. 4.8: Comparison between analytically derived and simulated DC-link voltage V_{dc} control open-loop transfer function $G_{ol,v}$ and closed-loop transfer function $G_{cl,v}$.

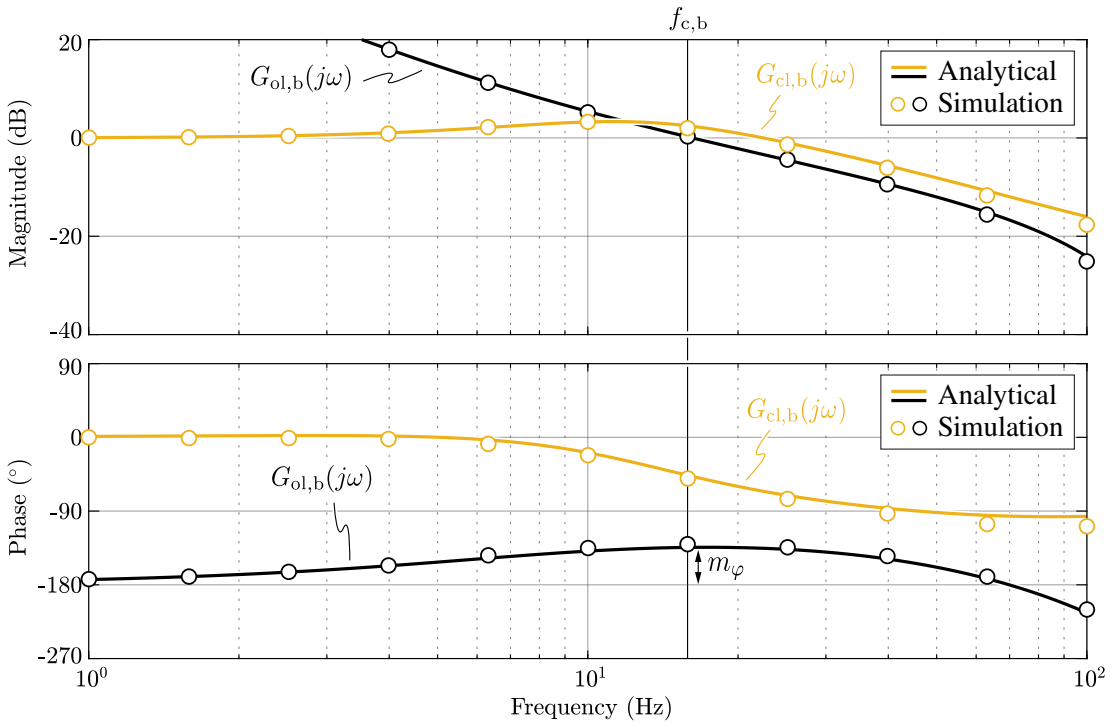


Fig. 4.9: Comparison between analytically derived and simulated DC-link mid-point voltage deviation V_m control open-loop transfer function $G_{ol,b}$ and closed-loop transfer function $G_{cl,b}$.

4.5 Experimental Results

The steady-state and dynamical performance of the proposed control strategy are verified experimentally on the T-type rectifier prototype shown in **Fig. 3.11**, leveraging the test setup illustrated in **Fig. 3.12** with the parameters reported in **Table 3.2**. As in **Section 3.3**, the experimental tests are limited to a single 30 kW three-phase converter unit due to the power limitation of the two electronic loads (i.e., 15 kW each). The complete converter multi-loop control is implemented on a STM32G474VE MCU from ST Microelectronics with an interrupt service routine running at $f_s = 20\,\text{kHz}$.

In this section, the rectifier closed-loop control performance is assessed both in steady-state (i.e., current THD, grid-side displacement power factor, mid-point current capability) and in dynamical conditions (i.e., current reference step response, DC-link voltage reference and load step response, mid-point voltage deviation unbalance step response).

4.5.1 Steady-State Operation

An overview of the rectifier steady-state AC-side inductor currents i_{abc} and DC-link mid-point current i_m is provided in **Fig. 3.13** and **Fig. 3.14**, respectively (cf. **Section 3.3**).

Since the grid-side current THD is a direct performance indicator of the steady-state current control loop performance, **Fig. 4.10** simultaneously shows the converter-side currents i_{abc} and the grid-side (i.e., filtered) currents $i_{g,abc}$ for $V_{dc} = 800\,\text{V}$, $\varphi = 0$ and different values of transferred power. It is observed that the grid-side currents slightly anticipate the respective PCC voltages, as the current flowing into the filter capacitors C_f is not compensated by the control (i.e., $\varphi = 0$). Furthermore, as already mentioned in **Section 3.3.1**, the phase current quality improves with the rectifier loading. For instance, at 10 % of the rated power (cf. **Fig. 4.10(b)**) the converter-side current ripple amplitude becomes comparable to the current peak value, therefore leading to marked low-frequency zero-crossing distortion that bypasses the filter capacitor and appears in the grid-side currents. Even though the distortion at light load may seem large, the pronounced DCM operation of unidirectional rectifiers typically leads to much higher distortion levels [54]. In the present case, the pseudo-sinusoidal shape of the currents is maintained thanks to the adopted current oversampling and averaging strategy, the high current control loop bandwidth and the feed-forward contributions illustrated in **Fig. 4.3**. At 50 % and 100 % of the rated power (cf. **Fig. 4.10(c)– (d)**) the quality of both converter-side and grid-side currents significantly improves, as the relative amplitude of the current ripple decreases and the zero-crossing distortion related to DCM operation is mostly eliminated by the high closed-loop control bandwidth.

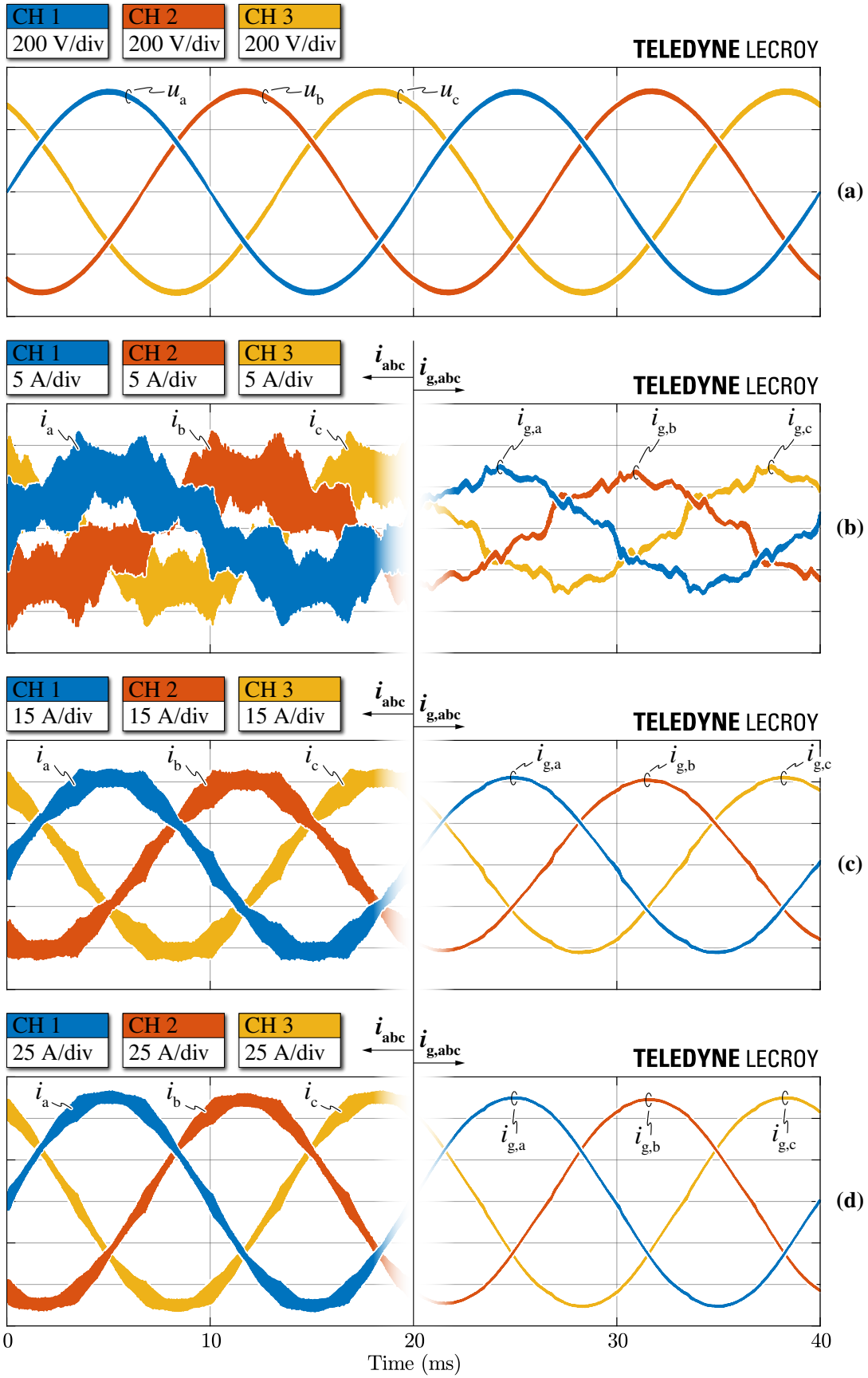


Fig. 4.10: Experimental **(a)** PCC voltage waveforms u_{abc} and **(b)–(d)** converter-side currents i_{abc} and grid-side currents $i_{g,abc}$ in steady-state conditions with ZMPCPWM, $V_{dc} = 800\,\text{V}$ and $\varphi = 0$ at **(b)** 10 %, **(c)** 50 % and **(d)** 100 % of the nominal power (i.e., $P = 30\,\text{kW}$).

To highlight the benefits of the implemented zero-sequence voltage saturation block ($v_{\mathrm{o,max/min}}$, cf. **Fig. 4.6**), the steady-state operation of the rectifier under non-unity power factor (i.e., $\varphi \neq 0$) and under unbalanced split DC-link loading (i.e., $I_{\mathrm{o,p}} \neq I_{\mathrm{o,n}}$, $V_{\mathrm{o},\delta} \neq 0$) is assessed, comparing the proposed solution to a conventional control implementation with no saturation acting on v_{o}.

The steady-state operation of the rectifier at $\varphi = 15^{\circ}$ is illustrated in **Fig. 4.11** for $V_{\mathrm{dc}} = 800\,\mathrm{V}$ and $S = 15\,\mathrm{kVA}$, showing the reference bridge-leg voltages v^{*}_{am}, v^{*}_{bm}, v^{*}_{cm}, the reference zero-sequence voltage v^{*}_{o}, the converter-side currents i_{abc}, the grid-side currents $i_{\mathrm{g,abc}}$ and the DC-link mid-point current i_{m}. In particular, v^{*}_{am}, v^{*}_{bm}, v^{*}_{cm} and v^{*}_{o} are obtained from separate digital-to-analog converters (DACs) of the MCU (i.e., with a 0–3.3 V scale) and are thus suitably rescaled. It is observed that the operation at non-unity power factor leads to a significant zero-crossing distortion if no zero-sequence voltage saturation is implemented. The enforcement of $v_{\mathrm{o,max/min}}$, in fact, allows the rectifier to correctly apply the desired bridge-leg voltage values even when the phase currents are phase-shifted with respect to the reference voltages (cf. **Section 2.2.2**), allowing for undistorted operation. Furthermore, **Fig. 4.11(d)** shows that by saturating the zero-sequence voltage, a larger mid-point current local average i_{m} and thus a higher DC-link mid-point peak-to-peak charge ripple $\Delta Q_{\mathrm{m,pp}}$ are obtained. This is because, to ensure the undistorted operation of the rectifier, the applied zero-sequence voltage v_{o} departs from the ideal $v_{\mathrm{o,3}}$ waveform introduced by ZMPCPWM, as explained in **Section 2.4.2** (cf. **Fig. 2.17**, **Fig. 2.18**).

Fig. 4.12 shows the rectifier operation under constant zero-sequence voltage injection $V^{*}_{\mathrm{o},\delta} = 0.15\,V_{\mathrm{dc}}/2$, which is added to $v^{*}_{\mathrm{o,3}}$. This injection emulates the converter performance under unbalanced split DC-link loading, i.e., when the rectifier provides a constant mid-point current periodical average $I_{\mathrm{m}} = I_{\mathrm{o,n}} - I_{\mathrm{o,p}}$. In particular, **Fig. 4.12(d)** shows that the injection of a positive value of $V^{*}_{\mathrm{o},\delta}$ generates a negative value of I_{m}, as expected from theoretical considerations. Also in this case, the zero-sequence voltage saturation $v_{\mathrm{o,max/min}}$ provides a substantial improvement of the phase current waveforms (cf. **Fig. 4.12(c)**) and leads to larger i_{m} and $\Delta Q_{\mathrm{m,pp}}$ ripple values (cf. **Fig. 4.12(d)**). However, the zero-crossing distortion cannot be completely avoided in this case, as the injection of a constant zero-sequence voltage component increases the amplitude of the converter-side current ripple (cf. **Fig. 4.10(c)** for comparison), which widens the DCM window around the current zero-crossings and leads to higher distortion. In this context, it is worth noting that the DCM-related current distortion can be greatly reduced in practice by independently controlling the two anti-series mid-point switches (i.e., with two separate gate drivers), such that the free-wheeling of the current through the mid-point is always possible [105]. In this work, the two anti-series switches are controlled with the same PWM signal to simplify the rectifier modulation process (cf. **Section 2.3.1**).

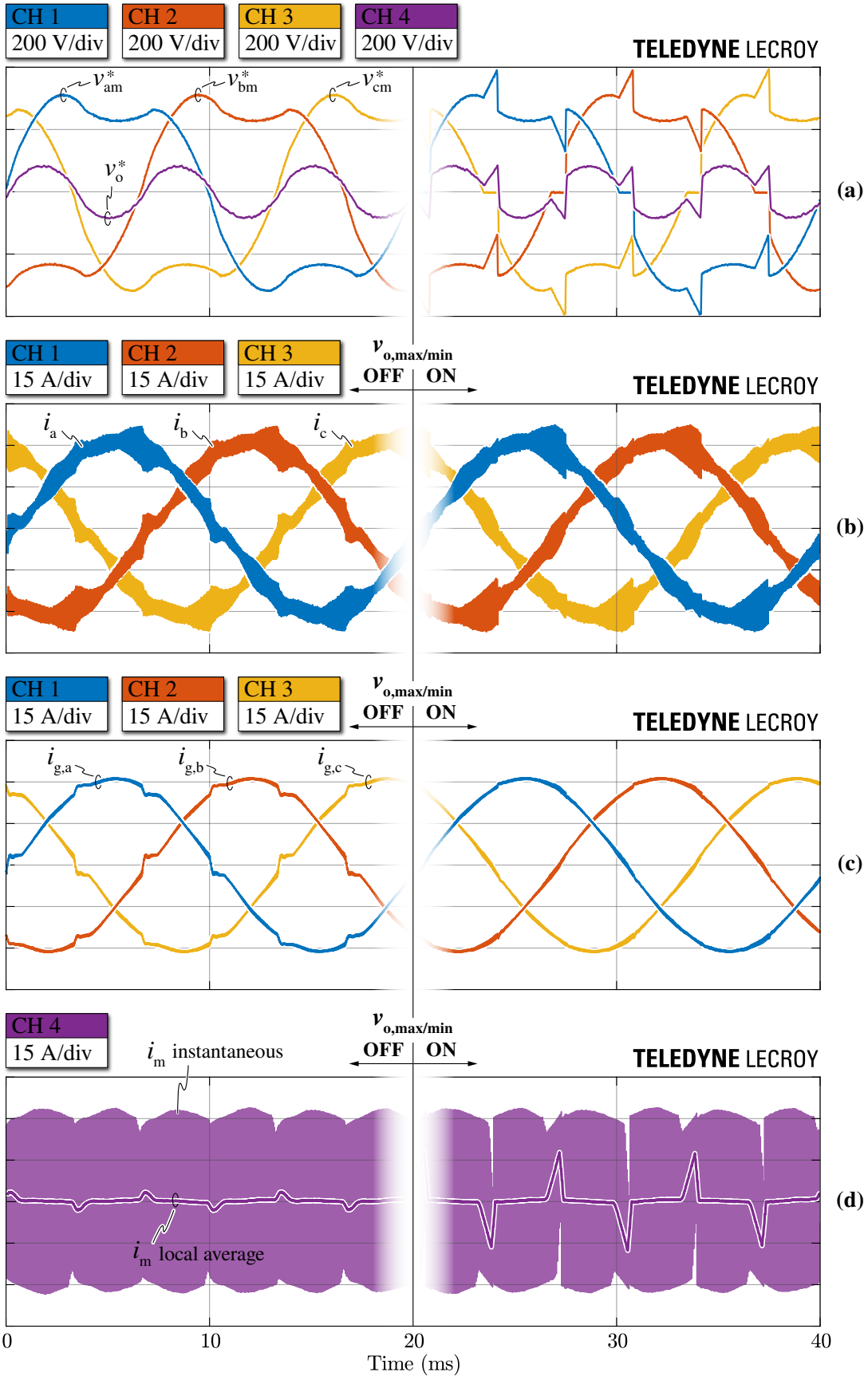


Fig. 4.11: Experimental waveforms in steady-state conditions with $V_{dc} = 800\,\text{V}$, $\varphi = 15°$, $S = 15\,\text{kVA}$. **(a)** reference bridge-leg and zero-sequence voltages v^*_{xm}, v^*_o, **(b)** converter-side currents i_{abc}, **(c)** grid-side currents $i_{g,abc}$, **(d)** mid-point current i_m, with/without zero-sequence voltage saturation $v_{o,max/min}$.

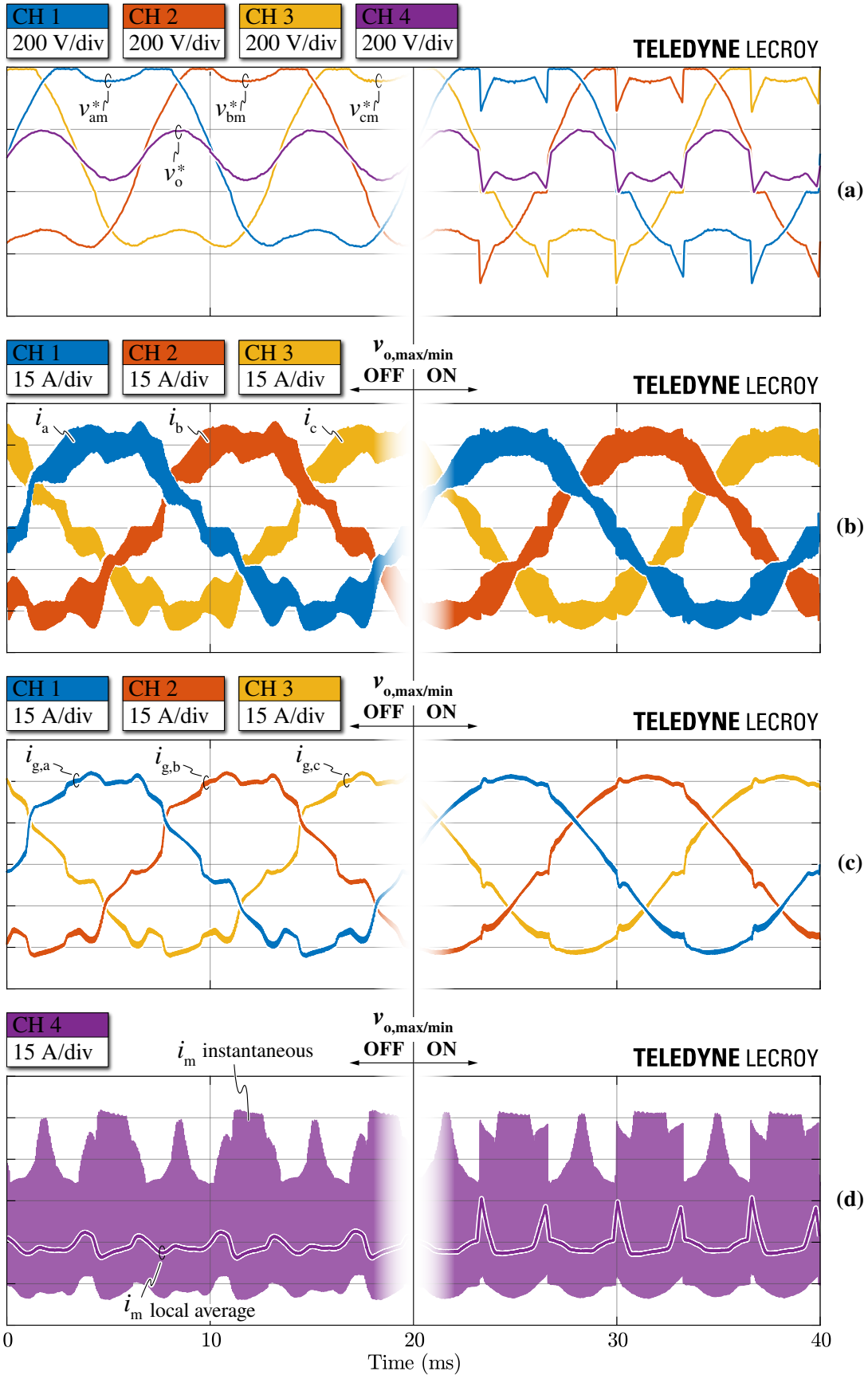


Fig. 4.12: Experimental waveforms in steady-state conditions with $V_{dc} = 800\,\text{V}$, $\varphi = 0$, $V_{o,\delta} = 0.15\,V_{dc}/2$, $P = 15\,\text{kW}$. **(a)** reference bridge-leg and zero-sequence voltages v^*_{xm}, v^*_o, **(b)** converter-side currents i_{abc}, **(c)** grid-side currents $i_{g,abc}$, **(d)** mid-point current i_m, with/without zero-sequence voltage saturation $v_{o,max/min}$.

Total Harmonic Distortion (THD)

The grid-side current total harmonic distortion (THD) is defined as

$$\mathrm{THD} = \frac{\sqrt{I_{\mathrm{g,RMS}}^2 - I_{\mathrm{g,1,RMS}}^2}}{I_{\mathrm{g,1,RMS}}} \tag{4.26}$$

where $I_{\mathrm{g,RMS}}$ is the total RMS value of the grid-side current and $I_{\mathrm{g,1,RMS}}$ is the RMS value of the grid current first harmonic.

The rectifier performance is mapped over the complete modulation index M and power factor angle φ operating region, both at 50 % and 100 % of the nominal apparent power (i.e., $S = 30\,\mathrm{kVA}$). The results are shown in **Fig. 4.13**, where the THD performance obtained with and without $v_{\mathrm{o,max/min}}$ saturation are compared. As expected from **Fig. 4.10**, the grid-side current quality improves at higher load levels, as the zero-crossing distortion is reduced. Moreover, by enforcing the zero-sequence voltage saturation, the THD stays

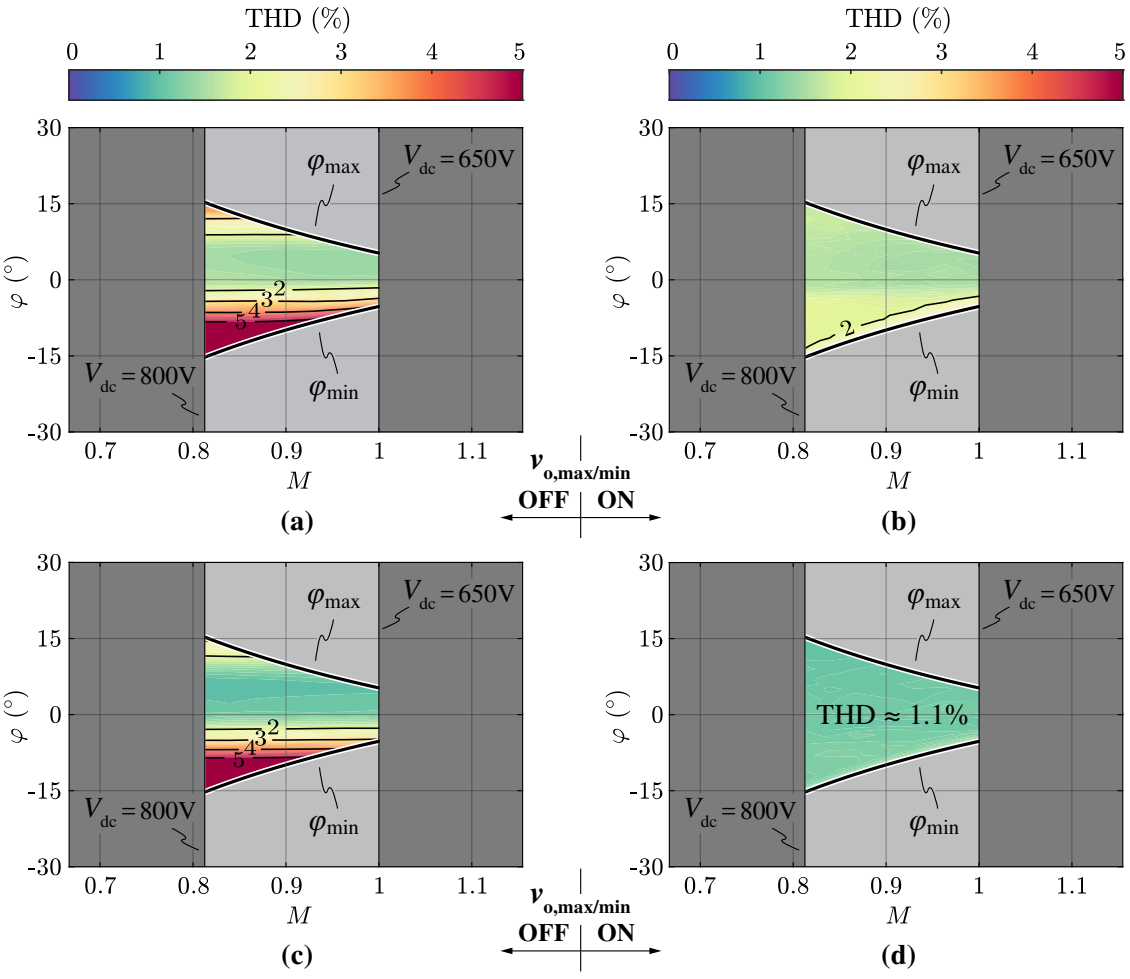


Fig. 4.13: Experimental grid-side current THD for **(a)–(b)** $S = 15\,\mathrm{kVA}$ and **(c)–(d)** $S = 30\,\mathrm{kVA}$ with/without zero-sequence voltage saturation $v_{\mathrm{o,max/min}}$.

below the conventional 5 % limit (i.e., required by grid standards [11]) for all operating points, which is not the case when $v_{\mathrm{o,max/min}}$ is disabled. Finally, it is observed that the THD values are not symmetrical with respect to φ, resulting in worse distortion for $\varphi < 0$ (i.e., capacitive operation). This is mainly due to the fact that the zero-sequence voltage saturation modifies the current ripple shape and amplitude, leading to a wider DCM operation around the zero-crossings for negative values of φ.

Displacement Power Factor (DPF)

The displacement power factor (DPF) of the rectifier is defined as

$$\mathrm{DPF} = \cos\left(\angle\vec{U} - \angle\vec{I}_{\mathrm{g}}\right) = \frac{P}{S} \tag{4.27}$$

where $\angle\vec{U}$ and $\angle\vec{I}_{\mathrm{g}}$ are the phase angles of the grid voltage vector (i.e., measured at the PCC) and the grid current vector, respectively. It is worth noting that DPF $\neq \varphi$, as the grid-side converter current also includes the filter capacitor current contribution.

The experimental DPF is illustrated in **Fig. 4.14** for 50 % and 100 % of the nominal apparent power (i.e., $S = 30\,\mathrm{kVA}$). In both cases, the zero-sequence voltage saturation is enabled. For a better understanding of the phase-shift between $\vec{U}$ and $\vec{I}_{\mathrm{g}}$, the DPF angle $\cos^{-1}(\mathrm{DPF})$ is shown in **Fig. 4.15**, where a positive value indicates a lagging power factor (i.e., inductive behavior) and a negative value indicates a leading power factor (i.e., capacitive behavior). It can be observed that the current flowing into the filter capacitors C_{f} is completely compensated for $\varphi \approx 4.2°$ at 50 % of the rated power and $\varphi \approx 3°$ at 100 % of the rated power, as expected from basic theoretical considerations.

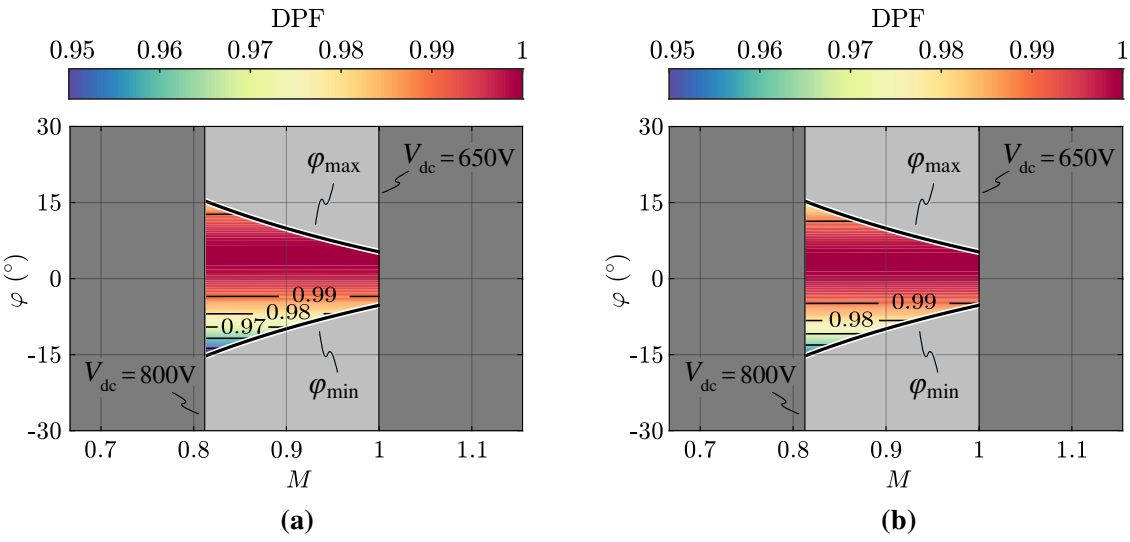


Fig. 4.14: Experimental grid-side displacement power factor (DPF) for **(a)** $S = 15\,\mathrm{kVA}$ and **(b)** $S = 30\,\mathrm{kVA}$. The zero-sequence voltage saturation $v_{\mathrm{o,max/min}}$ is enabled.

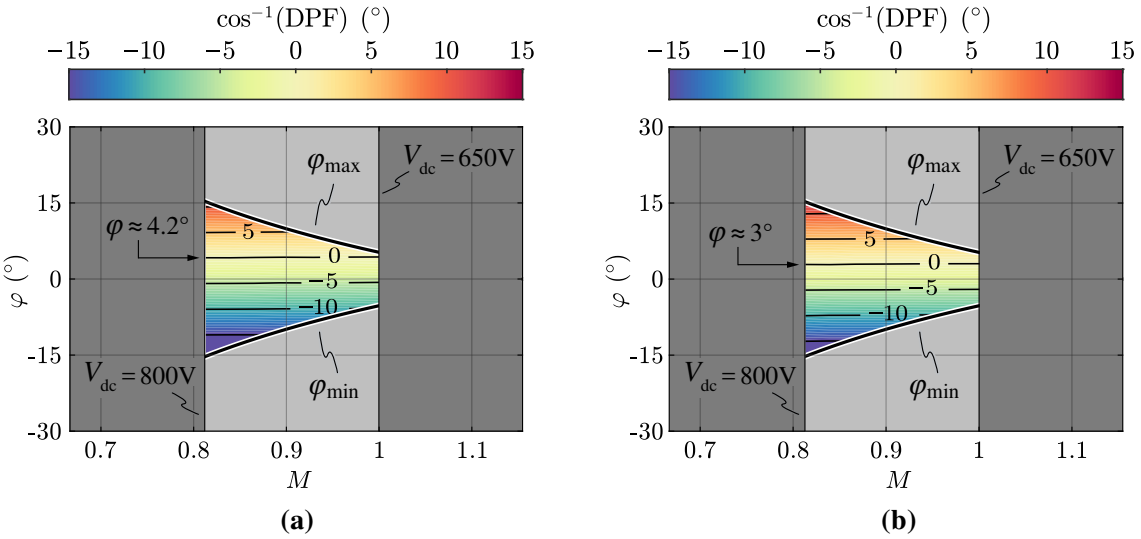


Fig. 4.15: Experimental grid-side current-to-voltage phase-shift $\cos^{-1}(\mathrm{DPF})$ for **(a)** $S = 15\,\mathrm{kVA}$ and **(b)** $S = 30\,\mathrm{kVA}$. The current flowing into the filter capacitors C_f is completely compensated for $\varphi \approx 4.2°$ in **(a)** and $\varphi \approx 3°$ in **(b)**.

Mid-Point Current Capability

The maximum DC-link mid-point current capability of the rectifier $I_{\mathrm{m,max}}$ is assessed experimentally by operating the converter at 50 % of the rated apparent power (i.e., $S = 15\,\mathrm{kVA}$) and injecting a zero-sequence voltage equal to $v_{\mathrm{o,min}}$. The experimental results are compared to (2.34) in **Fig. 4.16**, where $I_{\mathrm{m,max}}$ is normalized with respect to the converter-side peak phase current value I. It is observed that the analytical and the experimental results are in close agreement, achieving a maximum deviation of 5 % over the complete operating range of the rectifier.

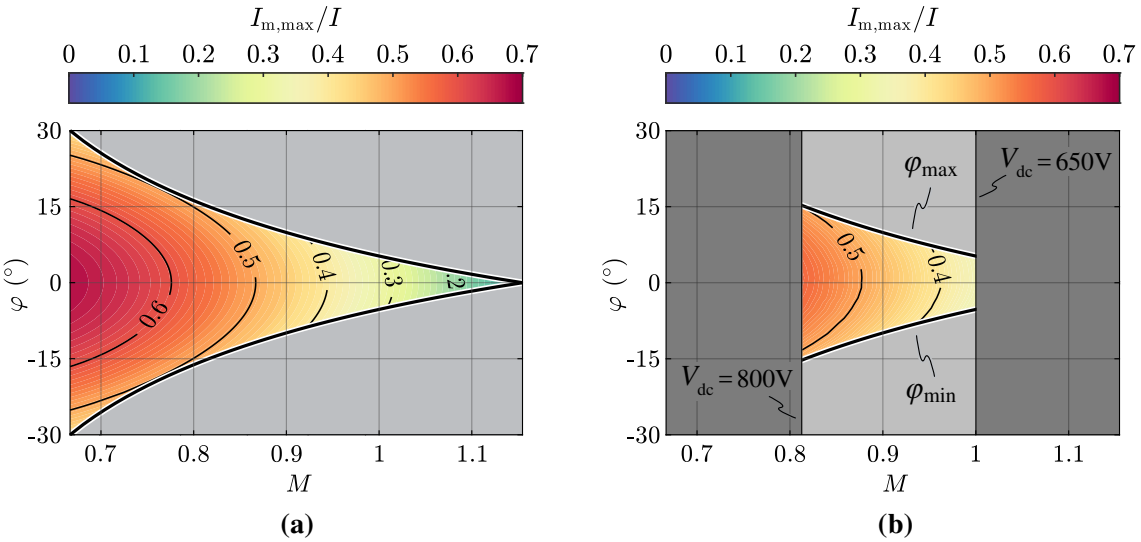


Fig. 4.16: Maximum rectifier mid-point current capability $I_{\mathrm{m,max}}$, normalized with respect to the peak phase current value I: **(a)** analytical results according to (2.34) and **(b)** experimental results.

4.5.2 Dynamical Operation

In this section, the large-signal dynamical performance of all control loops is verified experimentally, complementing the small-signal simulation results of **Section 4.4**.

dq Current Control Loops

The dynamical performance of the dq current control loops is verified by testing the system response to a d-axis current reference I_{d}^{*} step (i.e., being the q-axis current control loop identical, cf. **Fig. 4.4**). The measured phase currents i_{abc} and d-axis current I_{d} for a current step between 50 % and 100 % of the nominal rated current $I = 61.5\,\mathrm{A}$ are shown in **Fig. 4.17**. A fast rise-time of $\approx 0.4\,\mathrm{ms}$ and a $\approx 15\,\%$ overshoot are observed, very much consistent with the tuning procedure outlined in **Section 4.3.1**. It is worth noting that I_{d} is discretized in time, since it is measured at the output of a digital-to-analog converter (DAC) of the MCU and is updated once per control period (i.e., $T_{\mathrm{s}} = 50\,\mu\mathrm{s}$).

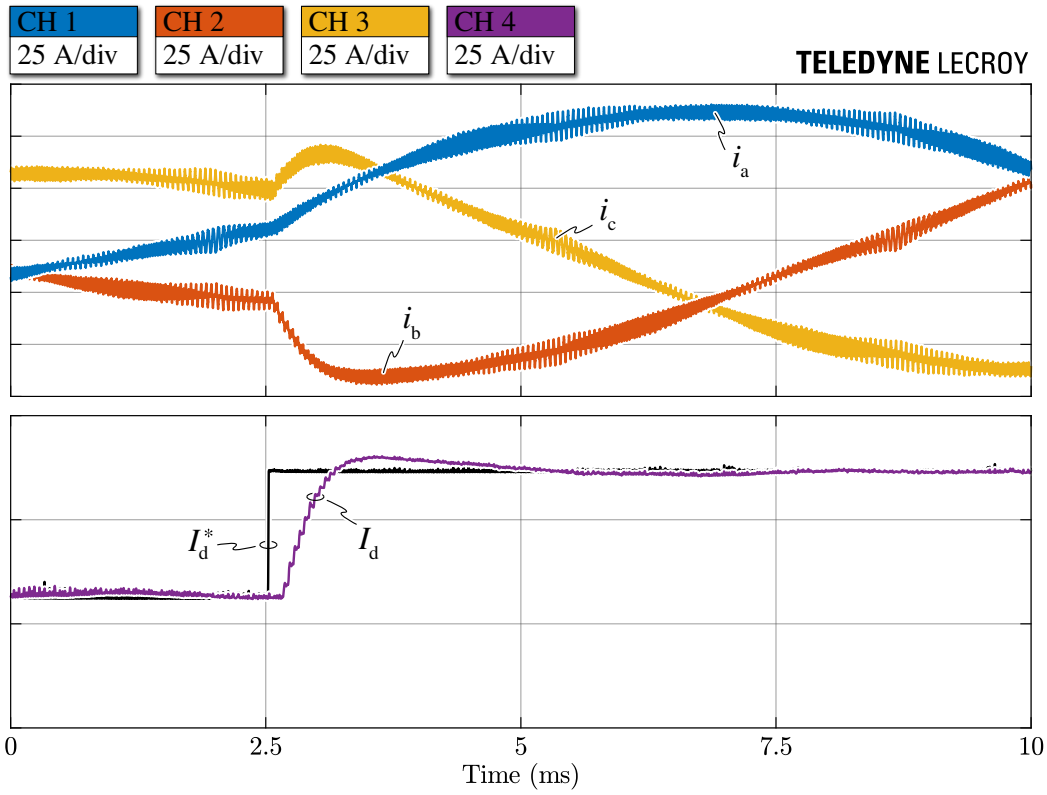


Fig. 4.17: Experimental d-axis current control loop reference step response between 50 % and 100 % of the nominal current (i.e., $I = 61.5\,\mathrm{A}$) with $V_{\mathrm{dc}} = 800\,\mathrm{V}$. Measured phase currents i_{abc}, d-axis current reference I_{d}^{*} and d-axis current I_{d}. The d-axis quantities are obtained from the DAC of the MCU (i.e., with a 0–3.3 V measurement range), therefore they are rescaled.

DC-Link Voltage Control Loop

The dynamical performance of the DC-link voltage control loop is verified with two separate tests.

First, the system response to a step in V_{dc}^{*} is assessed. **Fig. 4.18** shows the DC-link voltage control loop response to a reference step change between $V_{dc} = 650\,V$ and $V_{dc} = 800\,V$. Due to the large DC-link voltage variation, the PI controller output (i.e., I_{d}^{*}) reaches the maximum converter current limit I_{max} and gets saturated (cf. **Fig. 4.5**), therefore V_{dc} rises linearly avoiding overshoots. **Fig. 4.18** also shows that the two cascaded control loops (i.e., outer V_{dc} loop and inner I_{d} loop) are well decoupled and do not interfere with each other.

The second test evaluates the disturbance rejection capability of the control loop, by assessing the DC-link voltage deviation following a load step. To strictly evaluate the dynamical performance of the controller, the feed-forward contribution $(I_{o,p} + I_{o,n})/2$ shown in **Fig. 4.5** is disabled. **Fig. 4.19** shows the system response to a 10 kW load step between $P_{o} = 22.5\,kW$ and $P_{o} = 12.5\,kW$. A maximum voltage deviation of $\approx 15\,V$ is observed, mostly counteracted by the large low-frequency open-loop gain of the controller,

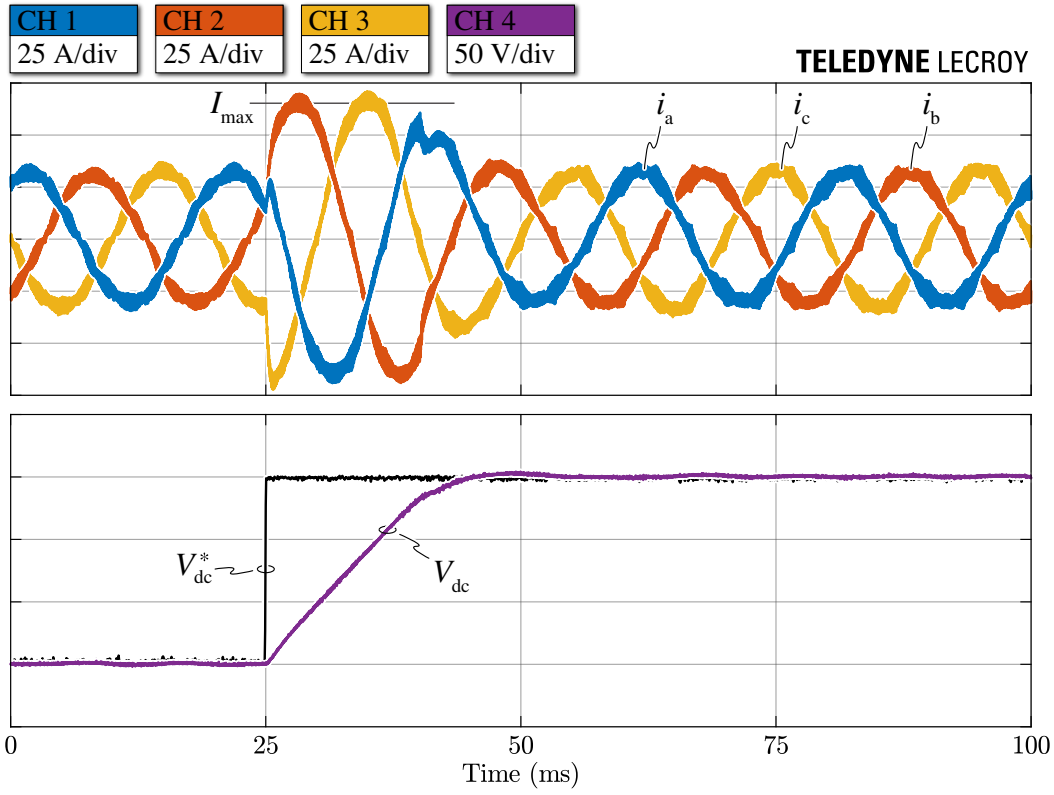


Fig. 4.18: Experimental DC-link voltage control loop reference step response between $V_{dc} = 650\,V$ and $V_{dc} = 800\,V$ with a constant load power $P_{o} = 15\,kW$. Measured phase currents i_{abc}, DC-link voltage reference V_{dc}^{*} and DC-link voltage V_{dc}. The DC-link voltage reference is obtained from the DAC of the MCU (i.e., with a 0–3.3 V measurement range), therefore it is rescaled.

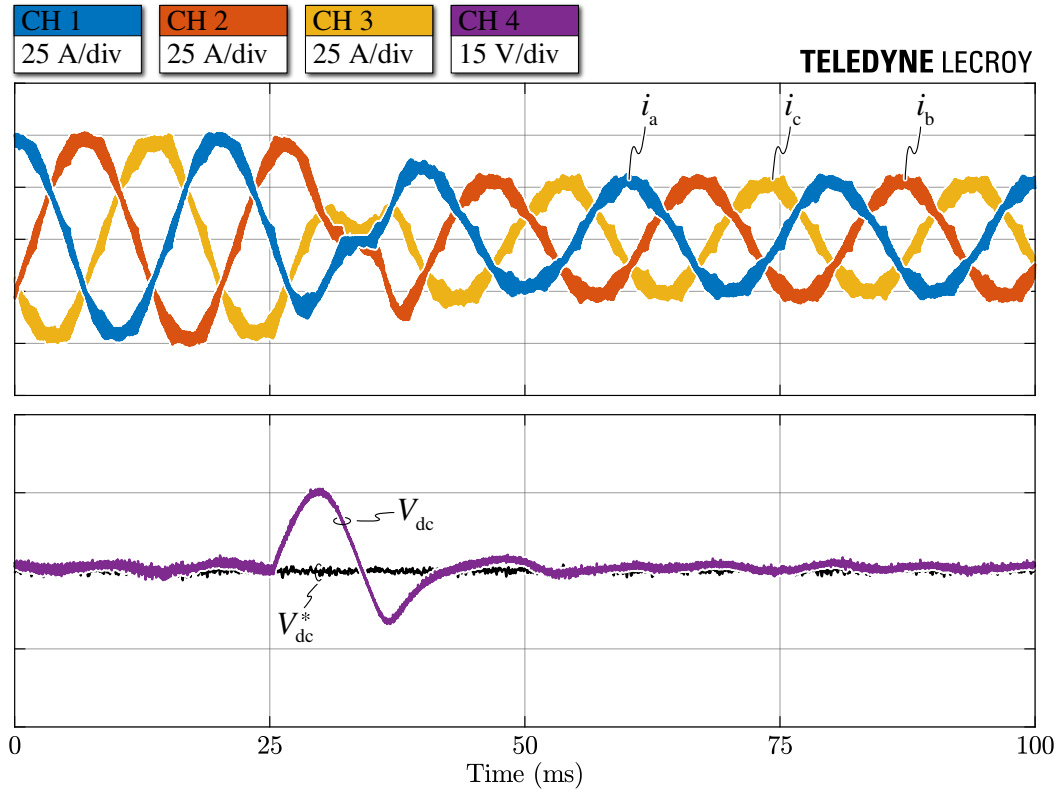


Fig. 4.19: Experimental DC-link voltage control loop response to a 10 kW load step between $P_o = 22.5\,\text{kW}$ and $P_o = 12.5\,\text{kW}$ with $V_{dc} = 800\,\text{V}$. Measured phase currents i_{abc}, DC-link voltage reference V^*_{dc} and DC-link voltage V_{dc}. The DC-link voltage reference is obtained from the DAC of the MCU (i.e., with a 0–3.3 V measurement range), therefore it is rescaled.

which ensures the desired high disturbance rejection performance. It is worth noting that, since the rectifier is unable to reverse the power transfer, the currents are temporarily controlled to zero in response to the DC-link voltage overshoot. During this time interval, the DC-link voltage decreases almost linearly due to the constant power absorbed by the load, and the system dynamics are therefore uncontrolled (i.e., they are completely determined by the load).

DC-Link Mid-Point Voltage Balancing Loop

Finally, the dynamical performance of the DC-link mid-point voltage balancing control loop is assessed by evaluating the mid-point voltage deviation following a load unbalance step. As previously illustrated in **Fig. 4.6**, the V_m control loop regulates the mid-point current I_m by acting on the zero-sequence voltage injection $V_{o,\delta}$. Since the zero-sequence voltage does not affect the phase voltages applied by the rectifier, the V_m loop ideally does not interfere with the phase currents and/or the total power transfer. **Fig. 4.20** shows the system response to a 3 kW load unbalance step, performed by changing the power absorbed by the electronic

load connected to the lower DC-link half between $P_{o,n} = 10.5\,\text{kW}$ and $P_{o,n} = 7.5\,\text{kW}$. It is worth noting that, for simplicity of the test realization, both an unbalance step and a load step are performed simultaneously, as only one DC-link half is affected by the load step. Therefore, both the V_{dc} and V_m control loops act at the same time, however their response is completely decoupled. In particular, it is observed that the action of the V_{dc} loop is restricted to few ms after the step (i.e., visible by the amplitude change of the phase currents), while the response of the V_m loop lasts tens of ms, due to its lower bandwidth. A maximum mid-point voltage dynamical deviation of 18 V is obtained, as the PI regulator zero $\omega_{z,b}$ has been tuned to maximize the disturbance rejection capability of the controller (cf. **Section 4.3.3**).

Furthermore, the same test is performed adopting SPWM (i.e., $v_{o,3} = 0$), to increase the DC-link mid-point voltage oscillation and highlight the fundamental role of the MAF applied to the measured V_m (cf. **Fig. 4.6**). The results of this test are illustrated in **Fig. 4.21** and show that similar control performance is achieved when adopting either ZMPCPWM or SPWM, as the MAF eliminates the 150 Hz voltage ripple from the V_m feedback.

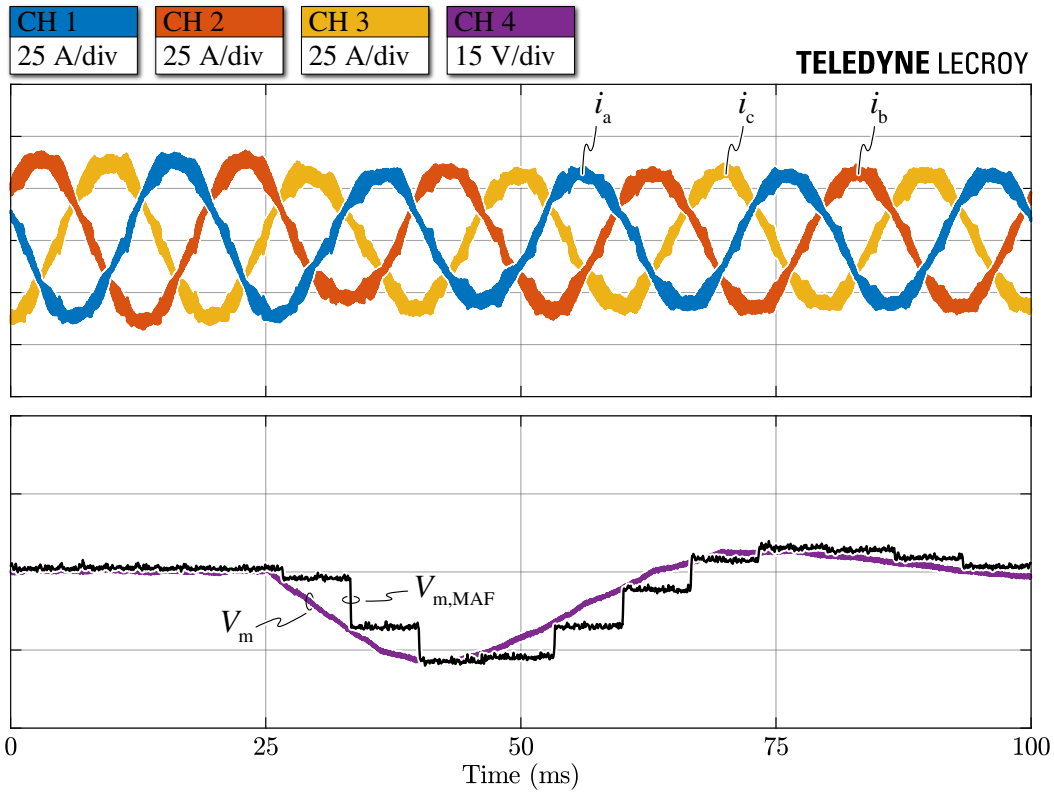


Fig. 4.20: Experimental DC-link mid-point voltage balancing loop response to a 3 kW load unbalance step with $V_{dc} = 800\,\text{V}$ and ZMPCPWM. The load connected to the lower DC-link half performs a step between $P_{o,n} = 10.5\,\text{kW}$ and $P_{o,n} = 7.5\,\text{kW}$, whereas the load connected to the higher half absorbs a constant power $P_{o,p} = 7.5\,\text{kW}$. Measured phase currents i_{abc}, DC-link mid-point voltage deviation V_m and DC-link mid-point voltage moving average $V_{m,MAF}$. The mid-point voltage moving average is obtained from the DAC of the MCU (i.e., with a 0–3.3 V measurement range), therefore it is rescaled.

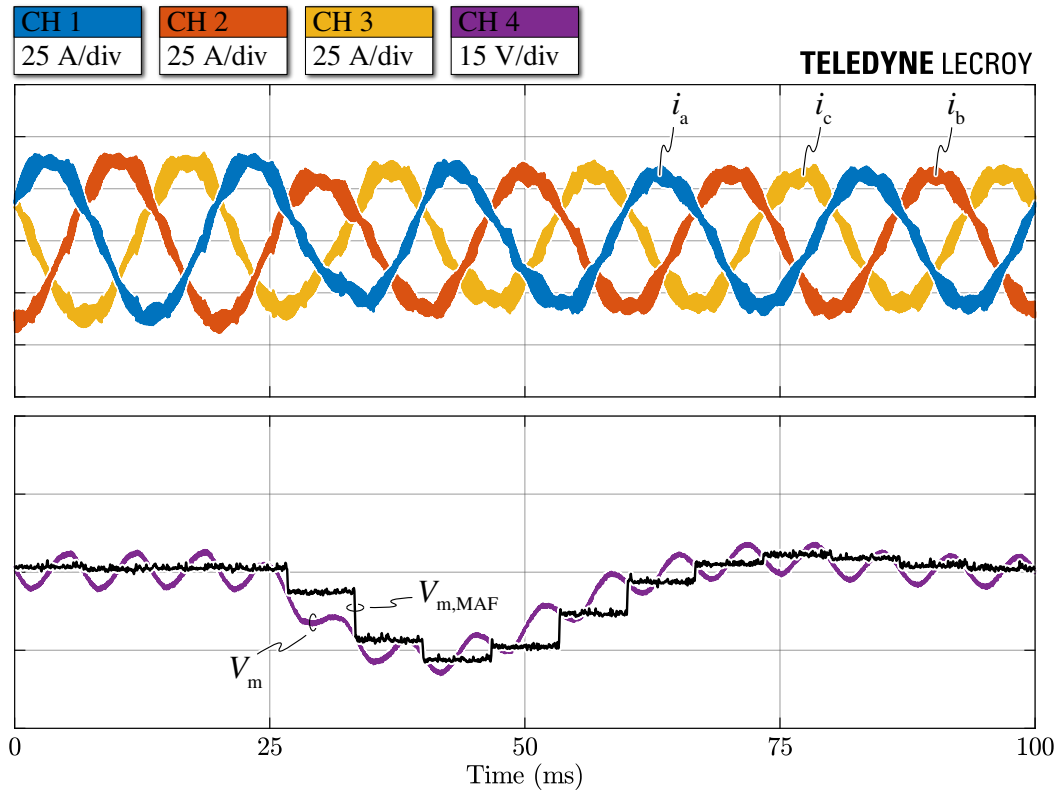


Fig. 4.21: Experimental DC-link mid-point voltage balancing loop response to a 3 kW load unbalance step with $V_{dc} = 800$ V and SPWM. Refer to **Fig. 4.20** for further details.

4.6 Summary

This chapter has presented the design, tuning and experimental assessment of the adopted digital multi-loop control strategy for the considered three-level unidirectional AC/DC converter for EV ultra-fast battery charging. To accurately design the four control loops (i.e., dq-currents, DC-link voltage, DC-link mid-point voltage deviation), the system state-space equations have been exploited to derive a fourth-order small-signal model of the three-level rectifier. The controllers have then been accurately tuned, taking into account the delays and the discretization introduced by the digital control implementation and compensating for the plant non-linearities. Finally, the steady-state and dynamical performances of the proposed multi-loop control strategy have been verified in circuit simulation and experimentally on the T-type rectifier prototype, adopting a general purpose microcontroller unit (MCU) for the digital control implementation (i.e., running at 20 kHz). Overall, the designed control loops have achieved all requested features, namely sinusoidal input current shaping with low THD under all operating conditions (i.e., with non-unity power factor and unbalanced split DC-link loading), fast response dynamics and strong disturbance rejection.

PART II

DC/DC Converter

Chapter 5

DC/DC Converter – Analysis

Abstract

The DC/DC conversion stage of an electric vehicle (EV) ultra-fast battery charger must control the charging process (i.e., the power delivered to the battery), meanwhile providing galvanic isolation from the grid. Since the application demands high conversion efficiency and power density, only converter topologies operating in soft-switching conditions are suitable candidates. In this chapter, an overview of the most adopted topologies for EV battery charging is provided and a resonant LLC converter is selected for the present 4x15 kW application, due to its unmatched efficiency and wide output load/voltage regulation capability. The operating principle of the LLC converter is described, leveraging the first harmonic approximation (FHA) method to identify the converter operating limits in terms of switching frequency, input/output voltage gain and output load. Furthermore, the three typical modes of operation of the LLC converter (i.e., boost-mode, unity-gain-mode, buck-mode) are described in detail and the soft-switching mechanisms of the primary-side transistors and secondary-side diodes are explained. Finally, the stresses on the converter active and passive components (i.e., semiconductor devices, resonant capacitor, resonant inductor, transformer, input/output filter capacitors) are assessed both analytically with FHA and numerically with the more accurate time-domain analysis (TDA), providing straightforward tools for the converter design and/or assessment.

5.1 Introduction

The high-frequency isolated DC/DC converter of an EV ultra-fast battery charger has the fundamental role of controlling the power delivered to the battery (i.e., regulating the charging current), meanwhile providing galvanic isolation from the grid. The main requirements of this converter stage include:

- wide output load and voltage regulation capability, to comply with the broad range of battery voltage and load levels during the charging process [4, 17];
- low battery-side current ripple, which causes the premature aging of the battery itself [119].
- high conversion efficiency and power density.

Notably, high power density can only be achieved by operating the converter at high switching frequencies, in order to reduce the size of the passive components. Therefore, the soft-switching operation of all semiconductor devices is a fundamental requirement, as it provides the only means to limit the converter losses and thus achieve high conversion efficiency. Accordingly, hard-switching converters cannot be adopted in the present application.

5.1.1 Converter Topologies

Considering that the power must only flow unidirectionally from the grid to the battery, and taking into account the mentioned DC/DC stage requirements, the most suitable converter topologies for the considered 4x15 kW converter application (cf. **Section 1.3**) are:

- phase-shift full bridge (PSFB) converter (cf. **Fig. 5.1(a)**); originally proposed in [120], analyzed in detail in [121, 122] and often adopted in EV battery chargers [123, 124], the PSFB consists of an input transistor bridge, an output diode bridge, an isolation transformer (i.e., including a leakage inductance component) and an output filter inductor. The converter operates as a buck (i.e., step-down) converter, regulating the phase shift between the two primary bridge-legs to modify the duty-cycle of the voltage square-wave applied to the transformer, meanwhile achieving the zero-voltage switching (ZVS) operation of the primary transistors. The voltage applied to the transformer is then rectified by the secondary-side diode bridge and is thus applied to the output inductor. While this converter can achieve high efficiency in rated load conditions, it is affected by several drawbacks, such as the duty-cycle loss for increasing load values (i.e., which translates in a reduction in the active power transfer capability), the relatively high switching losses in the output diodes (i.e., due to the high turn-off $^{di}/_{dt}$) and the loss of the primary-side transistor ZVS in light load conditions. Furthermore, the large LC ringing across the secondary-side rectifier (i.e., between the transformer leakage inductance and the output capacitance of the diodes) either requires semiconductor devices with a blocking voltage rating of two times the maximum output voltage, or demands for the adoption of active or passive snubber circuits at the cost of reduced system efficiency.

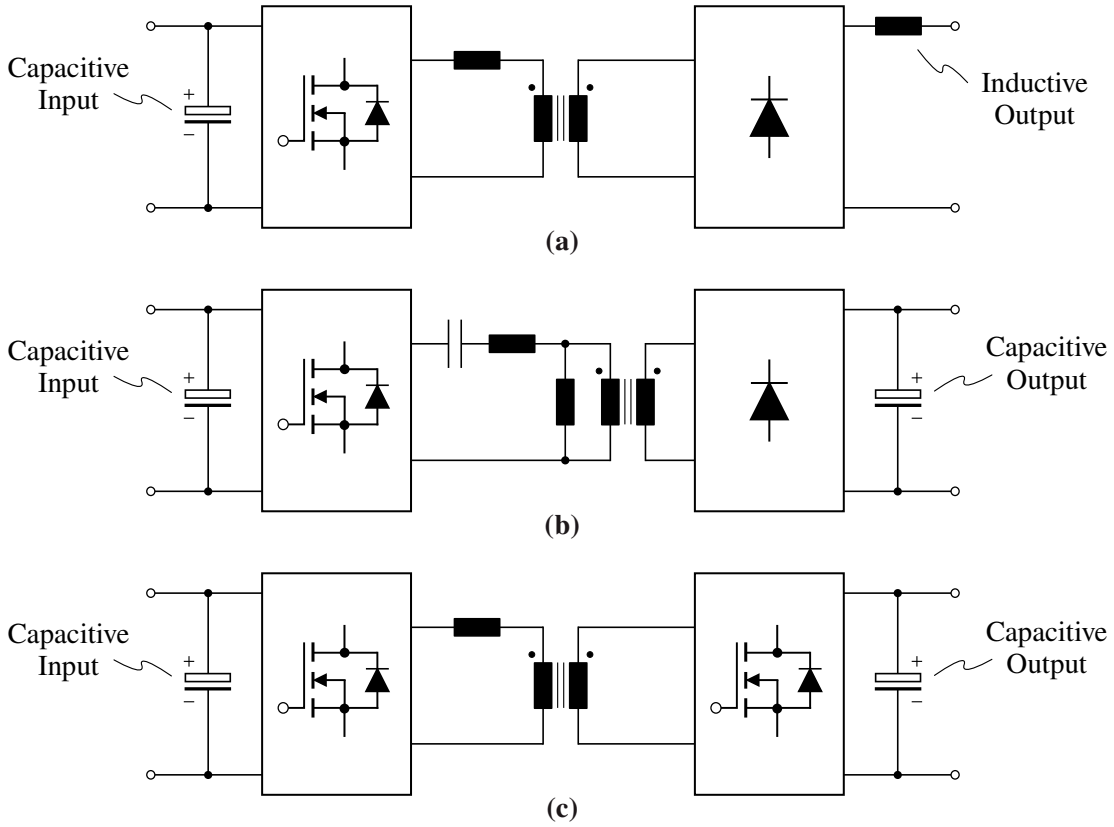


Fig. 5.1: Simplified equivalent circuit schematics of the most suitable converter topologies for EV battery charging: **(a)** phase-shift full-bridge (PSFB) converter, **(b)** series-parallel resonant LLC converter, **(c)** dual active bridge (DAB) converter.

- series-parallel resonant LLC converter (cf. **Fig. 5.1(b)**); originally patented in [125], analyzed in detail in [126–128] and currently widespread in EV charging applications [129–134], the LLC resonant converter consists of an input inverter bridge, an output rectifier bridge and a resonant tank made up by a series capacitor, a series inductor and an isolation transformer, which features a non-negligible parallel magnetizing inductance component. In particular, the LLC converter addresses the main shortcomings of the other basic resonant topologies (i.e., series-resonant and parallel-resonant [135]), featuring a wide output load/voltage regulation capability. As for all resonant topologies, the main regulation principle of the LLC converter is based on varying the switching frequency of the inverter bridge to modulate the impedance of the resonant tank, which may provide both step-up (i.e., boost) and step-down (i.e., buck) functionality with a relatively narrow switching frequency variation. A prominent feature of the LLC converter is the soft-switching operation of all semiconductor devices across the complete operating region, since the transformer magnetizing current allows to achieve the ZVS of the primary-side transistors also in no-load conditions, whereas the relatively low values of $^{di}/_{dt}$ practically eliminate the reverse-

recovery loss of the output rectifier diodes. Notably, the soft-switching operation of all semiconductor devices is behind the well documented high efficiency achievable by this converter topology and, together with the low values of $^{di}/_{dt}$, also leads to limited EMI generation. The main drawback of the LLC converter is that the resonant tank consists of three passive components (i.e., capacitor, inductor and transformer), which may negatively affect the overall converter power density. Nonetheless, with a proper design, the series resonant inductor can be integrated into the transformer (i.e., as the leakage inductance component), whereas the resonant capacitor can be realized with ceramic technology, simultaneously providing the required high-voltage and high-current specifications with minimum footprint. Furthermore, the soft-switching operation of both transistors and diodes allows to significantly increase the converter switching frequency, thus enabling the volume reduction of the passive components with a minor impact on the conversion efficiency.

- dual active bridge (DAB) converter (cf. **Fig. 5.1(c)**); originally described in [136], analyzed in detail in [137–139] and typically proposed for next-generation bidirectional EV battery chargers [140, 141], the DAB consists of two transistor bridges, an isolation transformer and an inductor. Due to its capacitive output, the DAB can achieve high power density, especially if the primary-side inductor is integrated within the transformer (i.e., as the leakage inductance component). This topology requires an active bridge at the secondary side to achieve a wide input/output voltage regulation capability (i.e., buck-boost operation) and ensure the ZVS of all semiconductor devices: in fact, if the secondary-side transistor bridge is replaced with a diode rectifier, the converter operating limits are significantly shrunk and some primary-side transistors experience lossy zero-current switching (ZCS) transitions [142]. In the DAB converter the primary-side inductor serves as the power-transfer element, as the power flow is controlled by adjusting the phase shift between the fundamental components of the primary and the secondary voltages (i.e., regulating the quadrature voltage applied across the inductor). Due to the wide input/output voltage range and the variable load required in battery charging applications, the reactive power transfer can increase substantially and the ZVS of the transistors may be lost. To enhance the performance of the DAB converter under a wide variety of operating conditions, three main modulation strategies have been proposed, namely single phase-shift (SPS) modulation [137, 138], double phase-shift (DPS) modulation [143, 144] and triple phase-shift (TPS) modulation [145, 146], which increasingly exploit the three control degrees of freedom of the converter (i.e., primary duty-cycle, secondary duty-cycle, primary-to-secondary phase-shift). Additionally, hybrid modulation strategies leveraging variable switching frequency have also been

reported [147]. Nonetheless, all proposed DAB control methods are characterized by inherent performance trade-offs between overall RMS current stress (i.e., related to conduction losses) and ZVS capability (i.e., related to switching losses), requiring complex modulation strategies that are difficult to implement in practice and may be sensitive to parameter variation. Furthermore, the most valuable DAB feature of enabling bidirectional power flow is not exploited in the present application, making the four additional active switches very difficult to justify both in terms of cost and increased complexity (i.e., the secondary-side transistors must be supplied and driven on the other side of the converter isolation barrier).

Overall, the series-parallel resonant LLC converter provides the most promising converter-level performance for the present application. The main advantages of this topology can be summarized in: ZVS of the input inverter transistors and ZCS of the output rectifier diodes across the complete converter operating region, wide output voltage regulation capability with a relatively small switching frequency variation, capacitive converter output (i.e., requiring semiconductors with lower voltage rating and reducing the output filtering requirements with respect to the PSFB) and limited EMI generation, due to the converter resonant operation (i.e., no hard-switching, low $^{\mathrm{d}i}/_{\mathrm{d}t}$).

5.1.2 Key Challenges

Despite all of its proven advantages, the LLC converter poses significant challenges because of its complex multi-resonant nature, thus still representing an active research topic for both industry and academia. In particular, this converter is difficult to analyze and design due to its multiple operational modes [127, 133, 148–150]. Moreover, the inherent converter characteristics prevent to control it by switching frequency variation at light load and low output voltage, although this limitation may be overcome with burst-mode [151] or phase-shift/duty-cycle regulation [152, 153]. Finally, the tight output current control required in battery charging applications can be extremely challenging, since the converter resonant nature causes drastic system transfer function variations when moving away from the resonance frequency [154, 155]. For instance, in the present application the LLC converter is subject to the input DC-link voltage oscillation at three times the grid frequency generated by the three-level active rectifier (cf. **Section 2.4.2**). The rejection of this voltage ripple requires high output current control bandwidth and consistent control performance across the complete converter operating region, which are both hard to achieve in practice (cf. **Chapter 7**).

Part of the content of this chapter has been published in [156] and [157].

5.2 Operating Principle

The equivalent circuit schematic of the LLC resonant converter is shown in **Fig. 5.2**. A full-bridge inverter and a full-bridge rectifier are considered in this work, as explained in **Section 6.1.1**, nevertheless all considerations can be extended to other LLC topologies (i.e., with different input/output bridges) by simply adapting the amplitudes of the applied voltage square-waves.

The LLC converter may be functionally subdivided into different subsystems, namely the input source, the inverter bridge, the resonant tank, the diode rectifier bridge and the output load, as illustrated in **Fig. 5.3**.

The inverter bridge generates an output square wave v_{inv} consisting of a fundamental component and an infinite number of harmonics:

$$v_{\mathrm{inv}}(t) = \frac{4}{\pi} V_{\mathrm{i}} \sin(2\pi f_{\mathrm{sw}} t) + \sum_{h=3,5,7,..}^{\infty} \frac{4}{n\pi} V_{\mathrm{i}} \sin(h 2\pi f_{\mathrm{sw}} t)\,, \tag{5.1}$$

where f_{sw} is the inverter switching frequency and h is the harmonic order. Although the two inverter bridge-legs may be operated with a phase shift, leading to an additional degree of freedom (i.e., a zero-voltage state) in the generation of the voltage square-wave [152, 153, 158], in this work the inverter is assumed to be controlled only by frequency modulation with a fixed 50 % duty cycle, limiting the complexity of the modulator and simplifying both the system analysis and the converter design.

The resonant tank consists of a resonant capacitor C_{r}, a resonant inductor L_{r} and an isolation transformer featuring a $n:1$ turns ratio and a primary-referred magnetizing inductance value L_{m}. Due to the combination of one capacitive element and two inductive

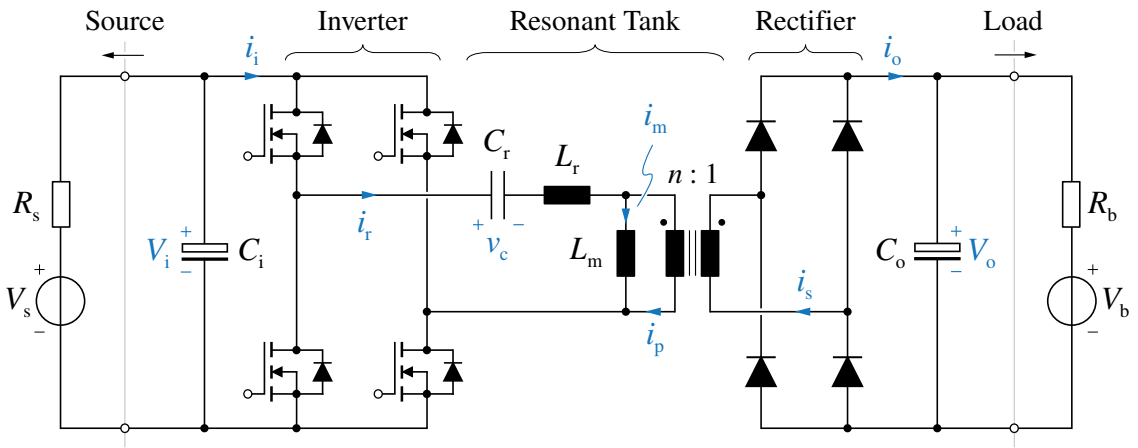


Fig. 5.2: Equivalent circuit schematic of the considered LLC resonant converter with full-bridge inverter and full-bridge rectifier. The input source (i.e., the DC-link of the AC/DC stage) and the output load (i.e., the battery) are modeled as ideal voltage sources with an internal series resistance.

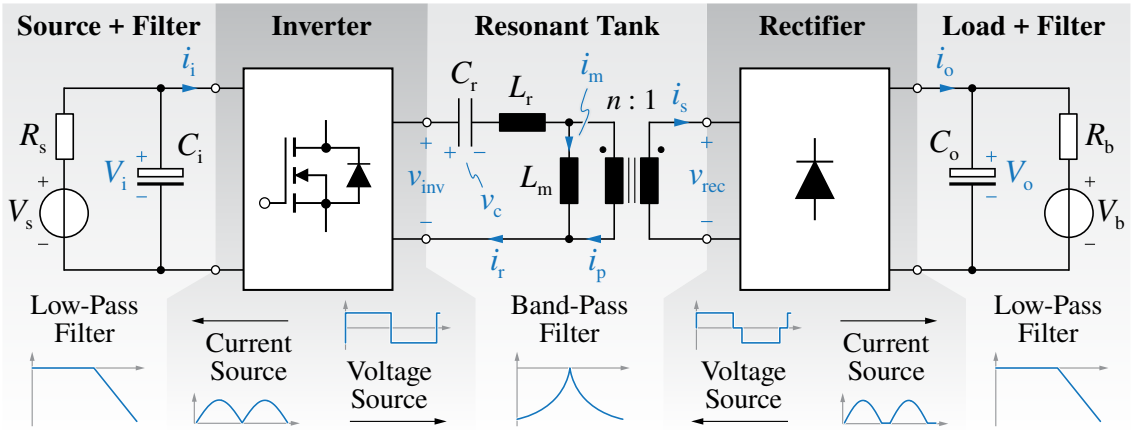


Fig. 5.3: Schematic diagram of the considered LLC resonant converter system, subdivided into input source (+ filter), inverter bridge, resonant tank, rectifier bridge and output load (+ filter).

elements, the equivalent impedance of the resonant tank is frequency dependent (i.e., allowing for the input/output voltage gain regulation by varying f_{sw}, cf. **Section 5.2.1**) and features two resonance frequencies, i.e.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}, \qquad f_m = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}}. \tag{5.2}$$

In particular, the system is characterized by inductive behavior (i.e., increasing impedance) for frequency values higher than f_r. Therefore, the harmonics contained in the inverter voltage square-wave get heavily attenuated (i.e., being $h f_{sw} \gg f_r$), leading to a pseudo-sinusoidal resonant current i_r [126].

The difference between the resonant current i_r and the magnetizing current i_m flows to the secondary side of the transformer (i.e., i_s) and is rectified by the diode bridge into i_o. In turn, the rectifier bridge generates a voltage square-wave v_{rec} (i.e., synchronized with i_s) across the transformer terminals.

Finally, the output load (i.e., consisting of a filter capacitor C_o in parallel to the battery R_b, V_b) provides a low-pass filtering action that attenuates the harmonics contained in i_o, making sure that only the DC current component flows into the battery.

Because of the high order of the system and the current/voltage discontinuities introduced by the diode rectifier operation, the accurate time-domain analysis (TDA) of the converter is extremely complicated and requires the solution of cumbersome and/or non-linear mathematical equations [127, 133, 148–150, 159]. With the goal of providing a straightforward understanding of the converter operation and derive simple analytical expressions of the converter component stresses, a simplified approach based on a sinusoidal approximation of the state variables is described in the following.

5.2.1 First Harmonic Approximation (FHA)

Due to the high selectivity of the resonant tank impedance, the first harmonic of the square-wave input voltage (5.1) dominates the LLC converter power transfer. In fact, the filtering action of the high-frequency inductive impedance allows to neglect the harmonics of the tank variables (i.e., $h = 3,5,7,...$) without incurring in a significant loss of accuracy [135]. Therefore, a first harmonic approximation (FHA) can be performed, converting all AC voltages and currents in pure sinusoidal quantities [126]. In a similar way, due to the low-pass filtering action of the input and output capacitors, the input and output currents can be approximated with their average (i.e., DC) value.

The voltage applied by the inverter is therefore expressed as

$$v_{\mathrm{inv}}(t) \approx \frac{4}{\pi} V_{\mathrm{i}} \sin(2\pi f_{\mathrm{sw}} t)\,, \tag{5.3}$$

leading to a resonant tank current equal to

$$i_{\mathrm{r}}(t) \approx I_{\mathrm{r}} \sin(2\pi f_{\mathrm{sw}} t - \varphi)\,, \tag{5.4}$$

where I_{r} is the peak current value and φ is the phase shift between voltage and current (i.e., determined by the total impedance seen from the inverter side). The average input current I_{i} can be thus obtained as

$$I_{\mathrm{i}} = \frac{2}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}/2} i_{\mathrm{r}}(t)\,\mathrm{d}t = \frac{2}{\pi} I_{\mathrm{r}} \cos\varphi. \tag{5.5}$$

Similarly, the expression of the rectified output voltage is

$$v_{\mathrm{rec}}(t) \approx \frac{4}{\pi} V_{\mathrm{o}} \sin(2\pi f_{\mathrm{sw}} t - \gamma)\,, \tag{5.6}$$

which is in phase with the transformer secondary current (i.e., due to the rectifier operation)

$$i_{\mathrm{s}}(t) \approx I_{\mathrm{s}} \sin(2\pi f_{\mathrm{sw}} t - \gamma)\,. \tag{5.7}$$

Both $v_{\mathrm{rec}}(t)$ and $i_{\mathrm{s}}(t)$ are phase-shifted by an angle γ with respect to the inverter voltage $v_{\mathrm{inv}}(t)$. The average output current is thus obtained as

$$I_{\mathrm{o}} = \frac{2}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}/2} |i_{\mathrm{s}}(t)|\,\mathrm{d}t = \frac{2}{\pi} I_{\mathrm{s}}. \tag{5.8}$$

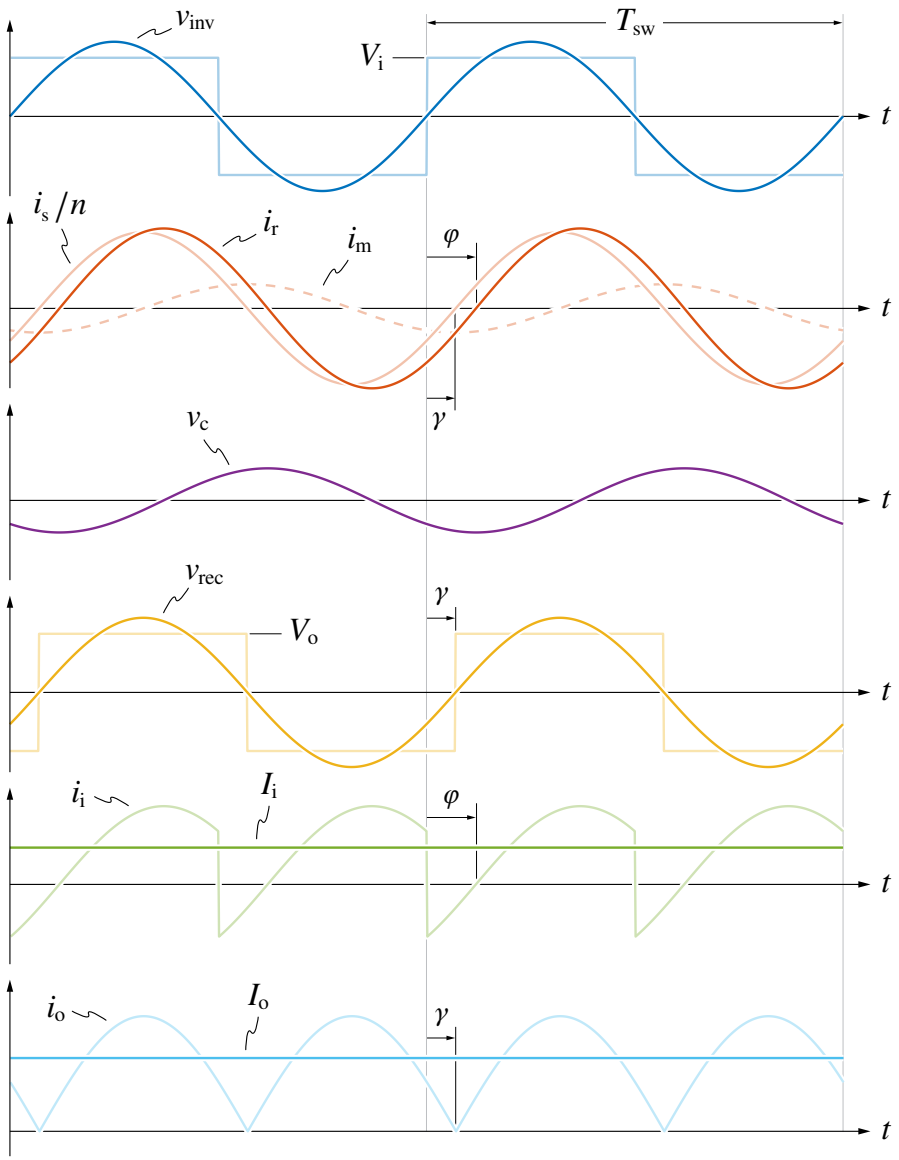


Fig. 5.4: Simplified LLC converter waveforms considering FHA.

All converter waveforms, simplified according to FHA, are illustrated in **Fig. 5.4**.

Since $v_{rec}(t)$ and $i_s(t)$ are in phase, the output rectifier appears as an equivalent resistive load to the resonant tank circuit [135], equal to

$$R = n^2 \frac{v_{rec}(t)}{i_s(t)} = \frac{4n^2}{\pi} \frac{V_o}{I_s} = \frac{8n^2}{\pi^2} \frac{V_o}{I_o}. \tag{5.9}$$

Therefore, according to FHA, the LLC resonant converter system can be represented with the simplified equivalent circuit shown in **Fig. 5.5**, where conventional AC circuit analysis can be applied.

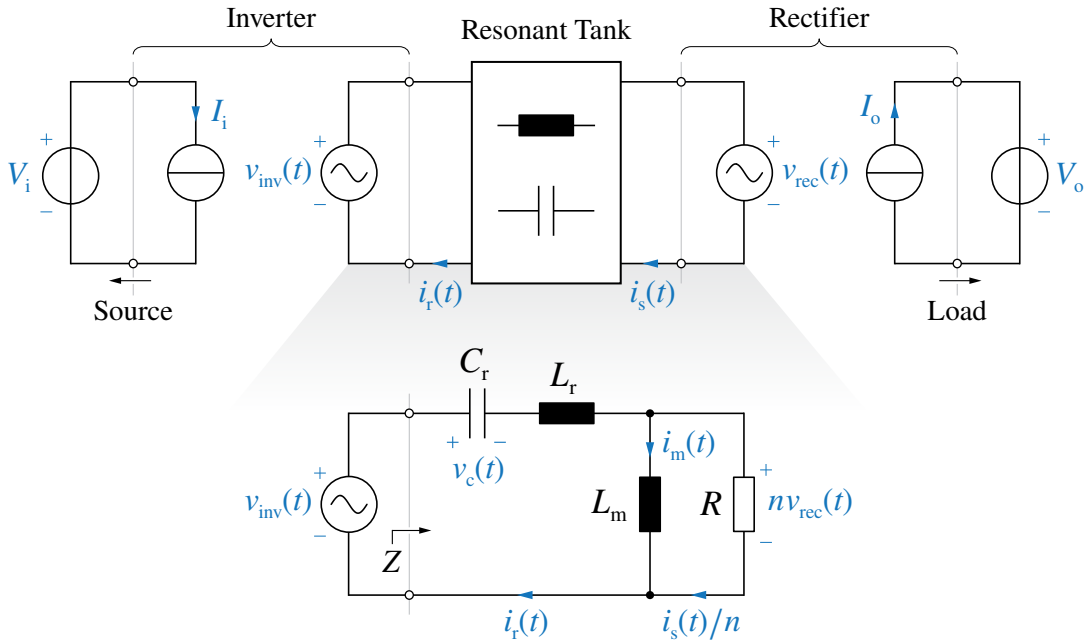


Fig. 5.5: Simplified equivalent circuit of the considered LLC resonant converter according to FHA.

The expression of the equivalent impedance Z seen from the inverter side (cf. **Fig. 5.5**) is obtained as

$$Z = \frac{1}{j2\pi f_{sw} C_r} + j2\pi f_{sw} L_r + \left(\frac{1}{R} + \frac{1}{j2\pi f_{sw} L_m}\right)^{-1}, \tag{5.10}$$

which is both load-dependent (i.e., R) and frequency-dependent (i.e., f_{sw}), providing an opportunity to regulate the input/output voltage gain by varying the inverter switching frequency. Introducing the definitions of normalized switching frequency $f_n = f_{sw}/f_r$, characteristic impedance $Z_r = \sqrt{L_r/C_r}$, inductance ratio $\lambda = L_r/L_m$ and quality factor

$$Q = \frac{Z_r}{R} = Z_r \frac{\pi^2}{8n^2} \frac{I_o}{V_o}, \tag{5.11}$$

the impedance expression in (5.10) can be expressed as [128]

$$Z(f_n, Q) = Z_r \left[\frac{f_n^2 Q}{\lambda^2 + f_n^2 Q^2} + j\left(\frac{\lambda f_n}{\lambda^2 + f_n^2 Q^2} - \frac{1 - f_n^2}{f_n}\right)\right], \tag{5.12}$$

which is illustrated in **Fig. 5.6(a)** in terms of magnitude and phase assuming $\lambda = 1/4$.

The voltage gain of the converter can be therefore obtained by analyzing the impedance divider between the resonant tank and the output load, as

$$M = \frac{nV_o}{V_i} = \frac{1}{|Z|} \left|\frac{1}{R} + \frac{1}{j2\pi f_{sw} L_m}\right|^{-1}. \tag{5.13}$$

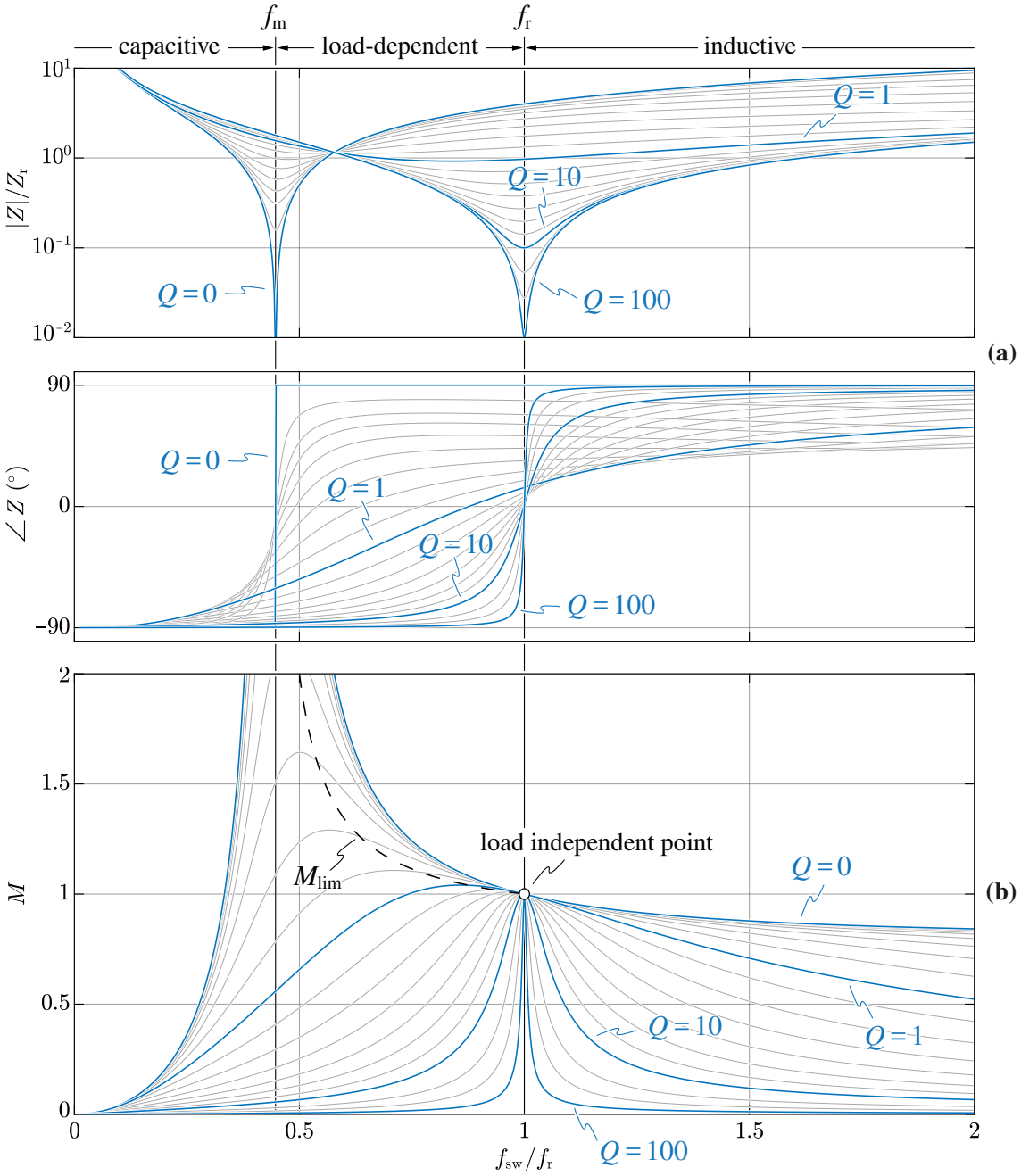


Fig. 5.6: LLC resonant converter **(a)** normalized input impedance Z/Z_r magnitude and phase, and **(b)** input/output voltage gain M for $\lambda = 1/4$, as functions of the normalized switching frequency f_n and the quality factor Q. The capacitive, inductive and load-dependent regions are indicated, together with the boundary gain curve M_{lim} between inductive and capacitive regions (i.e., the ZVS limit).

Therefore, substituting (5.9), (5.12) and the introduced definitions into (5.13), the following expression is derived [128]:

$$M(f_n, Q) = \frac{1}{\sqrt{\left(1+\lambda-\frac{\lambda}{f_n^2}\right)^2 + Q^2\left(f_n-\frac{1}{f_n}\right)^2}}, \tag{5.14}$$

which is graphically illustrated in **Fig. 5.6(b)**, also assuming $\lambda = 1/4$. As expected, once the converter design is defined (i.e., λ, f_r and Z_r are fixed), the voltage gain depends on the switching frequency, which represents the control parameter. In particular, **Fig. 5.6(b)** shows that the converter voltage gain decreases with increasing switching frequency. This implies that, as the switching frequency is increased, the impedance of the resonant tank is increased (i.e., inductive behavior), leading to a larger voltage drop across the resonant tank circuit components and thus a lower output voltage. The opposite is also true, as the output voltage can be increased by reducing the switching frequency value.

It is worth noting that the FHA modeling approach well reflects the real operation of the system near the resonance frequency (i.e., $f_{sw} \approx f_r$, where the resonant tank selectivity is maximum), but its accuracy progressively decreases for $f_{sw} < f_r$ and $f_{sw} > f_r$, as the converter waveforms include increasing harmonic content [128, 159].

5.2.2 Operating Limits

According to **Fig. 5.6(a)**, the operating frequency range of the LLC converter can be subdivided into three main intervals. When the switching frequency is lower than f_m, the resonant tank impedance is always capacitive (i.e., negative phase). Vice-versa, the impedance is always inductive (i.e., positive phase) when $f_{sw} > f_r$. The third interval is found in between, where the resonant tank impedance can be either capacitive or inductive, depending on the output load value. The two extremes are represented by the no-load or open-circuit condition (i.e., $Q = 0$) and the infinite-load or short-circuit condition (i.e., $Q = \infty$).

Identifying the phase of the input impedance (i.e., the phase shift between v_{inv} and i_r) is of primary importance to ensure the ZVS operation of the inverter bridge. For instance, when the impedance is inductive, the resonant tank current lags the inverter voltage square-wave, thus allowing for the soft turn-off of the transistors (cf. **Section 5.2.4**). The opposite is true in the capacitive region, which is characterized by hard-switching operation and must thus be avoided. Therefore, to ensure the correct operation of the LLC converter, all operating points must reside within the inductive impedance region. The boundary between capacitive and inductive impedance can be derived by setting the imaginary part of (5.12) to zero, deriving the value of Q and substituting it in (5.14), obtaining a load-independent expression [128]

$$M_{lim}(f_n) = \frac{f_n}{\sqrt{(1+\lambda)f_n^2 - \lambda}}, \tag{5.15}$$

which is graphically represented in **Fig. 5.6(a)**.

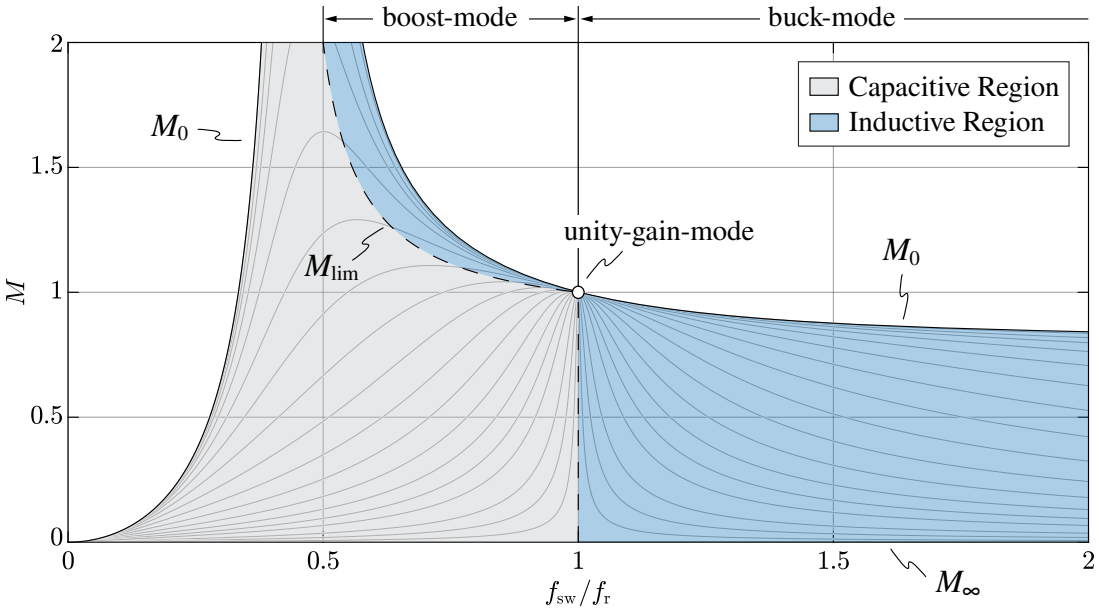


Fig. 5.7: Overview of capacitive and inductive operating regions of the LLC resonant converter in the (f_{n}, M) plane, assuming $\lambda = 1/4$. The boost-mode, unity-gain-mode and buck-mode frequency intervals are indicated, together with the boundary gain curve M_{lim} between inductive and capacitive regions (i.e., the ZVS limit), the open-circuit/no-load (i.e., $Q = 0$) characteristic M_0 and the short-circuit/infinite-load (i.e., $Q = \infty$) characteristic M_∞.

Therefore, the feasible operating region of the LLC converter is restricted between M_{lim} and the open-circuit/no-load (i.e., $Q = 0$) characteristic

$$M_0 = M(f_{\text{n}}, 0) = \frac{1}{\left| 1 + \lambda - \frac{\lambda}{f_{\text{n}}^2} \right|} \tag{5.16}$$

for $f_{\text{sw}} < f_{\text{r}}$, and between M_0 and the short-circuit/infinite-load (i.e., $Q = \infty$) characteristic

$$M_\infty = M(f_{\text{n}}, \infty) \approx 0 \tag{5.17}$$

for $f_{\text{sw}} > f_{\text{r}}$. The LLC converter feasible (i.e., inductive) operating region is highlighted in **Fig. 5.7**. Remarkably, all $M(f_{\text{n}}, Q)$ characteristics cross $M = 1$ for $f_{\text{n}} = 1$ (i.e., $f_{\text{sw}} = f_{\text{r}}$), where the voltage gain is not affected by the converter load.

5.2.3 Modes of Operation

The inductive region of the LLC resonant converter can be subdivided into three frequency intervals (cf. **Fig. 5.7**), namely $f_{\text{sw}} < f_{\text{r}}$, $f_{\text{sw}} = f_{\text{r}}$ and $f_{\text{sw}} > f_{\text{r}}$, which lead to different modes of operation.

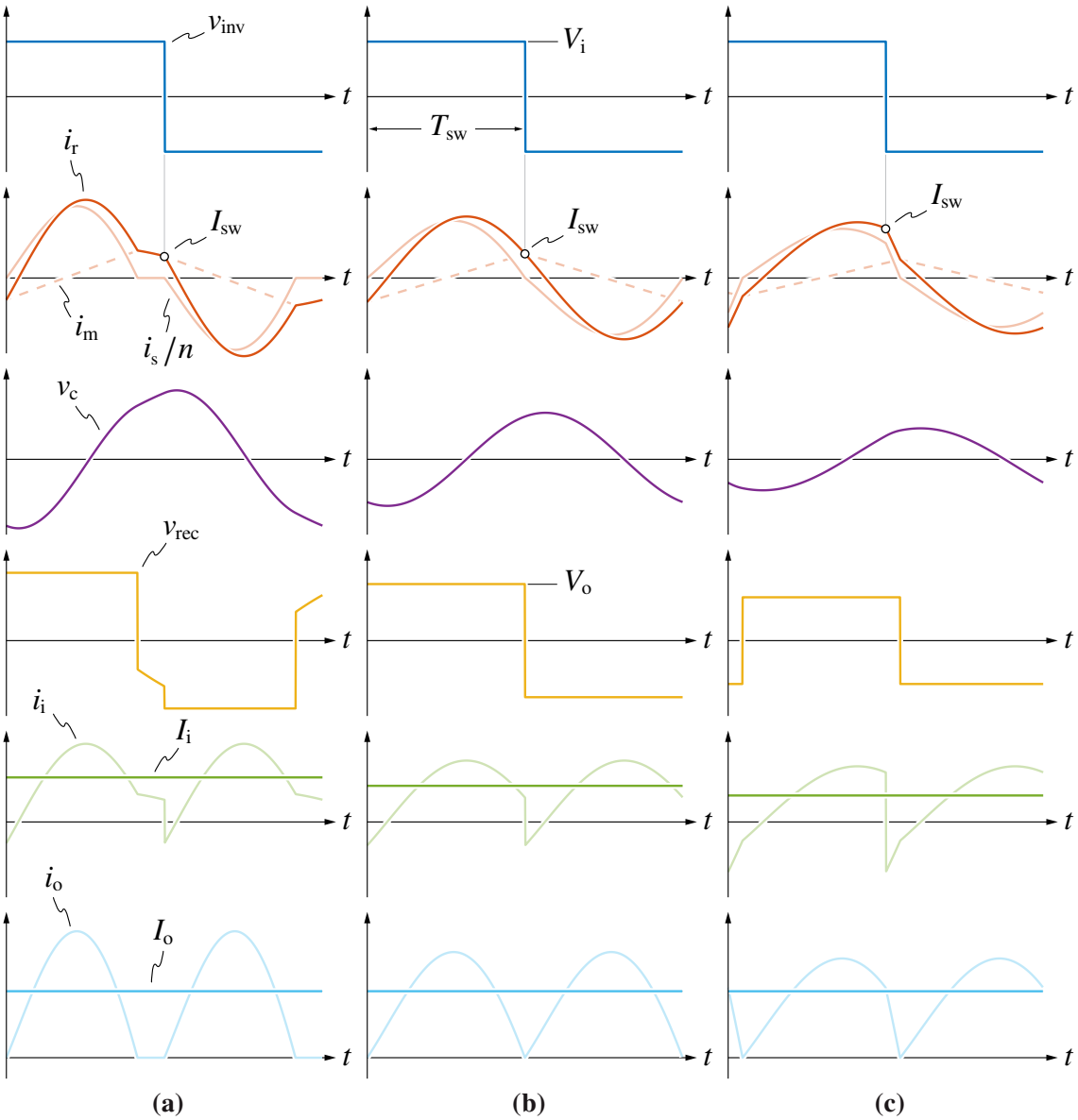


Fig. 5.8: Qualitative LLC converter waveforms obtained with TDA in **(a)** boost-mode ($f_{sw} < f_r$), **(b)** unity-gain-mode ($f_{sw} = f_r$) and **(c)** buck-mode ($f_{sw} > f_r$).

Boost-Mode ($f_{sw} < f_r$)

When the converter switching frequency f_{sw} is below the resonance frequency f_r the LLC voltage gain M is higher than 1 (cf. **Fig. 5.7**), therefore the converter operates in boost-mode (i.e., step-up operation). The qualitative waveforms in this operating mode are illustrated in **Fig. 5.8(a)**, showing that $T_{sw}/2$ can be divided in two distinct time intervals. At first, the series inductor L_r and the series capacitor C_r resonate together, while the magnetizing inductor L_m is clamped to the reflected output voltage nV_o. In this interval, the power is transferred from the source to the load and the current at the secondary-side of

the transformer has a sinusoidal shape with frequency f_r. Once the rectified output current i_o reaches zero (i.e., when the resonant current i_r reaches i_m at $t = 1/2f_r$), this interval ends and so does the power transfer. Since the output diode bridge is no longer active, the equivalent load is disconnected (i.e., the output current i_o is clamped to zero) and the primary circuit transitions to a resonance between C_r and $L_r + L_m$ (i.e., with frequency f_m). Being $f_m \ll f_r$, the magnetizing current i_m remains approximately constant and the voltage across C_r rises linearly, up to when the input voltage is inverted at $t = T_{sw}/2$.

Since the converter output operates in discontinuous conduction mode (DCM), the total RMS current stress on the active and passive components increases as f_{sw} is reduced, as the peak output current is increased and the magnetizing current circulation time interval widens. Nevertheless, the DCM operation allows to reduce the switching stress on the output diode bridge, as discussed in **Section 5.2.4**.

Unity-Gain-Mode ($f_{sw} = f_r$)

When $f_{sw} = f_r$, $M = 1$ independently of the load (cf. **Fig. 5.7**), therefore the converter operates in unity-gain-mode. The qualitative waveforms in this operating mode are illustrated in **Fig. 5.8(b)**. Since the switching period and the $L_r C_r$ resonant period coincide, the power is continuously transferred from the source to the load and no DCM occurs. Furthermore, the magnetizing inductor is always clamped to the reflected output voltage $\pm n V_o$, thus leading to a triangular magnetizing current i_m.

This operating mode minimizes the RMS current stress on the active and passive components for a given power transfer level, meanwhile ensuring boundary conduction mode (BCM) operation at the output (i.e., reducing the switching stress on the diodes). Therefore, the maximum LLC converter efficiency is typically obtained for $f_{sw} \approx f_r$.

Buck-Mode ($f_{sw} > f_r$)

When $f_{sw} > f_r$, the LLC voltage gain M is lower than 1 (cf. **Fig. 5.7**), therefore the converter operates in buck-mode (i.e., step-down operation). The qualitative waveforms in this operating mode are illustrated in **Fig. 5.8(c)**. Since the switching period is lower than the $L_r C_r$ resonant period, the reflected load current does not have enough time to reach the magnetizing current level. Therefore, when the input voltage is inverted at $t = T_{sw}/2$, the resonant tank current i_r changes slope and rapidly reaches i_m, starting a new half cycle. As the output load is connected during the complete switching period (i.e., continuous power transfer), no DCM occurs and the magnetizing current has a triangular shape.

Similarly to unity-gain-mode, buck-mode ensures a low RMS current stress on the active and passive components (i.e., due to the BCM operation at the output). However, the slope of the output rectified current i_o is increased, leading to a higher switching stress on the output diodes (cf. **Section 5.2.4**).

5.2.4 Soft-Switching Mechanisms

When the LLC converter is correctly operated within the inductive region (cf. **Fig. 5.7**), the soft-switching of all semiconductor devices can be achieved. This feature makes the converter efficiency almost unaffected by switching losses and thus allows for high frequency operation.

Zero-Voltage Switching (ZVS)

The transistors of the input inverter bridge can be successfully operated in zero-voltage switching (ZVS) conditions when the resonant tank current i_r lags the input voltage square-wave (i.e., inductive behavior, cf. **Fig. 5.7**). In fact, the current switched by the inverter (i.e., I_{sw}) must be positive when v_{inv} transitions from $+V_i$ to $-V_i$ and negative when v_{inv} transitions from $-V_i$ to $+V_i$. Notably, the value of I_{sw} coincides with the magnetizing current in boost-mode and unity-gain-mode (cf. **Fig. 5.8(a)**, **(b)**), whereas it includes also the load current in buck-mode (cf. **Fig. 5.8(c)**).

Fig. 5.9 shows the step-by-step inverter switching transition from $+V_i$ to $-V_i$ when $I_{sw} > 0$ (i.e., i_r lagging v_{inv}). It is worth noting that the input voltage square-wave is generated by switching on simultaneously two diagonally placed transistors. Moreover,

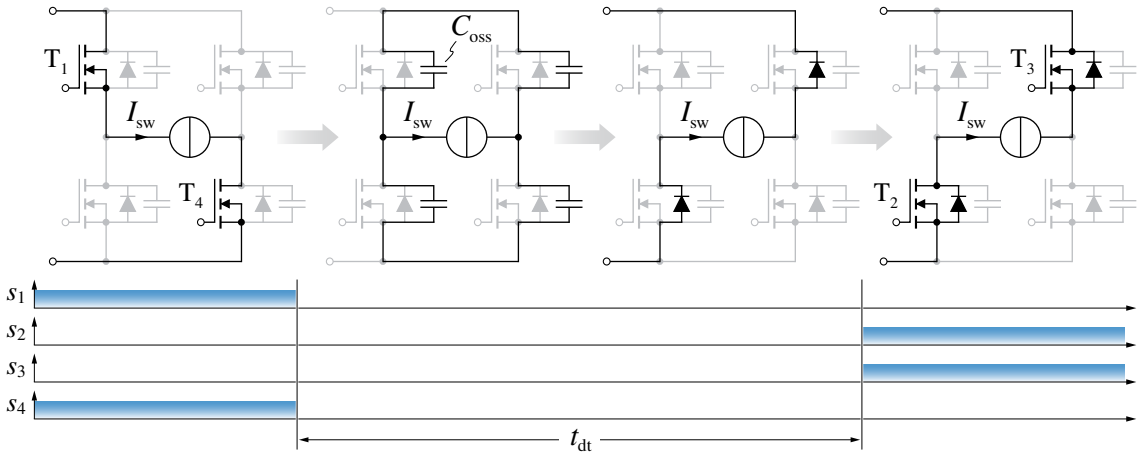


Fig. 5.9: Step-by-step ZVS transition from $v_{inv} = +V_i$ to $v_{inv} = -V_i$ with $I_{sw} > 0$ (i.e., $\varphi > 0$). s_1, s_2, s_3, s_4 are the gate signals of transistors T_1, T_2, T_3, T_4, respectively.

to prevent shoot-through phenomena within the bridge-legs and to make sure that the voltage transition is completed naturally (i.e., avoiding incomplete ZVS [160]), a sufficient dead time must be ensured between the turn-off and the turn-on signals of complementary switches. At first, transistors T_1 and T_4 are in the on-state. When the two transistors are turned off, the current deviates into the output capacitors (i.e., C_{oss}) of T_1, T_2, T_3 and T_4, charging/discharging them up to the point when the voltage transition is completed and the body diodes of T_2 and T_3 start conducting. Finally, once the dead time interval ends, transistors T_2 and T_3 are turned on in zero-voltage conditions (i.e., without loss) and the switching transition is completed. Similar considerations can be made for the inverter switching transition from $-V_i$ to $+V_i$ when $I_{sw} < 0$.

The phase lag between the inverter voltage square-wave and the resonant current is only a necessary condition to achieve ZVS. To make sure that the full voltage transition is completed naturally, the switched current I_{sw} must be high enough to charge/discharge the transistor output capacitances within the dead time interval t_{dt}, which translates into

$$t_{dt} I_{sw} \geq 2\, Q_{oss}(V_i), \tag{5.18}$$

where $Q_{oss}(V_i)$ is the total charge stored in the non-linear output capacitance C_{oss} of a transistor at V_i, defined as

$$Q_{oss}(V_i) = \int_0^{V_i} C_{oss}(v)\, \mathrm{d}v. \tag{5.19}$$

Fig. 5.10 shows the qualitative trends of C_{oss} and Q_{oss} as functions of the applied voltage for a typical Si MOSFET.

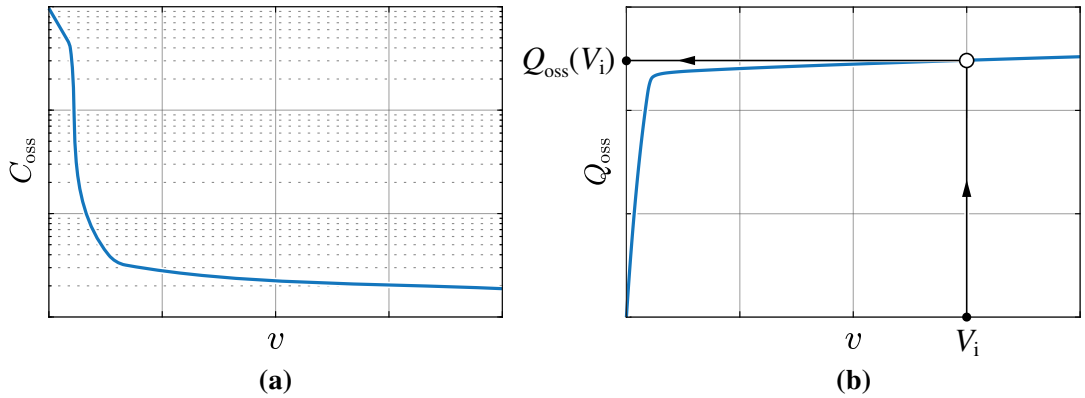


Fig. 5.10: Qualitative trends of the transistor **(a)** output capacitance C_{oss} (i.e., in semi-logarithmic scale) and **(b)** output charge Q_{oss} (i.e., in linear scale) as functions of the voltage applied across the transistor.

Allowing the transistor drain-source voltage to reach zero before the switch turns on allows to eliminate turn-on losses. However, turn-off losses are not completely eliminated, since for high switched current values a simultaneous overlap between the transistor drain-source voltage and channel current starts to appear [161]. Nonetheless, these losses can be kept to a minimum if the gate of the transistors is turned off fast enough and/or if the transistors feature a large value of C_{oss} (i.e., which acts as a turn-off snubber).

Zero-Current Switching (ZCS)

The diodes of the output rectifier bridge are always operated in soft-switching conditions, i.e., typically referred to as ZCS. In fact, they are naturally turned off by the output current, which features a relatively low $\mathrm{d}i/\mathrm{d}t$ (i.e., determined by the resonant tank) and thus provides time for the diode charge recombination process to take place, leading to negligible reverse-recovery with respect to hard-switching operation. Nevertheless, it is worth mentioning that in buck-mode operation the relatively high value of turn-off $\mathrm{d}i/\mathrm{d}t$ (cf. **Fig. 5.8(a)**), together with the high switching frequency (i.e., $f_{\mathrm{sw}} > f_{\mathrm{r}}$) can lead to significant rectifier switching losses, especially if high-voltage Si diodes are employed.

5.3 Component Stresses

The current and voltage stresses on the main active and passive converter components have a direct impact on the LLC converter design (cf. **Chapter 6**). In this section, all relevant component stresses are evaluated both analytically with FHA (i.e., providing easy-to-use expressions) and numerically with TDA (i.e., providing accurate results), which consists in solving the time-domain equations of the system state variables and is therefore equivalent to ideal circuit simulation [127, 133, 148–150, 159].

In the following, the component stresses are expressed as functions of f_{n} and Q for reasons of compactness, nonetheless they are graphically represented in the (f_{n}, M) plane for better understanding. It is worth noting that only two variables among f_{n}, Q and M are independent, since they are linked by (5.14). Therefore, all the expressions derived in the following can be represented in the (f_{n}, M) plane by simply leveraging the expression of Q obtained by inverting (5.14):

$$Q(f_{\mathrm{n}}, M) = \frac{\sqrt{\dfrac{1}{M^2} - \left(1 + \lambda - \dfrac{\lambda}{f_{\mathrm{n}}^2}\right)^2}}{\left| f_{\mathrm{n}} - \dfrac{1}{f_{\mathrm{n}}} \right|}. \tag{5.20}$$

To achieve compact FHA stress expressions, the amplitude and phase of the resonant tank current i_r (i.e., I_r, φ) and of the secondary-side transformer current i_s (i.e., I_s, γ) are expressed as functions of f_n and Q. The peak value of the resonant tank current I_r can be calculated as

$$I_r = \frac{4}{\pi}\frac{V_i}{|Z|} = \frac{4}{\pi}\frac{V_i}{Z_r}\sqrt{\frac{\frac{\lambda^2}{f_n^2}+Q^2}{\left(1+\lambda-\frac{\lambda}{f_n^2}\right)^2+Q^2\left(f_n-\frac{1}{f_n}\right)^2}}, \tag{5.21}$$

whereas I_s is obtained by inverting (5.8) and expressing I_o as function of Q, f_n and V_i, as

$$I_s = I_o\frac{\pi}{2} = \frac{4}{\pi}\frac{nV_i}{Z_r}\frac{Q}{\sqrt{\left(1+\lambda-\frac{\lambda}{f_n^2}\right)^2+Q^2\left(f_n-\frac{1}{f_n}\right)^2}}. \tag{5.22}$$

The phase shift angle between v_{inv} and i_r (i.e., φ) coincides with the phase of the input impedance expression in (5.12), as

$$\varphi = \tan^{-1}\left[\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}\right] = \tan^{-1}\left[\frac{f_n^4Q^2+f_n^2\left(\lambda^2+\lambda-Q^2\right)-\lambda^2}{f_n^3Q}\right], \tag{5.23}$$

whereas the phase between v_{inv} and i_s (i.e., γ) is found by analyzing the current divider between L_m and R in **Fig. 5.5**, as

$$\gamma = \varphi - \frac{\pi}{2} + \tan^{-1}\left(\frac{f_nQ}{\lambda}\right). \tag{5.24}$$

5.3.1 Semiconductor Devices

The transistors and the diodes employed in the LLC converter structure shown in **Fig. 5.2** (i.e., featuring a full-bridge inverter and a full-bridge rectifier) must be able to block the full input voltage V_i and the full output voltage V_o, respectively. Considering the maximum values of V_i and V_o set by the application (i.e., $V_{i,max} = 400\,V$, $V_{o,max} = 500\,V$, cf. **Section 6.1.1**) and taking into account a typical overvoltage safety margin of 50 % for the transistors (i.e., which can experience partial hard-switching) and of 20 % for the diodes (i.e., which always operate in soft-switching conditions) 600 V/650 V MOSFETs and diodes must be employed.

As mentioned in **Section 2.4.1**, the average (AVG) and root-mean-square (RMS) current stresses of all semiconductor devices are of interest, since they determine both the conduction losses and the switching losses (if any), thus also defining the semiconductor heat dissipation requirements. The current stresses in each transistor (T) and diode (D) can be calculated as

$$I_{\mathrm{T,AVG}} = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}/2} |i_{\mathrm{r}}(t)|\,\mathrm{d}t \approx \frac{1}{\pi} I_{\mathrm{r}}, \qquad I_{\mathrm{T,RMS}} = \sqrt{\frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}/2} i_{\mathrm{r}}^2(t)\,\mathrm{d}t} \approx \frac{1}{2} I_{\mathrm{r}}, \tag{5.25}$$

$$I_{\mathrm{D,AVG}} = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}/2} |i_{\mathrm{s}}(t)|\,\mathrm{d}t \approx \frac{1}{\pi} I_{\mathrm{s}}, \qquad I_{\mathrm{D,RMS}} = \sqrt{\frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}/2} i_{\mathrm{s}}^2(t)\,\mathrm{d}t} \approx \frac{1}{2} I_{\mathrm{s}}, \tag{5.26}$$

where I_{r} and I_{s} are reported in (5.21) and (5.22), respectively. **Fig. 5.11** shows the values of $I_{\mathrm{T,AVG}}$, $I_{\mathrm{T,RMS}}$ (i.e., normalized with respect to $V_{\mathrm{i}}/Z_{\mathrm{r}}$) and $I_{\mathrm{D,AVG}}$, $I_{\mathrm{D,RMS}}$ (i.e., normalized with respect to $nV_{\mathrm{i}}/Z_{\mathrm{r}}$) in the (f_{n}, M) plane assuming $\lambda = 1/4$. The results obtained with FHA (i.e., analytical expressions) and TDA (i.e., numerical/circuit simulation) are compared, showing that the results closely match each other around the resonance frequency. However it is observed that FHA becomes less and less accurate when moving away from f_{r}, especially for $f_{\mathrm{sw}} < f_{\mathrm{r}}$ (i.e., where the converter operates in DCM). **Fig. 5.11(b)** also shows that for $f_{\mathrm{n}} = 1$ (i.e., $f_{\mathrm{sw}} = f_{\mathrm{r}}$) the voltage gain becomes load dependent for low values of Q (i.e., as opposed to FHA, cf. **Fig. 5.11(a)**) and the feasible operating region in boost-mode is significantly narrower with respect to the one estimated by FHA, meaning that the converter can be regulated with a lower switching frequency variation.

Another important parameter is the switched current I_{sw}, which affects the ZVS transitions of the inverter bridge and the transistor turn-off losses (cf. **Section 5.2.4**). The expression of I_{sw} is simply obtained as

$$I_{\mathrm{sw}} = i_{\mathrm{r}}\left(\frac{T_{\mathrm{sw}}}{2}\right) \approx I_{\mathrm{r}} \sin(\pi - \varphi), \tag{5.27}$$

where I_{r} and φ are reported in (5.21) and (5.23), respectively. $I_{\mathrm{sw}}(f_{\mathrm{n}}, M)$ is shown in **Fig. 5.12** (i.e., normalized with respect to $V_{\mathrm{i}}/Z_{\mathrm{r}}$) for both FHA and TDA, assuming $\lambda = 1/4$. It is observed that the results show good agreement for $f_{\mathrm{sw}} \geq f_{\mathrm{r}}$, however FHA increasingly loses accuracy for $f_{\mathrm{sw}} < f_{\mathrm{r}}$.

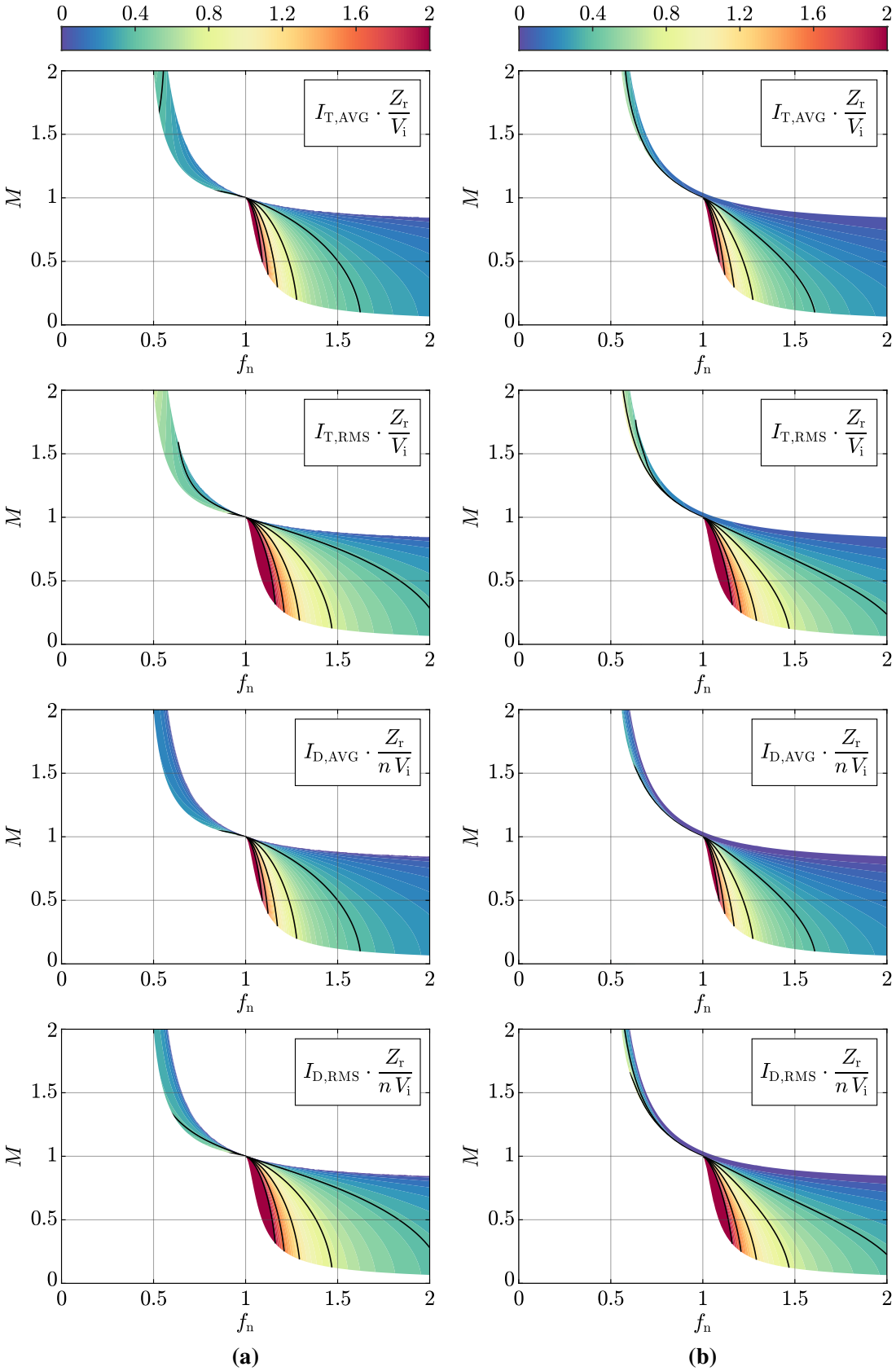


Fig. 5.11: Average and RMS current stresses on each transistor (i.e., $I_{\mathrm{T,AVG}}$, $I_{\mathrm{T,RMS}}$, normalized with respect to $V_\mathrm{i}/Z_\mathrm{r}$) and diode (i.e., $I_{\mathrm{D,AVG}}$, $I_{\mathrm{D,RMS}}$, normalized with respect to $nV_\mathrm{i}/Z_\mathrm{r}$) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_\mathrm{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

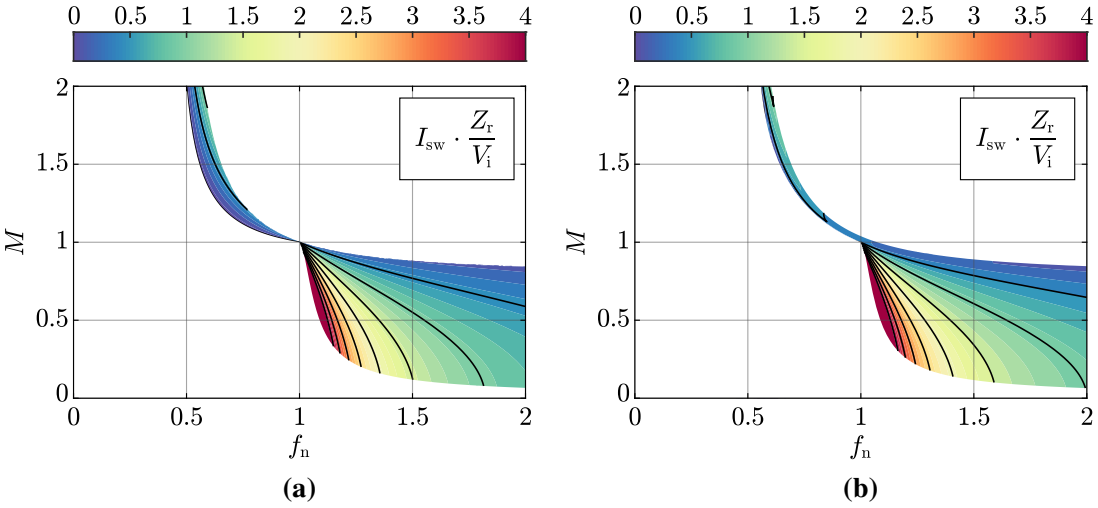


Fig. 5.12: Inverter switched current I_{sw} (i.e., normalized with respect to V_i/Z_r) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

Conduction Losses

The average conduction losses of each semiconductor device can be estimated leveraging its conduction characteristic $v(i, T_j)$ (i.e., provided in the manufacturer datasheet), the instantaneous current i flowing through it, and the instantaneous semiconductor junction temperature T_j, as

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v(i, T_j)\, i \, dt. \tag{5.28}$$

In particular, approximate expressions of the conduction losses can be obtained by considering simplified conduction characteristics (cf. **Fig. 2.14(a)**) as in (2.49). Substituting (2.49) into (5.28) and considering the average and RMS current stresses derived in (5.25)–(5.26), the following simplified conduction loss expressions are obtained:

$$P_{cond,T} \approx R_T I_{T,RMS}^2 \approx R_T \frac{I_r^2}{4}, \tag{5.29}$$

$$P_{cond,D} \approx V_D I_{D,AVG} + R_D I_{D,RMS}^2 \approx V_D \frac{I_s}{\pi} + R_D \frac{I_s^2}{4}. \tag{5.30}$$

Therefore, the total converter conduction losses are obtained as the sum of all transistor and diode losses, i.e.

$$P_{cond,tot} = 4 \left(P_{cond,T} + P_{cond,D} \right). \tag{5.31}$$

Switching Losses

As described in **Section 5.2.4**, all semiconductor devices (i.e., transistors and diodes) successfully achieve soft-switching when the LLC converter is properly designed and operates within the inductive region. Nonetheless, both transistors and diodes can generate a certain amount of switching losses. For instance, the MOSFETs of the input inverter bridge experience turn-off losses for switched current values higher than a given threshold, which depends on the device itself and the gate driving conditions [161]. Moreover, the output rectifier diodes are affected by reverse-recovery losses, however these can typically be neglected due to the low turn-off $\mathrm{d}i/\mathrm{d}t$ values determined by the resonant tank.

The switching losses of one transistor can be estimated as:

$$P_{\mathrm{sw,T}} = f_{\mathrm{sw}} \left[E_{\mathrm{on}}(I_{\mathrm{sw}}, V_{\mathrm{sw}}) + E_{\mathrm{off}}(I_{\mathrm{sw}}, V_{\mathrm{sw}}) \right] \approx f_{\mathrm{sw}} E_{\mathrm{off}}(I_{\mathrm{sw}}, V_{\mathrm{sw}}), \tag{5.32}$$

where I_{sw} is the switched current, $V_{\mathrm{sw}} = V_{\mathrm{i}}$ is the switched voltage and E_{on}, E_{off} are the turn-on and turn-off switching energies, respectively. In particular, E_{on} can be neglected when operating in ZVS conditions.

Similarly to conduction losses, approximate expressions of the switching losses can be derived by considering simplified switching energy characteristics (cf. **Fig. 2.14(b)**). The considered loss model is linear with respect to the switched voltage V_{sw} and quadratic with respect to the switched current I_{sw}. However, differently from the T-type rectifier in **Section 2.4.1**, when operating in ZVS conditions the energy stored in C_{oss} (i.e., the output capacitance of the transistor) must be subtracted to the turn-off switching energy, leading to a piece-wise defined expression [150, 161]

$$E_{\mathrm{off}} \approx \begin{cases} 0 & I_{\mathrm{sw}} \leq I_{\mathrm{sw,0}} \\ V_{\mathrm{sw}} \left(k_{0,\mathrm{off}} + k_{1,\mathrm{off}} I_{\mathrm{sw}} + k_{2,\mathrm{off}} I_{\mathrm{sw}}^2 \right) & I_{\mathrm{sw}} > I_{\mathrm{sw,0}} \end{cases}, \tag{5.33}$$

where $I_{\mathrm{sw,0}}$ is the threshold current value below which lossless switching is achieved and $k_{0,\mathrm{off}}$, $k_{1,\mathrm{off}}$, $k_{2,\mathrm{off}}$ are suitable parameters that best fit the real switching energy characteristics.

Therefore, substituting (5.33) into (5.32), the switching losses of one transistor can be expressed as

$$P_{\mathrm{sw,T}} \approx \begin{cases} 0 & I_{\mathrm{sw}} \leq I_{\mathrm{sw,0}} \\ f_{\mathrm{sw}} V_{\mathrm{sw}} \left(k_{0,\mathrm{off}} + k_{1,\mathrm{off}} I_{\mathrm{sw}} + k_{2,\mathrm{off}} I_{\mathrm{sw}}^2 \right) & I_{\mathrm{sw}} > I_{\mathrm{sw,0}} \end{cases}. \tag{5.34}$$

In conclusion, neglecting the reverse-recovery losses of the secondary-side rectifier diodes, the total converter switching losses are obtained by adding together the switching losses of the four transistors, as

$$P_{\mathrm{sw,tot}} = 4\,P_{\mathrm{sw,T}}. \tag{5.35}$$

5.3.2 Resonant Capacitor

The resonant capacitor C_r must be able to withstand the total RMS current stress (i.e., related to losses and temperature rise) and the peak voltage (i.e., which may cause the breakdown of the capacitor itself).

RMS Current

The resonant capacitor is subject to the resonant tank current i_r, leading to the following RMS current stress:

$$I_{\mathrm{C_r,RMS}} = \sqrt{\frac{1}{T_\mathrm{sw}}\int_0^{T_\mathrm{sw}} i_\mathrm{r}^2(t)\,\mathrm{d}t} \approx \frac{I_\mathrm{r}}{\sqrt{2}}, \tag{5.36}$$

where I_r is reported in (5.21). $I_{\mathrm{C_r,RMS}}(f_\mathrm{n}, M)$ is shown in **Fig. 5.13** in normalized form for both FHA and TDA, assuming $\lambda = 1/4$.

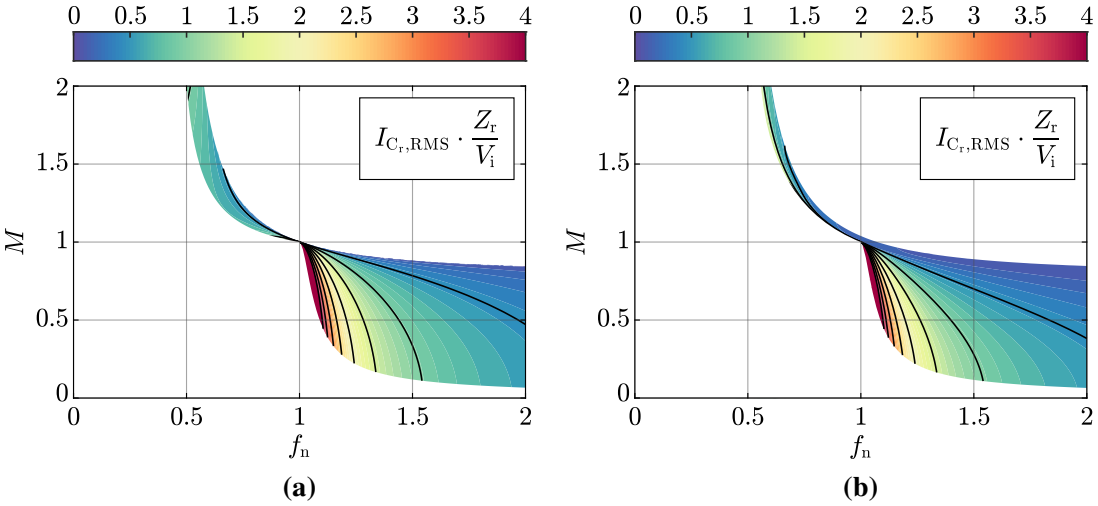


Fig. 5.13: Resonant capacitor RMS current stress $I_{\mathrm{C_r,RMS}}$ (i.e., normalized with respect to $V_\mathrm{i}/Z_\mathrm{r}$) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_\mathrm{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA. The same current stress is applied to the resonant inductor and the primary-side of the transformer (i.e., $I_{\mathrm{C_r,RMS}} = I_{\mathrm{L_r,RMS}} = I_{\mathrm{T_p,RMS}}$).

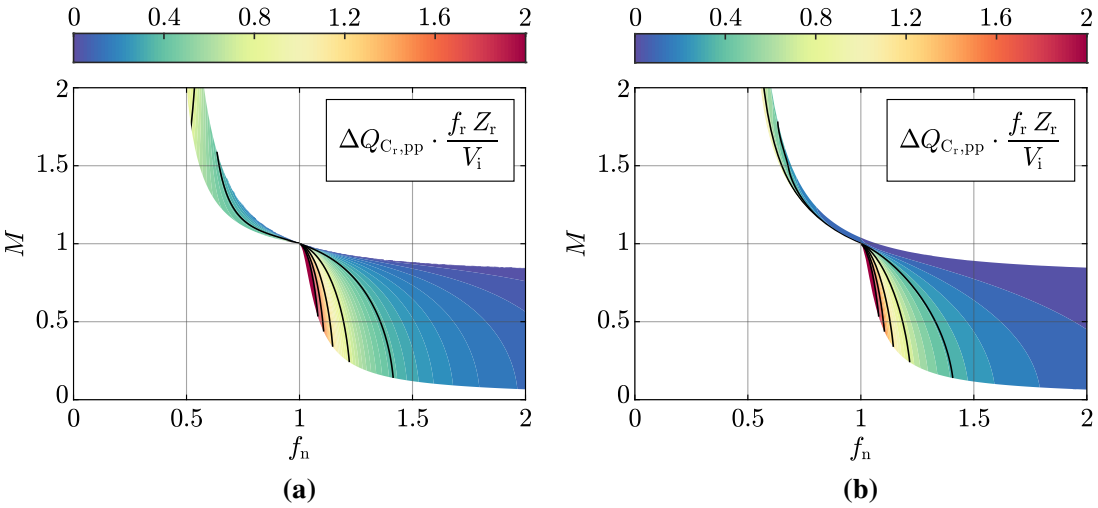


Fig. 5.14: Resonant capacitor peak-to-peak charge swing $\Delta Q_{C_r,pp}$ (i.e., normalized with respect to $V_i/(f_r Z_r)$) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

Peak-to-Peak Charge Swing

The peak-to-peak charge swing in the resonant capacitor must comply with the capacitor breakdown voltage, as $\Delta Q_{C_r,pp}/2 \leq C_r V_{C_r,max}$. The value of $\Delta Q_{C_r,pp}$ can be obtained as

$$\Delta Q_{C_r,pp} = \int_0^{T_{sw}/2} |i_r(t)|\,dt \approx \frac{1}{f_r}\frac{I_r}{\pi f_n}. \tag{5.37}$$

$\Delta Q_{C_r,pp}(f_n, M)$ is normalized with respect to $V_i/(f_r Z_r)$ and is shown in **Fig. 5.14** for both FHA and TDA, assuming $\lambda = 1/4$.

5.3.3 Resonant Inductor

The resonant inductor L_r must be able to withstand the total RMS current stress, which translates into winding losses, and the peak-to-peak flux density swing in the core, which generates core losses and must not exceed the saturation flux density of the material.

RMS Current

Being in series with the resonant capacitor, L_r is subject to the same current stress, i.e.

$$I_{L_r,RMS} = I_{C_r,RMS} \approx \frac{I_r}{\sqrt{2}}, \tag{5.38}$$

which is illustrated graphically in **Fig. 5.13** as function of f_n and M.

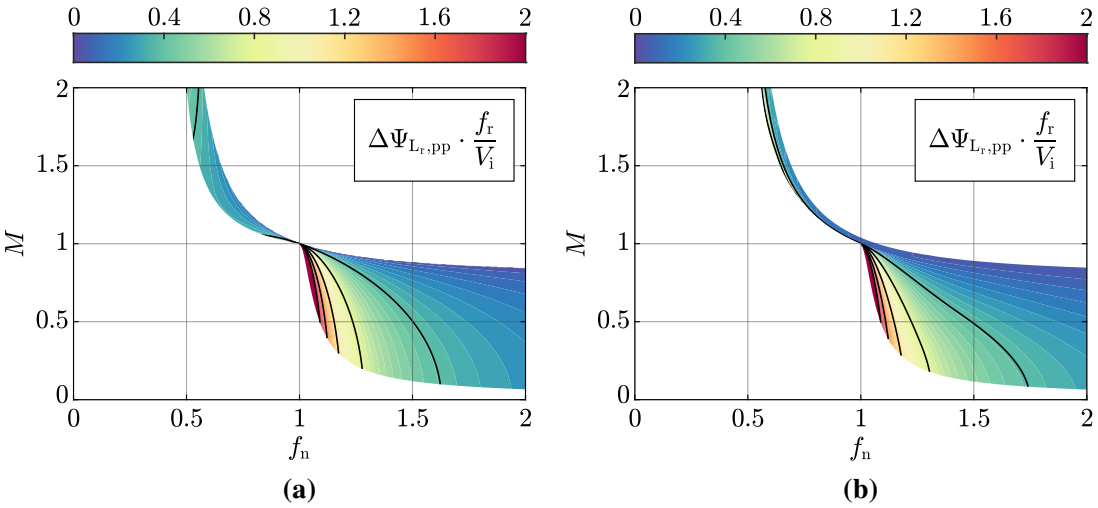


Fig. 5.15: Resonant inductor peak-to-peak flux swing $\Delta\Psi_{\mathrm{L_r,pp}}$ (i.e., normalized with respect to $V_\mathrm{i}/f_\mathrm{r}$) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_\mathrm{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

Peak-to-Peak Flux Swing

The expression of the inductor peak-to-peak flux swing can be obtained as

$$\Delta\Psi_{\mathrm{L_r,pp}} = 2L_\mathrm{r} \max\left[i_\mathrm{r}(t)\right] \approx \frac{Z_\mathrm{r}}{f_\mathrm{r}} \frac{I_\mathrm{r}}{\pi}. \tag{5.39}$$

$\Delta\Psi_{\mathrm{L_r,pp}}(f_\mathrm{n}, M)$ is normalized with respect to $V_\mathrm{i}/f_\mathrm{r}$ and is shown in **Fig. 5.15** for both FHA and TDA, assuming $\lambda = 1/4$.

5.3.4 Transformer

The isolation transformer must be able to withstand the total RMS current stresses both at the primary-side and the secondary-side, which translate into winding losses, and the peak-to-peak flux density swing in the core, which generates core losses and must not exceed the saturation flux density of the material.

RMS Current

The primary-side of the transformer takes part into the resonant tank and is thus subject to the total resonant current i_r, therefore

$$I_{\mathrm{T_p,RMS}} = I_{\mathrm{C_r,RMS}} \approx \frac{I_\mathrm{r}}{\sqrt{2}}, \tag{5.40}$$

which is illustrated graphically in **Fig. 5.13** as function of f_n and M.

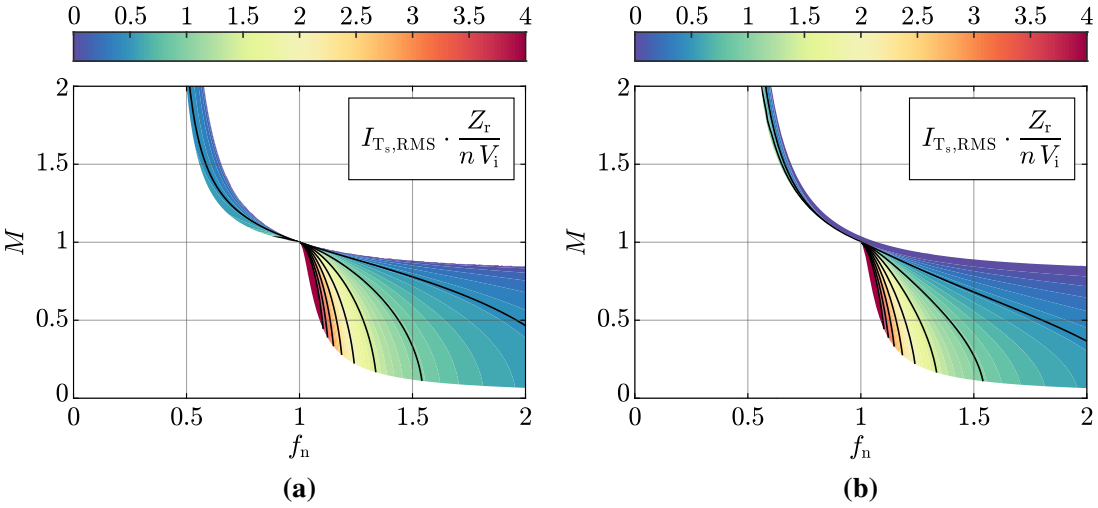


Fig. 5.16: Transformer secondary-side RMS current stress $I_{\mathrm{T_s,RMS}}$ (i.e., normalized with respect to $nV_\mathrm{i}/Z_\mathrm{r}$) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_\mathrm{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

The secondary-side of the transformer, instead, is not affected my the magnetizing current component, leading to the following RMS current stress expression:

$$I_{\mathrm{T_s,RMS}} = \sqrt{\frac{1}{T_\mathrm{sw}} \int_0^{T_\mathrm{sw}} i_\mathrm{s}^2(t)\,\mathrm{d}t} \approx \frac{I_\mathrm{s}}{\sqrt{2}}. \tag{5.41}$$

$I_{\mathrm{T_s,RMS}}(f_\mathrm{n}, M)$ is normalized with respect to $nV_\mathrm{i}/Z_\mathrm{r}$ and is shown in **Fig. 5.16** for both FHA and TDA, assuming $\lambda = 1/4$.

Peak-to-Peak Flux Swing

The expression of the transformer (i.e., magnetizing inductor L_m) peak-to-peak flux swing can be obtained as

$$\Delta\Psi_{\mathrm{L_m,pp}} = 2L_\mathrm{m} \max\left[i_\mathrm{m}(t)\right] \approx \frac{Z_\mathrm{r}}{f_\mathrm{r}} \frac{I_\mathrm{m}}{\pi\lambda}, \tag{5.42}$$

where

$$I_\mathrm{m} = \sqrt{I_\mathrm{r}^2 - \frac{I_\mathrm{s}^2}{n^2}}. \tag{5.43}$$

$\Delta\Psi_{\mathrm{L_m,pp}}(f_\mathrm{n}, M)$ is normalized with respect to $V_\mathrm{i}/f_\mathrm{r}$ and is shown in **Fig. 5.17** for both FHA and TDA, assuming $\lambda = 1/4$.

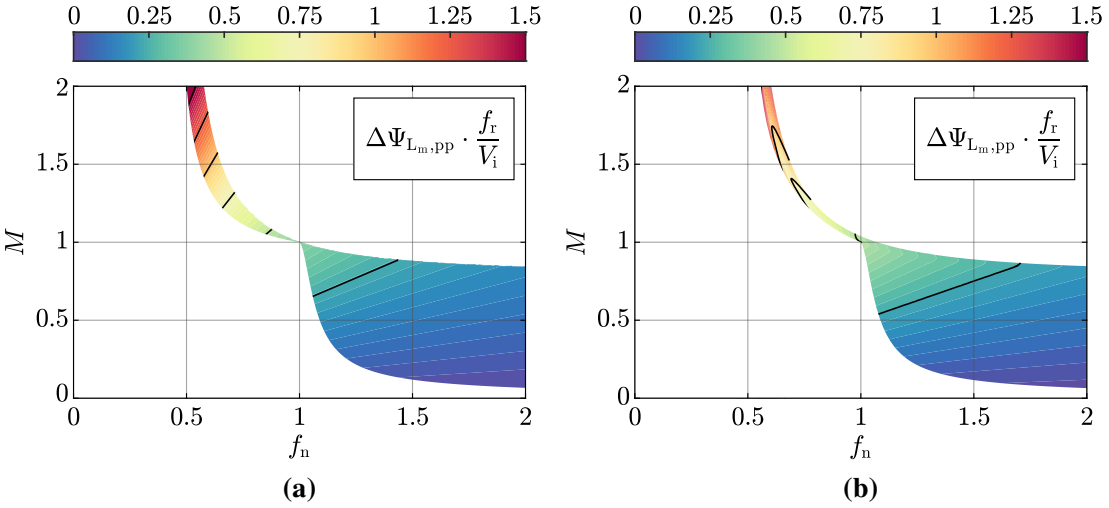


Fig. 5.17: Transformer peak-to-peak flux swing $\Delta\Psi_{L_m,pp}$ (i.e., normalized with respect to V_i/f_r) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

5.3.5 Input Filter Capacitor

The input filter capacitor C_i must simultaneously satisfy two main design criteria. First, it must be able to withstand the maximum RMS current stress defined by the application, which generates losses and affects the capacitor temperature rise. Moreover, it must ensure a predefined maximum peak-to-peak voltage ripple, which increases the peak voltage applied to the semiconductor devices and alters the ideal operation of the converter.

RMS Current

The capacitor current stress can be calculated as

$$I_{C_i,RMS} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i_i^2(t)\,dt - I_i^2} \approx I_r \sqrt{\frac{1}{2} - \frac{4}{\pi}\cos^2\varphi} \tag{5.44}$$

where I_r and φ are reported in (5.21) and (5.23), respectively. $I_{C_i,RMS}(f_n, M)$ is normalized with respect to V_i/Z_r and is shown in **Fig. 5.18** for both FHA and TDA, assuming $\lambda = 1/4$.

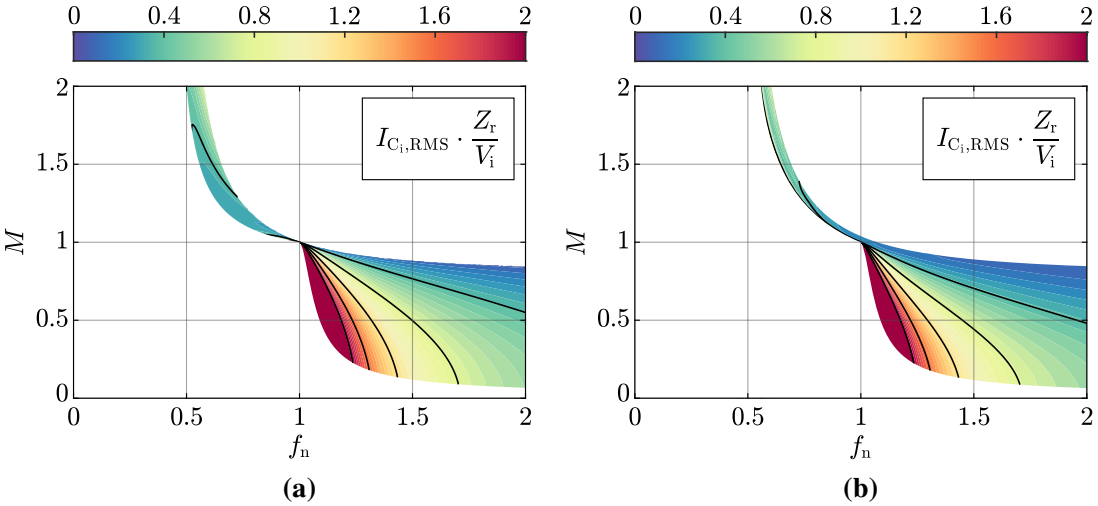


Fig. 5.18: Input filter capacitor RMS current stress $I_{C_i,RMS}$ (i.e., normalized with respect to V_i/Z_r) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

Peak-to-Peak Charge Ripple

The capacitor peak-to-peak charge ripple $\Delta Q_{C_i,pp}$ is directly proportional to the voltage ripple $\Delta V_{i,pp}$ and can be expressed as

$$\Delta Q_{C_i,pp} = \int_{t_0}^{t_1} |I_i - i_i(t)| \, dt \tag{5.45}$$

where t_0 and t_1 are the time instants within the first half-cycle when $i_i(t) = I_i$, i.e.

$$t_0 \approx \frac{1}{f_r} \frac{1}{2\pi f_n} \left[\varphi + \sin^{-1}\left(\frac{2}{\pi} \cos\varphi \right) \right], \tag{5.46}$$

$$t_1 \approx \begin{cases} \dfrac{1}{f_r} \dfrac{1}{2f_n} \left[\varphi - \sin^{-1}\left(\dfrac{2}{\pi} \cos\varphi \right) + \pi \right] & \varphi \leq \tan^{-1}\left(\dfrac{2}{\pi} \right) \\ \dfrac{1}{f_r} \dfrac{1}{2f_n} & \varphi > \tan^{-1}\left(\dfrac{2}{\pi} \right) \end{cases}. \tag{5.47}$$

Therefore, the following expression is obtained:

$$\Delta Q_{C_i,pp} \approx \frac{1}{f_r} \frac{I_r}{2\pi f_n} \left[\frac{2}{\pi} \cos\varphi \left(k_\varphi \, \varphi + \sin^{-1}\left(\frac{2}{\pi} \cos\varphi \right) - \frac{\pi}{2} \right) + \sqrt{1 - \frac{4}{\pi^2} \cos^2\varphi} \right], \tag{5.48}$$

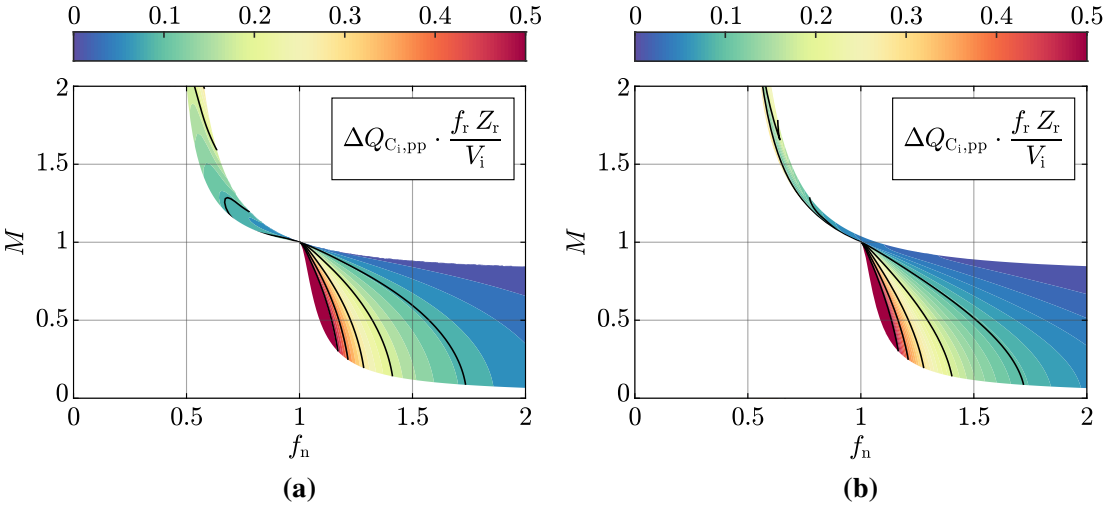


Fig. 5.19: Input filter capacitor peak-to-peak charge ripple $\Delta Q_{C_i,pp}$ (i.e., normalized with respect to $V_i/(f_r Z_r)$) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

where $k_\varphi = 0$ for $\varphi \leq \tan^{-1}(2/\pi)$, whereas $k_\varphi = 1$ for $\varphi > \tan^{-1}(2/\pi)$. $\Delta Q_{C_i,pp}(f_n, M)$ is normalized with respect to $V_i/(f_r Z_r)$ and is shown in **Fig. 5.19** for both FHA and TDA, assuming $\lambda = 1/4$.

5.3.6 Output Filter Capacitor

The output filter capacitor C_o shares the same design criteria as C_i, namely it must comply with the maximum RMS current stress set by the application and must ensure a predefined maximum peak-to-peak voltage ripple.

RMS Current

The capacitor current stress can be calculated as

$$I_{C_o,RMS} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i_o^2(t)\,dt - I_o^2} \approx I_s \sqrt{\frac{1}{2} - \frac{4}{\pi^2}} \tag{5.49}$$

where I_s is reported in (5.22). $I_{C_o,RMS}(f_n, M)$ is normalized with respect to nV_i/Z_r and is shown in **Fig. 5.20** for both FHA and TDA, assuming $\lambda = 1/4$.

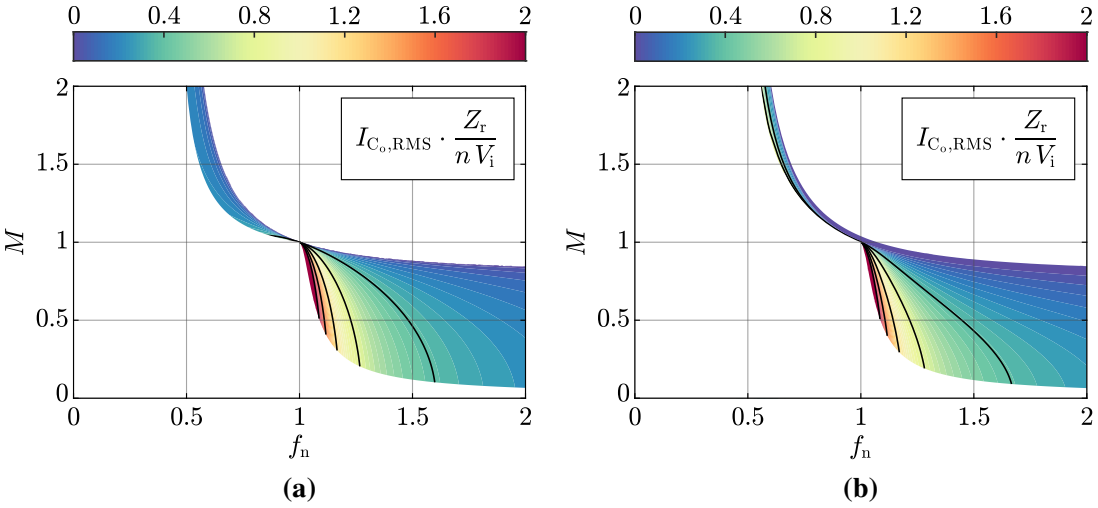


Fig. 5.20: Output filter capacitor RMS current stress $I_{C_o,RMS}$ (i.e., normalized with respect to nV_i/Z_r) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

Peak-to-Peak Charge Ripple

The expression of the capacitor peak-to-peak charge ripple is obtained as

$$\Delta Q_{C_o,pp} = \int_{t_2}^{t_3} |I_o - i_o(t)| \, dt \tag{5.50}$$

where t_2 and t_3 are the time instants within the first half-cycle when $i_o(t) = I_o$, i.e.

$$t_2 \approx \frac{1}{f_r} \frac{1}{2\pi f_n} \left[\gamma + \sin^{-1}\left(\frac{2}{\pi}\right) \right], \quad t_3 \approx \frac{1}{f_r} \frac{1}{2\pi f_n} \left[\gamma - \sin^{-1}\left(\frac{2}{\pi}\right) + \pi \right]. \tag{5.51}$$

Therefore, the following expression is obtained:

$$\Delta Q_{C_o,pp} \approx \frac{1}{f_r} \frac{2I_s}{\pi^2 f_n} \left[\sin^{-1}\left(\frac{2}{\pi}\right) + \frac{\pi}{2} \left(\sqrt{1 - \frac{4}{\pi^2}} - 1 \right) \right]. \tag{5.52}$$

$\Delta Q_{C_o,pp}(f_n, M)$ is normalized with respect to $nV_i/(f_r Z_r)$ and is shown in **Fig. 5.21** for both FHA and TDA, assuming $\lambda = 1/4$.

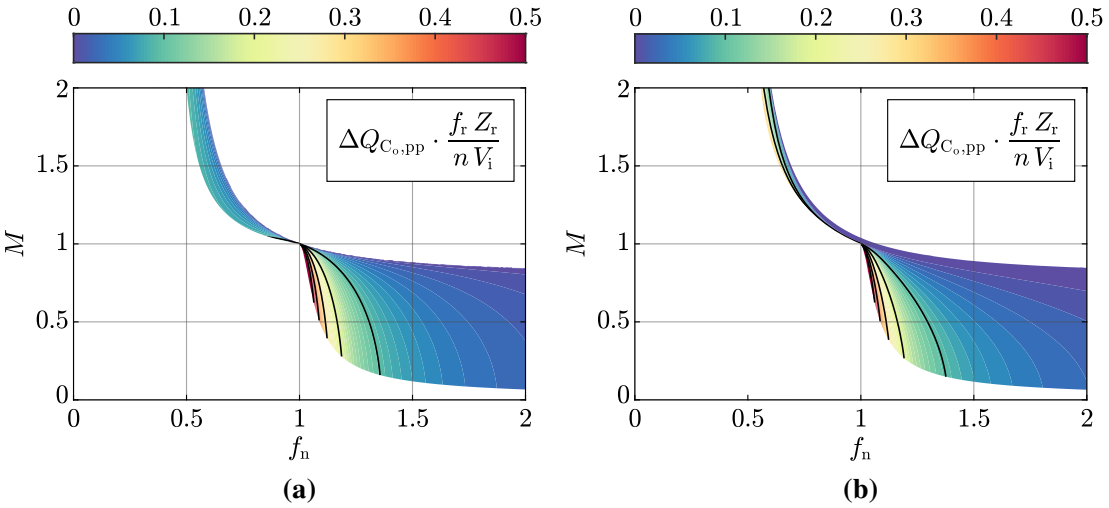


Fig. 5.21: Output filter capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{Co,pp}}$ (i.e., normalized with respect to $n V_\mathrm{i}/(f_\mathrm{r} Z_\mathrm{r})$) in the (f_n, M) plane assuming $\lambda = 1/4$ and $Q_\mathrm{max} = 10$: **(a)** estimated with FHA, **(b)** obtained with TDA.

5.4 Summary

In this chapter, a comprehensive analysis of the DC/DC conversion stage of the considered EV ultra-fast battery charger has been provided. A unidirectional resonant LLC converter topology has been selected for the present 4x15 kW application, in view of its promising features such as high conversion efficiency (i.e., due to the soft-switching operation of both primary-side transistors and secondary-side diodes) and wide output load/voltage regulation capability. The operational basics of the LLC converter have been described, with particular focus on the first harmonic approximation (FHA) analysis method. This simplified approach has been exploited to identify the converter feasible operating region in terms of switching frequency, input/output voltage gain and output load. For a better understanding, the LLC time-domain waveforms under boost-mode operation (i.e., below resonance), unity-gain-mode operation (i.e., at resonance) and buck-mode operation (i.e., above resonance) have been shown and described. Additionally, the zero-voltage switching (ZVS) mechanism of the primary-side transistors has been explained in detail and the zero-current switching (ZCS) operation of the secondary-side diodes has been briefly discussed. Finally, with the aim of providing straightforward tools for the design and assessment of the LLC converter, the stresses on the converter active and passive components (i.e., semiconductor devices, resonant capacitor, resonant inductor, transformer, input/output filter capacitors) have been derived analytically with FHA and calculated numerically with the more accurate time-domain analysis (TDA). Such comprehensive analytical assessment is currently not available in literature and is thus a contribution of this work.

Chapter 6

DC/DC Converter – Design

Abstract

The isolated DC/DC stage of an electric vehicle (EV) ultra-fast battery charger must simultaneously achieve high conversion efficiency and high power density, leading to a challenging power converter design. In this chapter, a novel iterative design procedure for resonant LLC converters is proposed and applied to the considered modular 4x15 kW application, aiming to minimize the total converter conduction losses. In view of the high target nominal power, an unconventional LLC circuit structure is adopted to split the current/voltage ratings of the magnetic components (i.e., resonant inductors, transformers) and the current rating of the output rectifier diodes (i.e., allowing for the adoption of discrete Si semiconductor devices). Once the main converter parameters are determined by the proposed design procedure, the selection, sizing and/or optimization of all main converter active and passive components is carried out, including the semiconductor devices, the resonant capacitor, the resonant inductors, the isolation transformers, the input/output filter capacitors and the heat dissipation system (i.e., heatsink and fans). Finally, a 15 kW LLC converter prototype is built and its performance in terms of loss and efficiency is assessed experimentally.

6.1 Introduction

As reported in **Section 5.1**, the isolated DC/DC stage of an EV ultra-fast charger must simultaneously ensure wide output load and voltage regulation capability, low battery-side current ripple, high conversion efficiency and high power density. In particular, the last two requirements demand for an accurate topology selection and a proper converter design.

The LLC resonant converter has been identified in **Section 5.1** as the most promising candidate among unidirectional isolated DC/DC topologies for the present application, providing an excellent trade-off between regulation capability and loss/efficiency performance. In particular, the LLC converter features the soft-switching operation of all semiconductor devices (i.e., transistors, diodes) across the complete converter operating region, a wide output voltage regulation capability with a relatively small switching frequency variation, a capacitive output filter and limited EMI noise emission. Nonetheless, the accurate design of LLC resonant converters poses significant challenges, due to the complex multi-resonant nature of the system and its multiple operating modes [127, 133, 148–150]. Moreover, the converter operation at high switching frequencies (i.e., to minimize the size and weight of resonant and/or filtering elements) requires special care in the design and realization of the magnetic components, since the simultaneous size reduction and loss increase can rapidly lead to exceed the winding and/or core thermal limits.

The design and assessment of LLC resonant converters has been extensively reported in literature [128–131, 133, 150, 162–167], however typically focusing on power applications up to the kW range. Among these solutions, [129–131, 133, 164, 167] specifically focus on LLC converter designs for EV battery charging. In particular, a straightforward step-by-step design procedure is provided in [129], where simple approximated expressions are exploited for the sizing and the loss estimation of all components. A 650 W prototype with Si MOSFETs and Si diodes is built, achieving a 96 % peak efficiency. The authors in [130] outline a design method based on FHA that ensures the ZVS operation of the primary-side transistors considering the worst-case operating point defined by the non-linear charging characteristic of a battery. The proposed approach is validated on a full-Si 3.3 kW prototype achieving a peak efficiency of 98.2 %, nevertheless no details on the semiconductor device selection and on the design of the magnetics are provided. In [131], an iterative design procedure exploiting both FHA and circuit simulation is described, providing a particular focus on the design/optimization of the resonant inductor and the isolation transformer. To verify the methodology, a 1 kW proof-of-concept with Si MOSFETs and Si diodes is realized, achieving a 95.4 % peak efficiency. Another iterative design approach is reported in [133], where TDA is exploited to achieve a better accuracy with respect to FHA (i.e., at the cost of higher computational effort). Basic analytical expressions are exploited to estimate the active and passive component losses, however no indication on the design of the magnetics is provided. A full-Si 3 kW converter prototype is built, achieving a peak efficiency of 95.2 %. It is worth noting that only few high-power (i.e., $\geq$ 10 kW) designs are reported in literature, mostly because of the challenges related to the design of the magnetic components. In [164], a full-Si 10 kW prototype achieving a peak efficiency around 96.5 % is presented, however the converter design process is not fully

described and no details are given on the design/sizing of the passive components (i.e., resonant capacitor, resonant inductor, isolation transformer, input/output filter capacitors). Finally, a 4x12.5 kW modular LLC converter design for EV off-board charging using SiC MOSFETs is reported in [167]. No details on the design process are provided, nonetheless the converter achieves a peak efficiency of 97.9 %, significantly exceeding the performance of comparable Si-based solutions.

Since high-power LLC converter designs are extremely rare in literature, the goal of this chapter is to provide a complete step-by-step methodology for the design of the considered modular 4x15 kW LLC resonant converter for EV ultra-fast battery charging. In particular, a straightforward iterative procedure for the identification of the main design parameters is proposed, aimed at minimizing the total converter conduction losses. Furthermore, the selection, design and/or optimization processes of all active and passive components are reported in detail and the adopted analytical/numerical models are described.

6.1.1 Specifications and Performance Targets

As explained in **Section 1.3**, the proposed 60 kW DC/DC converter stage is characterized by a modular structure (i.e., 4x15 kW), enabling the series/parallel reconfiguration of the converter modules and thus narrowing the output voltage regulation requirement of a single converter unit. The modular approach also allows to reduce the power rating of the units and to turn-off one or more modules at light-load operation, ensuring higher efficiency over the complete charging range.

The specifications and the performance targets of a single LLC converter unit are reported in **Tab. 6.1**. In particular, it is assumed that the converter input voltage V_i (i.e., $V_\mathrm{dc}/2$) is adjusted by the AC/DC converter stage between 325 V and 400 V, to minimize the required voltage gain range of the LLC. Furthermore, a nominal efficiency of $\geq 97\,\%$ is targeted.

Tab. 6.1: Specifications and performance targets of a single DC/DC converter unit.

Parameter	Description	Value
$P_\mathrm{o,nom} = P_\mathrm{o,max}$	nominal/maximum output power	15 kW
$I_\mathrm{o,nom} = I_\mathrm{o,max}$	nominal/maximum output current	37.5 A
$V_\mathrm{o,nom}$	nominal output voltage	400 V
V_o	output voltage range	250…500 V
V_i	input voltage range	325…400 V
η	target nominal efficiency	$\geq 97\,\%$

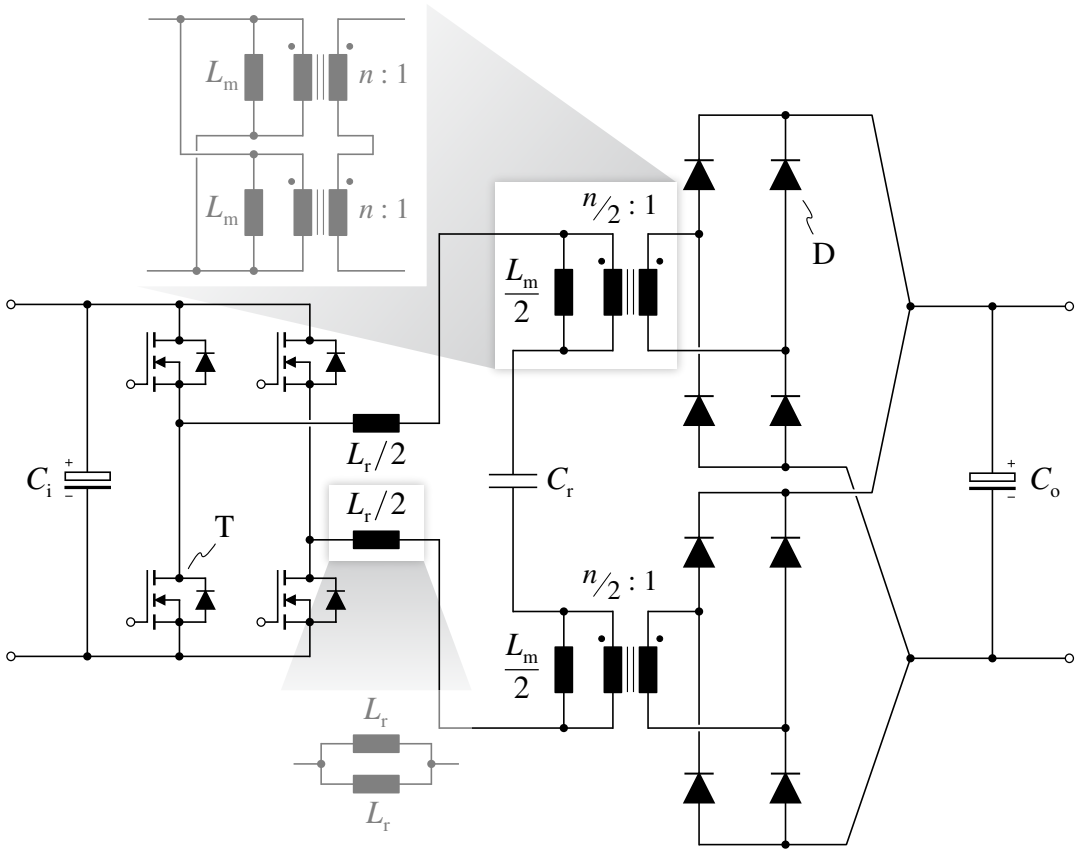


Fig. 6.1: Equivalent circuit schematic of the adopted LLC converter module structure.

In view of the high power rating of a single converter unit, the unconventional LLC circuit structure shown in **Fig. 6.1** is adopted. Two transformers (i.e., each consisting of two input-parallel/output-series units) are series-connected at the primary side and supply two separate diode bridges at the secondary side, which are then connected in parallel. This allows to both reduce the current/voltage ratings of the single transformers and halve the current rating of the output rectifier diodes, enabling the use of commercially available magnetic cores and discrete semiconductor devices. In particular, the modularization of the output diode bridge allows to avoid the static current sharing issues that affect conventional hard-paralleling. To ensure the balanced operation of the converter, the resonant inductor is split in two elements (i.e., each consisting of two parallel units) placed on the two resonant tank branches, whereas the resonant capacitor is connected between the transformers. A full-bridge inverter is considered, in order to halve the current rating of the semiconductor devices with respect to the half-bridge implementation. Similarly, full-bridge rectifiers are selected, since they allow for a simpler transformer construction and diodes with half rated voltage with respect to the center-tapped solution and allow to halve the diode current stress with respect to the voltage-doubler implementation [168].

Part of the content of this chapter has been published in [156].

6.2 Design Procedure

The common goal of all design procedures for LLC resonant converters is to identify the four parameters n, L_r, C_r and L_m that ensure the required converter input/output characteristics, meanwhile minimizing the losses and/or the size of the passive components. In this section, a novel iterative design approach based on FHA is described, aiming to minimize the converter conduction losses for a given set of constraints defined by the application. It is worth noting that, even though the adopted LLC circuit structure (cf. **Fig. 6.1**) apparently features higher complexity with respect to the conventional LLC circuit (cf. **Fig. 5.2**), the two topologies operate in the exact same way and are thus subject to the same design process.

Once the transformer turns ratio is defined, the LLC converter structure has three main degrees of freedom (i.e., L_r, C_r, L_m), which can be expressed as functions of the inductance ratio $\lambda = L_r/L_m$, the characteristic impedance $Z_r = \sqrt{L_r/C_r}$ and the primary resonance frequency $f_r = 1/(2\pi\sqrt{L_r C_r})$, defined in **Chapter 5**. Remarkably, analyzing the converter operation in the normalized frequency domain (i.e., as function of $f_n = f_{sw}/f_r$), the combination of λ and Z_r is sufficient to identify a single converter design. In particular, higher values of λ shrink the gain curves in the (f_n, M) plane (cf. **Fig. 6.2**), widening the regulation capability of the converter (i.e., achieving higher voltage gain at maximum load and lower voltage gain at minimum load for the same f_n range), however increasing the circulating/magnetizing current and thus reducing the converter efficiency (i.e., especially at light-load). On the other hand, Z_r does not affect the shape of the gain curves in the (f_n, M) plane but modifies their quality factor Q for a given load value (i.e., $Q = Z_r/R$). A lower value of Z_r provides increased maximum voltage gain for a given load level (cf. **Fig. 6.3**), however it also leads to higher circulating current and conduction losses.

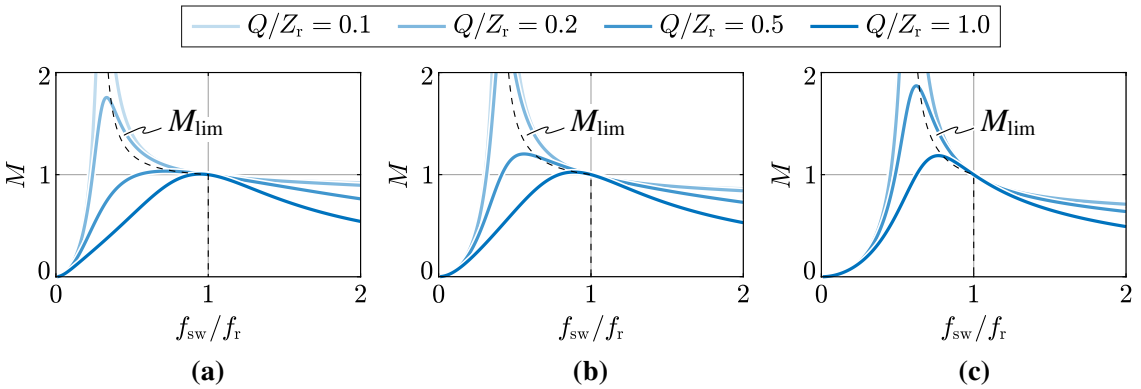


Fig. 6.2: FHA input/output voltage gain M as function of the normalized switching frequency f_n and the output load $Q/Z_r = 1/R$ for $Z_r = 1\,\Omega$ and **(a)** $\lambda = 0.1$, **(b)** $\lambda = 0.2$, **(c)** $\lambda = 0.5$.

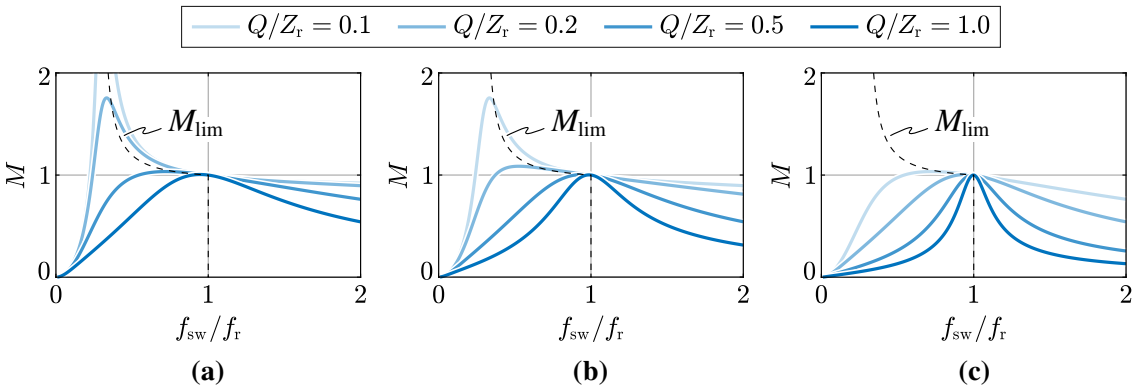


Fig. 6.3: FHA input/output voltage gain M as function of the normalized switching frequency f_n and the output load $Q/Z_r = 1/R$ for $\lambda = 0.1$ and **(a)** $Z_r = 1\,\Omega$, **(b)** $Z_r = 2\,\Omega$, **(c)** $Z_r = 5\,\Omega$.

The considered LLC design procedure iteratively changes the value of the resonance frequency f_r (i.e., the first degree of freedom) and calculates the optimal values of λ and Z_r (i.e., the remaining two degrees of freedom) that satisfy the given specifications. The iteration is ideally stopped once the value of f_r ensures that the converter operating region completely exploits the available switching frequency range. This translates in the minimization of the converter conduction losses for a given set of constraints defined by the application, as explained in the following. The proposed iterative design procedure consists of several steps, which are summarized in **Fig. 6.4**, namely:

① Definition of the design specifications and constraints. The specifications of the LLC module considered in this work are reported in **Table 6.1**. As mentioned in **Section 6.1.1**, it is assumed that the converter input voltage V_i is regulated by the AC/DC stage between 325 V and 400 V, to minimize the required voltage gain range of the LLC. The converter switching frequency is constrained within $f_{sw,min} = 100\,\text{kHz}$ and $f_{sw,max} = 250\,\text{kHz}$.

② Transformer turns ratio n selection. It is well known that the operation at resonance (i.e., unity-gain-mode) normally represents the highest efficiency working point of the LLC converter (cf. **Section 5.2.3**), since no recirculation time is present, i.e. reducing conduction losses with respect to boost-mode operation, and the reverse-recovery of the output diodes is minimized, i.e. reducing switching losses with respect to buck-mode operation. Therefore, unity-gain-mode ($M = 1$) is targeted for the nominal operating conditions (i.e., $V_{o,nom} = 400\,\text{V}$). According to the specifications reported in **Table 6.1**, this is obtained for every value $n \leq V_{i,max}/V_{o,nom} = 1$. Nonetheless, $n = 1$ is selected herein to simplify the transformer design and to maximize the converter efficiency within $V_o = 325$–$400\,\text{V}$ (i.e., 650–800 V when two LLC units are connected in series), representing the typical battery voltage range of most commercially available EVs [39, 169]. An overview of the input/output voltage gain M values obtained with $n = 1$ is reported in **Fig. 6.5**. A minimum gain $M_{min} = 0.77$ and a maximum gain $M_{max} = 1.25$ are obtained.

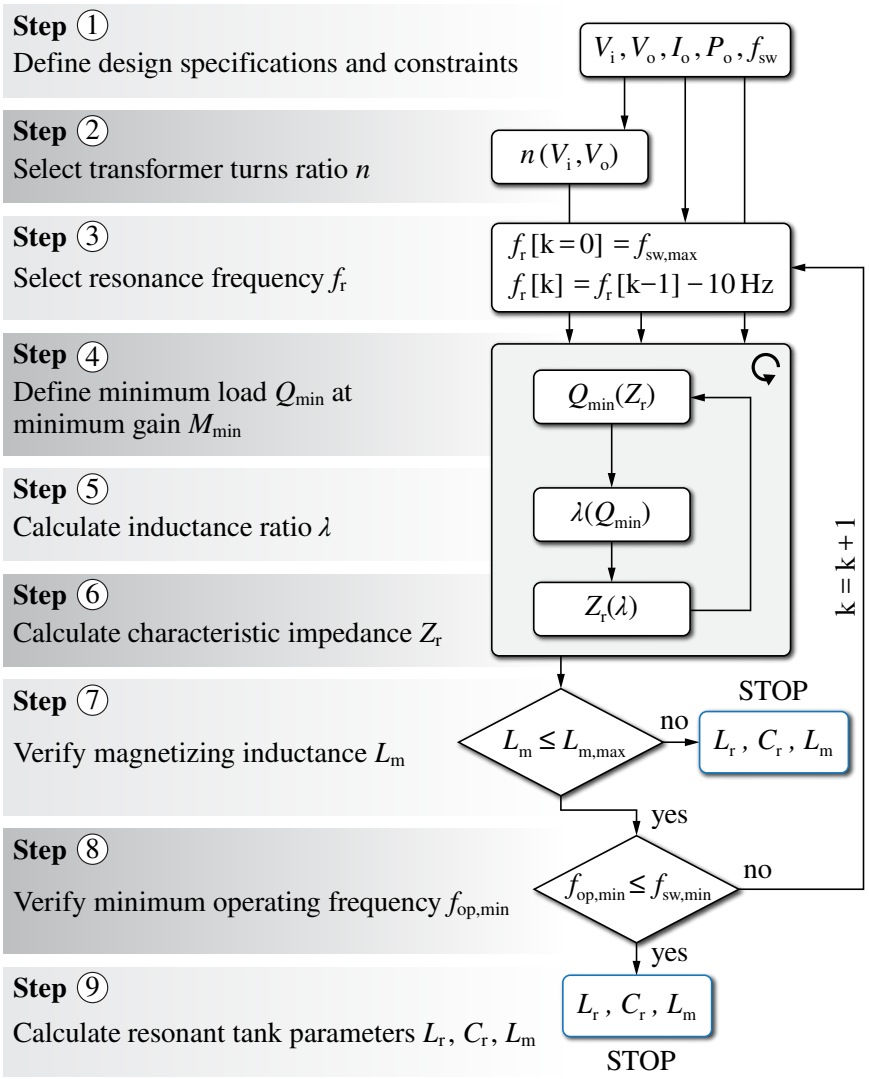


Fig. 6.4: Flowchart of the proposed LLC converter iterative design procedure.

③ Resonance frequency f_r selection. This value is initialized at the maximum possible switching frequency (i.e., $f_{sw,max} = 250\,kHz$), and is subject to successive iterations as shown in the design flowchart of **Fig. 6.4**. In particular, f_r is progressively reduced with 10 Hz steps until the converter operating frequency range coincides with $[f_{sw,min}, f_{sw,max}]$.

④ Minimum load Q_{min} at minimum gain M_{min} definition. To limit the buck-mode operating range of the converter, a minimum load at maximum frequency is considered. In this case, 25 % of the nominal current is assumed as $I_{o,min}$, since the modular charger is already split in four modules that can be selectively turned off at light-load. Unfortunately, the minimum quality factor expression depends on the characteristic impedance of the resonant tank, as

$$Q_{min}(V_{o,min}) = \frac{\pi^2}{8n^2} Z_r \frac{I_{o,min}}{V_{o,min}}, \tag{6.1}$$

therefore it is calculated by iterative means together with the two following design steps.

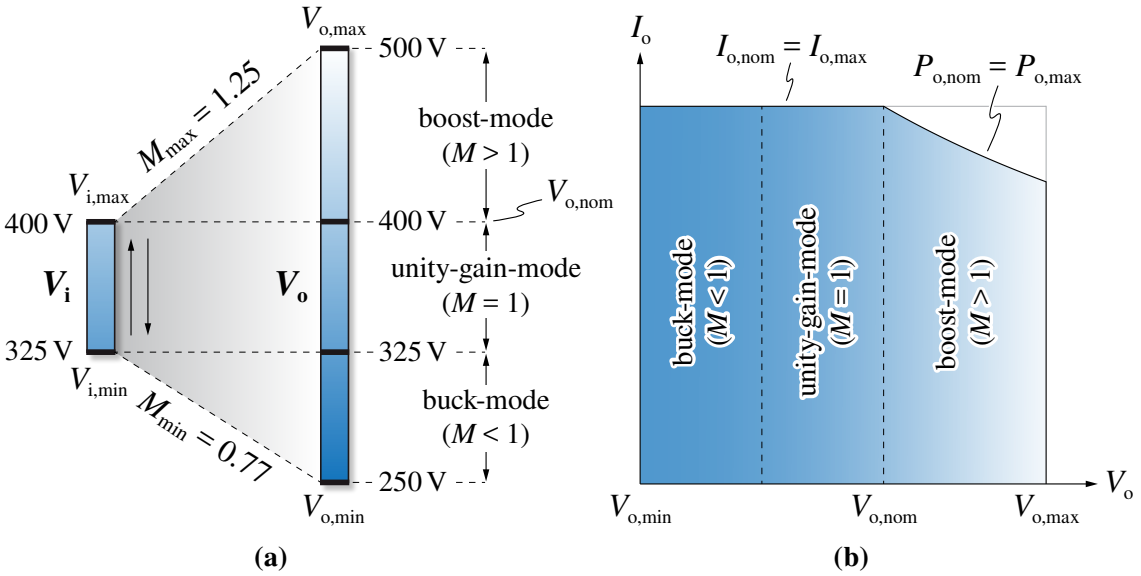


Fig. 6.5: (a) input/output voltage gain M range and **(b)** operating region in the (V_o, I_o) plane of the considered LLC converter, assuming $n = 1$. The input voltage V_i is adjusted by the AC/DC stage according the output voltage V_o, in order to maximize the unity-gain-mode operating region.

⑤ Inductance ratio λ calculation. This value is found by enforcing the Q_{min} curve to pass through the point $(f_{sw,max}, M_{min})$ in the (f_{sw}, M) plane, inverting (5.14):

$$\lambda = \frac{f_{sw,max}^2}{f_r^2 - f_{sw,max}^2} \left[1 - \sqrt{\frac{1}{M_{min}^2} - Q_{min}^2 \left(\frac{f_{sw,max}^2 - f_r^2}{f_r f_{sw,max}} \right)^2} \right]. \tag{6.2}$$

Higher values of λ with respect to (6.2) provide an operational margin in terms of quality factor, however they lead to a lower L_m and thus higher circulating current.

⑥ Characteristic impedance Z_r calculation. Since in the present case boost-mode operation only takes place within the power-limited region (cf. **Fig. 6.5(b)**), the worst-case condition for achieving complete ZVS of the primary-side transistors is found according to [130], by setting the tangency in the (M, Q) plane between the converter maximum power envelope and the inductive/capacitive region boundary curve. Taking into account a predefined p.u. margin x for achieving ZVS, the characteristic impedance expression is derived as [130]

$$Z_r = (1 - x) \frac{8}{\pi^2} \frac{V_{i,max}^2}{P_{o,nom}} \left[\lambda + \sqrt{\lambda (1 + \lambda)} \right]. \tag{6.3}$$

Lower values of Z_r provide an increased ZVS margin, however they lead to reduced L_r and L_m, increasing the circulating current, and to an increased C_r. The calculated Z_r is reiterated into ④, until a stable solution is obtained.

⑦ Maximum magnetizing inductance L_m verification. The current switched by the primary-side transistors (i.e., I_sw) must be high enough to ensure that the ZVS transitions are completed within the available dead time (cf. **Section 5.2.4**). The worst-case condition (i.e., the minimum value of I_sw) is found at the maximum switching frequency $f_\mathrm{sw,max}$ and at zero load (i.e., $Q = 0$), when only the transformer magnetizing current I_m is switched. As the peak value of the magnetizing current is proportional to the output voltage V_o, $V_\mathrm{o} = V_\mathrm{o,min}$ is considered to achieve ZVS also during transients. Therefore, being $Q_\mathrm{oss}(V_\mathrm{i})$ the total charge stored in the non-linear output capacitance C_oss of a transistor at V_i (cf. **Section 5.2.4**), the magnetizing inductance must fulfill

$$L_\mathrm{m} \leq \frac{n V_\mathrm{o,min} t_\mathrm{dt}}{8 Q_\mathrm{oss}(V_\mathrm{i,min}) f_\mathrm{sw,max}} = L_\mathrm{m,max}, \tag{6.4}$$

where t_dt is the switching dead time. In the present case, to limit the recirculating time of the primary MOSFET body diodes, a dead time equal to 10 % of the minimum switching period (i.e., $t_\mathrm{dt} = 400\,\mathrm{ns}$), is selected. Since Infineon IPW65R019C7 MOSFETs are employed as primary-side switches (cf. **Section 6.3.1**), the output capacitance charge is equal to $Q_\mathrm{oss}(V_\mathrm{i,min}) \approx 1.3\,\mu\mathrm{C}$, resulting in $L_\mathrm{m,max} \approx 38.4\,\mu\mathrm{H}$. If this limit is encountered, the iterative procedure is stopped and the resonant tank parameters are calculated according to

$$L_\mathrm{m} = L_\mathrm{m,max}, \quad L_\mathrm{r} = \lambda L_\mathrm{m}, \quad C_\mathrm{r} = \frac{1}{(2\pi f_\mathrm{r})^2 L_\mathrm{r}}, \tag{6.5}$$

leading to a suboptimal design.

⑧ Minimum operating frequency $f_\mathrm{op,min}$ calculation and verification. This value is calculated by numerical means, knowing λ, Z_r, $M = M_\mathrm{max}$ and $Q = Q(V_\mathrm{o,max}, P_\mathrm{o,nom})$, and inverting equation (5.14). If $f_\mathrm{op,min} > f_\mathrm{sw,min}$, then the procedure is repeated, restarting from step ③ with a progressively lower f_r value. Otherwise, the iterative design procedure is stopped and the last step is entered.

⑨ Resonant tank parameters L_r, C_r, L_m calculation:

$$L_\mathrm{r} = \frac{Z_\mathrm{r}}{2\pi f_\mathrm{r}}, \quad C_\mathrm{r} = \frac{1}{2\pi f_\mathrm{r} Z_\mathrm{r}}, \quad L_\mathrm{m} = \frac{1}{\lambda}\frac{Z_\mathrm{r}}{2\pi f_\mathrm{r}}. \tag{6.6}$$

It is worth noting that the aforementioned design steps lead to the minimization of the conduction losses of the semiconductor devices and the winding losses of the magnetic components. In fact, the proposed design procedure minimizes the transformer magnetizing current I_m, which doesn't contribute to the power transfer, and narrows the boost-mode operating region, avoiding large recirculation times. The peak value of the magnetizing

current can be expressed as

$$I_m = \frac{n V_o}{4 f_x L_m} \tag{6.7}$$

where $f_x = f_{sw}$ in buck-mode, $f_x = f_{sw} = f_r$ in unity-gain-mode and $f_x \approx f_r$ in boost-mode (i.e., assuming that the magnetizing current remains approximately constant during the circulating period, cf. **Section 5.2.3**). By substituting (6.3) into (6.6), then (6.6) into (6.7),

$$I_m \propto \frac{\lambda}{\lambda + \sqrt{\lambda\,(1+\lambda)}} \tag{6.8}$$

is obtained, which is monotonically increasing with λ. Therefore, since the required value of λ decreases by lowering f_r according to (6.2) (i.e., the further is f_r from $f_{sw,max}$, the flatter the Q curves can be), it is clear that the lowest I_m is obtained when the converter operating region fits the complete switching frequency range selected in step ①. Moreover, decreasing f_r also minimizes the frequency width of the boost-mode region, leading to an overall conduction loss optimal design. These considerations are verified in **Fig. 6.6**, which shows the RMS value of the resonant tank current (i.e., obtained with TDA) according to three different designs increasingly exploiting the available switching frequency range.

With the input specifications of **Table 6.1** and considering a ZVS load margin of $x = 5\,\%$, the proposed design procedure results in $L_r = 9.0\,\mu H$, $C_r = 141.8\,nF$ and $L_m = 26.5\,\mu H$, being $f_r = 140.6\,kHz$, $\lambda = 0.34$ and $Z_r = 8.0\,\Omega$. The selected margin assumes that the capacitor value may vary in a $\pm 5\,\%$ window, i.e. due to manufacturing tolerances, and the resonant/magnetizing inductance values can be tuned to keep the desired f_r, thus varying Z_r and the worst-case Q for ZVS by $\pm 5\,\%$. The operating region of the designed LLC converter is illustrated in **Fig. 6.7**.

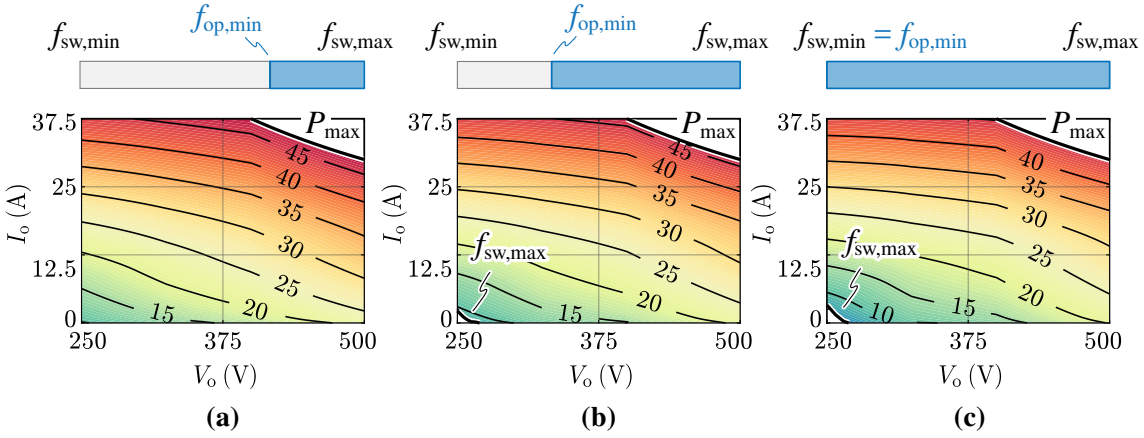


Fig. 6.6: RMS value of the resonant tank current (i.e., obtained with TDA) over the complete converter operating range in three different design conditions: **(a)** $f_{op,min} = 200\,kHz$, **(b)** $f_{op,min} = 150\,kHz$ and **(c)** $f_{op,min} = f_{sw,min} = 100\,kHz$. The minimum current stress is obtained when the full switching frequency range is exploited.

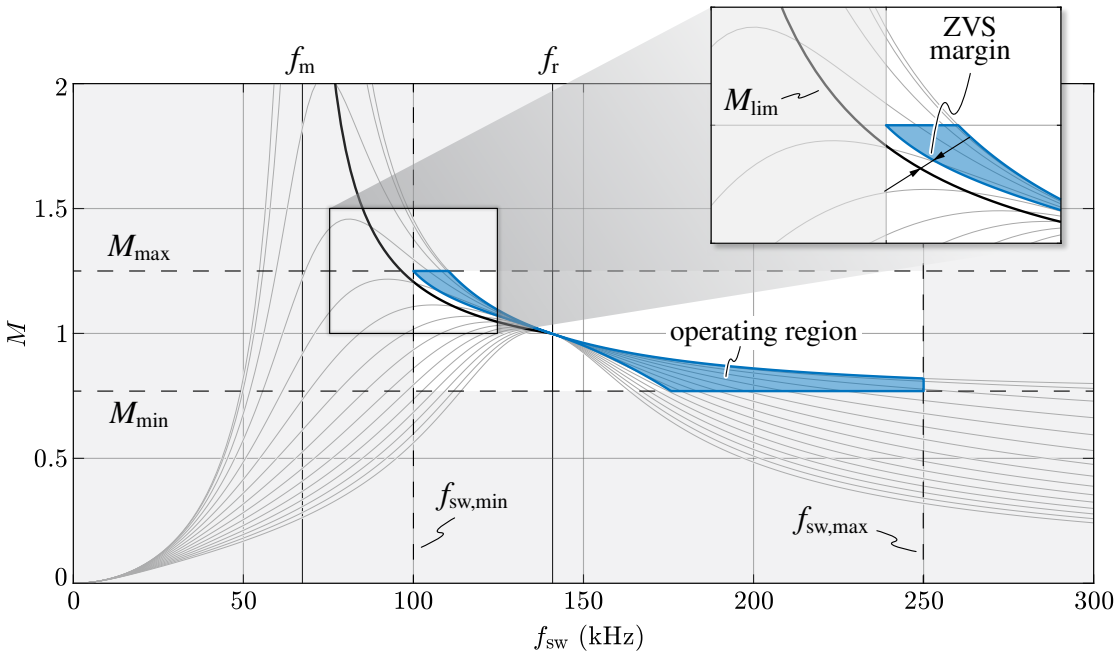


Fig. 6.7: Operating region of the designed LLC converter, with highlight of the selected ZVS margin in boost-mode operation.

6.3 Component Design/Selection

In this section, the main converter active and passive components are designed or selected, either exploiting the stresses derived in **Section 5.3** (i.e., denormalizing the TDA results with the actual converter parameters) or as the outcome of an optimization procedure. Moreover, the adopted models for the estimation of the component losses and the converter efficiency are described.

It is worth noting that, due to the manufacturing tolerances affecting the resonant tank components, the final values of C_r, L_r and L_m are slightly different (i.e., within a $\pm 5\,\%$ range) with respect to the optimal values obtained in **Section 6.2**. The stresses calculated in the following consider the final component values of the LLC converter prototype (cf. **Table 6.2**).

6.3.1 Semiconductor Devices

Since the considered design targets a full-Si converter realization (cf. **Chapter 1**), the best performing commercially available 600/650 V Si MOSFETs and diodes (i.e., in a discrete package) are selected. In particular, the primary-side switches operate in ZVS conditions and should feature minimum on-state resistance $R_{ds,on}$ (i.e., to minimize conduction losses) and large-enough output capacitance C_{oss} to perform the snubbering action at turn-off

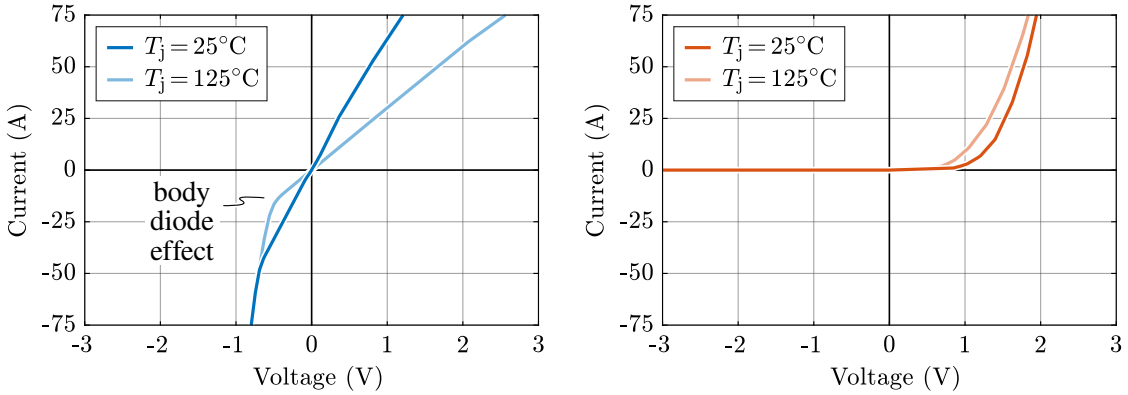


Fig. 6.8: Conduction characteristics of **(a)** Infineon IPW65R019C7 650 V Si Superjunction MOSFET and **(b)** Vishay VS-EPH6007L-N3 650 V Si Hyperfast diode, for $T_j = 25\,°C$ and $T_j = 125\,°C$.

(i.e., to minimize switching losses). Si Superjunction MOSFETs are perfect candidates for this application, therefore Infineon IPW65R019C7 MOSFETs (650 V, 19 mΩ) are selected for the full-bridge inverter. On the other hand, the output rectifier diodes cannot be only optimized for conduction performance, as the turn-off $\mathrm{d}i/\mathrm{d}t$ values are in the range of 10^1 A/µs in boost-mode and unity-gain-mode and can reach 10^2 A/µs in buck-mode. Therefore, Vishay VS-EPH6007L-N3 Hyperfast diodes (650 V, 60 A) are selected for the output diode bridge.

As explained in **Section 5.3.1**, the most accurate way to estimate the average conduction losses of each semiconductor device is by directly exploiting its conduction characteristics $v(i, T_j)$ provided in the manufacturer datasheet, the instantaneous current i flowing through it, and the instantaneous semiconductor junction temperature T_j, as

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v(i, T_j)\, i \, \mathrm{d}t. \tag{6.9}$$

where $T_{sw} = 1/f_{sw}$. The conduction characteristics of the selected MOSFET and diode are illustrated in **Fig. 6.8(a)** and **(b)**, respectively, for both $T_j = 25\,°C$ and $T_j = 125\,°C$. The instantaneous value of T_j required to calculate P_{cond} can be obtained exploiting a combined iterative electro-thermal model (i.e., taking into account both conduction and switching losses) based on the thermal specifications reported in **Section 6.3.7**. The estimated conduction losses in worst-case conditions (i.e., $T_j = 125\,°C$) of each primary-side transistor and each secondary-side diode (i.e., considering the LLC circuit structure in **Fig. 6.1**) are illustrated in **Fig. 6.9(a)** and **(b)**, respectively.

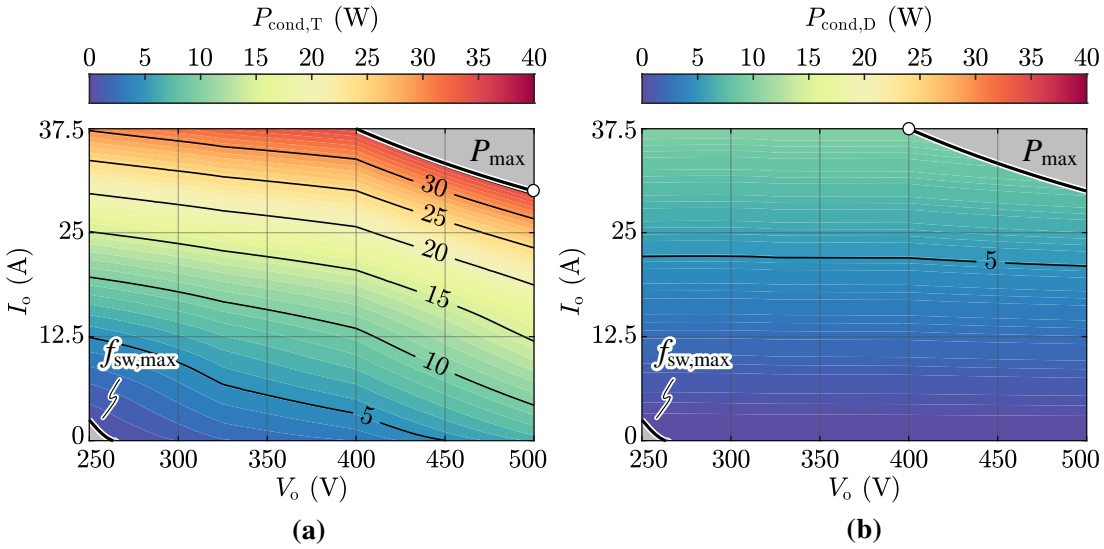


Fig. 6.9: Estimated conduction loss in worst-case conditions (i.e., $T_j = 125\,°C$) for each **(a)** primary-side transistor $P_{cond,T}$ and **(b)** secondary-side diode $P_{cond,D}$ assuming the LLC circuit structure in **Fig. 6.1** (i.e., four MOSFETs, eight diodes) and the parameters in **Table 6.2**. The worst-case operating point is indicated (○).

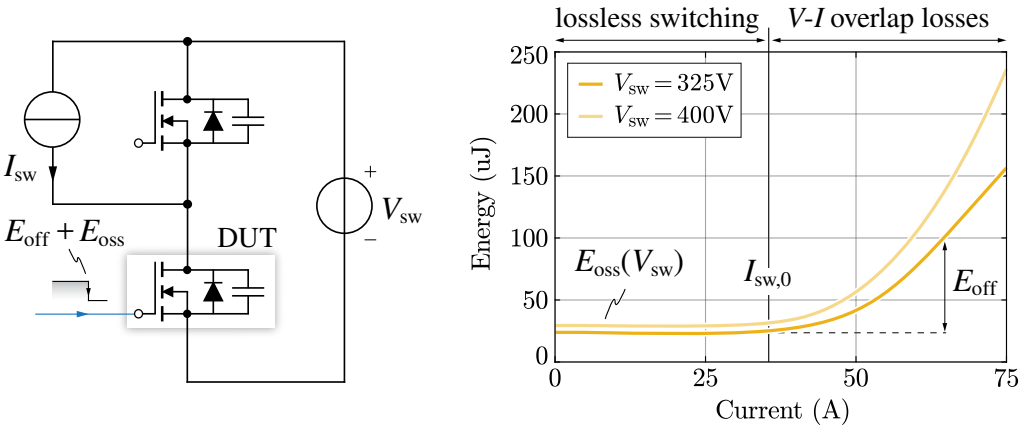
As described in **Chapter 5**, all semiconductor devices (i.e., transistors and diodes) successfully achieve soft-switching when the LLC converter is properly designed and operates within the inductive region. Nonetheless, both transistors and diodes can generate a certain amount of switching losses (cf. **Section 5.2.4**). Whereas the turn-off losses of the primary-side MOSFETs must be carefully evaluated at high current values (i.e., as the output capacitance may not provide sufficient snubbering action), the reverse-recovery of the output rectifier diodes can typically be neglected in a first approximation due to the relatively low turn-off $^{di}/_{dt}$ values determined by the resonant tank (i.e., hyperfast diodes are employed).

The switching losses of one transistor operating in ZVS are completely determined by the turn-off energy E_{off} as

$$P_{sw,T} \approx f_{sw}\, E_{off}(I_{sw}, V_{sw}). \tag{6.10}$$

It is worth noting that E_{off} must not include the energy stored in the output capacitance E_{oss}, which is not lost under ZVS operation and is recycled at the following switching transition (cf. **Section 5.3.1**).

The total energy involved at turn-off (i.e., $E_{off} + E_{oss}$) is obtained as function of the switched current I_{sw} and the switched voltage V_{sw} with a set of circuit simulations in Spice environment (cf. **Fig. 6.10(a)**), exploiting the equivalent circuit model of the Infineon IPW65R019C7 MOSFET provided by the semiconductor device manufacturer (i.e., with a $0\,\Omega$ turn-off gate resistance). The results are shown in **Fig. 6.10(b)** for $V_{sw} = 325\,V$ and $V_{sw} = 400\,V$. In particular, it is observed that the turn-off losses are ideally eliminated

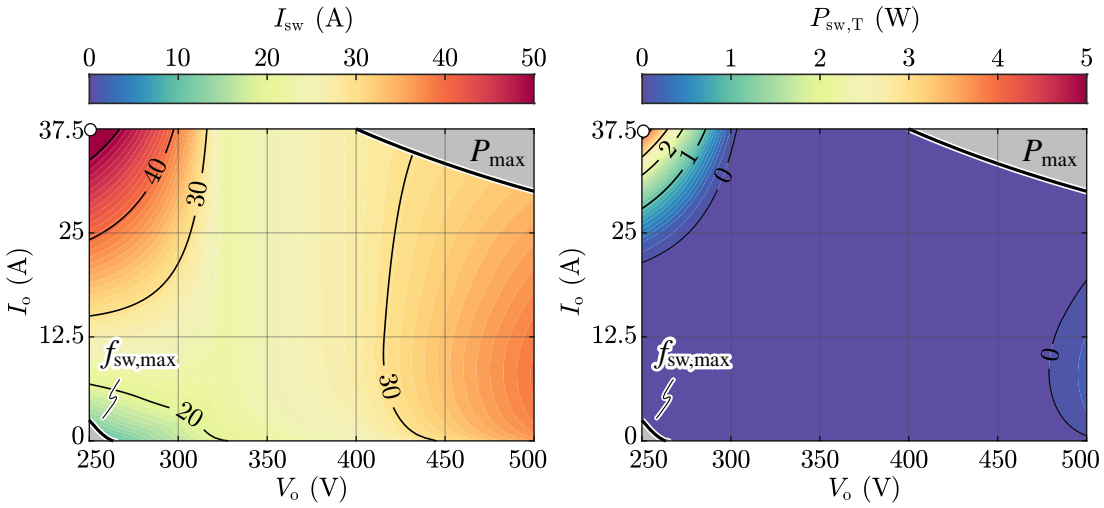


(a) **(b)**

Fig. 6.10: **(a)** equivalent circuit schematic of the simulation implemented in Spice for the switching loss extraction and **(b)** turn-off switching energy results for $V_{sw} = 325\,V$ and $V_{sw} = 400\,V$, including the energy stored in the output capacitance E_{oss}.

for $I_{sw} < I_{sw,0} \approx 35\,A$, whereas E_{off} rapidly increases for $I_{sw} > I_{sw,0}$, since a simultaneous overlap between the transistor drain-source voltage and channel current starts to appear [161]. The switched current I_{sw} obtained with TDA and the estimated switching losses of each primary-side transistor are illustrated in **Fig. 6.11(a)** and **(b)**, respectively.

The total primary-side and secondary-side semiconductor losses are of particular interest for the sizing of the heat dissipation system (cf. **Section 6.3.7**). Considering the worst-case operating condition (i.e., $T_j = 125\,°C$), the maximum total loss generated by the primary-side transistors is $\sum P_{semi,T} \approx 143\,W$, whereas the maximum diode losses are $\sum P_{semi,D} \approx 79\,W$.



(a) **(b)**

Fig. 6.11: **(a)** estimated transistor switched current I_{sw} obtained with TDA and **(b)** calculated transistor switching losses $P_{sw,T}$ assuming the parameters in **Table 6.2**. The worst-case operating point is indicated (○).

6.3.2 Resonant Capacitor

The resonant capacitor must be able to withstand the peak voltage (i.e., which may cause the breakdown of the capacitor itself) and the total RMS current stress (i.e., related to losses and temperature rise) meanwhile satisfying the required capacitance value $C_\mathrm{r} \pm 5\,\%$.

The peak capacitor voltage stress is illustrated in **Fig. 6.12(a)** as function of the output voltage V_o and output current I_o. A maximum capacitor voltage $V_{\mathrm{C_r,max}} \approx 625\,\mathrm{V}$ is obtained for $V_\mathrm{o} = 500\,\mathrm{V}$ and $I_\mathrm{o} = 30\,\mathrm{A}$ (i.e., at $P_\mathrm{o} = P_\mathrm{o,max}$). The RMS current stress is reported in the $(V_\mathrm{o}, I_\mathrm{o})$ plane in **Fig. 6.12(b)**. The worst-case value is identified as $I_{\mathrm{C_r,RMS,max}} \approx 46.4\,\mathrm{A}$, also obtained for $V_\mathrm{o} = 500\,\mathrm{V}$ and $I_\mathrm{o} = 30\,\mathrm{A}$.

Due to the high-frequency, high-voltage, high-current requirements, ceramic capacitors are employed. In particular, because of the necessarily strict C_r tolerance, C0G technology is considered (i.e., featuring low sensitivity with respect to voltage bias and temperature). The CAA572 1 kV resonant capacitor series from TDK is selected and two sets of 14 paralleled 20 nF devices are connected in series to split the RMS current stress among 28 capacitor units. Due to manufacturing tolerances, the realized resonant capacitor features $C_\mathrm{r} = 147.0\,\mathrm{nF}$, which is $\approx 4\,\%$ higher than the desired value.

To evaluate the impact of the resonant capacitor on the converter efficiency, the losses induced by the RMS current stress can be estimated as

$$P_{\mathrm{C_r}} \approx R_{\mathrm{C_r}} I^2_{\mathrm{C_r,RMS}}, \tag{6.11}$$

where $R_{\mathrm{C_r}}$ is the equivalent series resistance of the resonant capacitor at the considered switching frequency.

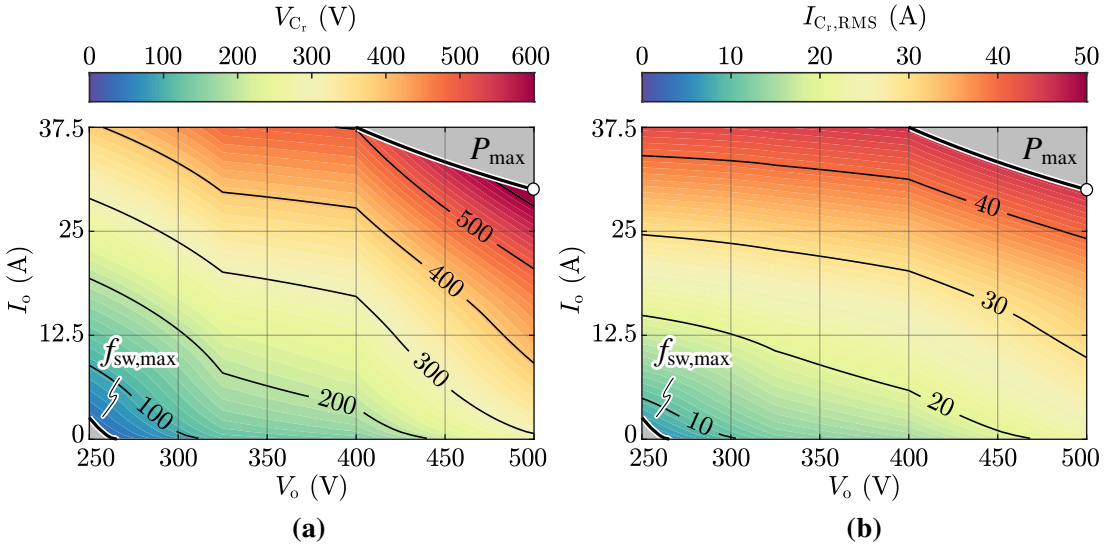


Fig. 6.12: Estimated resonant capacitor **(a)** peak voltage $V_{\mathrm{C_r}}$ and **(b)** RMS current $I_{\mathrm{C_r,RMS}}$ obtained with TDA, assuming the parameters in **Table 6.2**. The worst-case operating point is indicated (○).

6.3.3 Resonant Inductor

Due to the resonant capacitor tolerance, the design value of the resonant inductance is adjusted to maintain the specified resonance frequency, i.e. $L_r = 1/(4\pi^2 f_r^2 C_r) = 8.7\,\mu H$.

The resonant inductor must be able to withstand the total resonant tank RMS current stress (i.e., related to the winding losses) and the peak-to-peak flux ripple (i.e., related to the core losses), which both affect the temperature rise of the component. In view of the high power rating of the converter, the resonant inductor is split into four units connected as in **Fig. 6.1**. Each unit must achieve the original inductance value L_r, however it is subject to half of the resonant tank current and thus half of the peak-to-peak flux ripple.

The RMS current stress applied to each resonant inductor is shown in **Fig. 6.13(a)** as function of the output voltage V_o and output current I_o. The worst-case value is identified as $I_{L_r,RMS,max} \approx 23.2\,A$, obtained for $V_o = 500\,V$ and $I_o = 30\,A$ (i.e., at $P_o = P_{o,max}$). The peak-to-peak inductor flux ripple is obtained as $\Delta\Psi_{L_r,pp} = 2 L_r I_{L_r}$ (i.e., where I_{L_r} is the peak inductor current) and is illustrated in **Fig. 6.13(b)**. The maximum value $\Delta\Psi_{L_r,pp,max} \approx 0.60\,mV\,s$ is also obtained for $V_o = 500\,V$ and $I_o = 30\,A$.

It is worth noting that the leakage inductance of the isolation transformer is effectively in series with L_r, therefore it must be subtracted to the design value of the resonant inductance. For this reason, the transformer must be designed before the resonant inductor (cf. **Section 6.3.4**). In the present case, the transformer design leads to an equivalent primary-referred leakage inductance $\approx 1\,\mu H$, therefore the target design value of L_r is reduced to $7.7\,\mu H$.

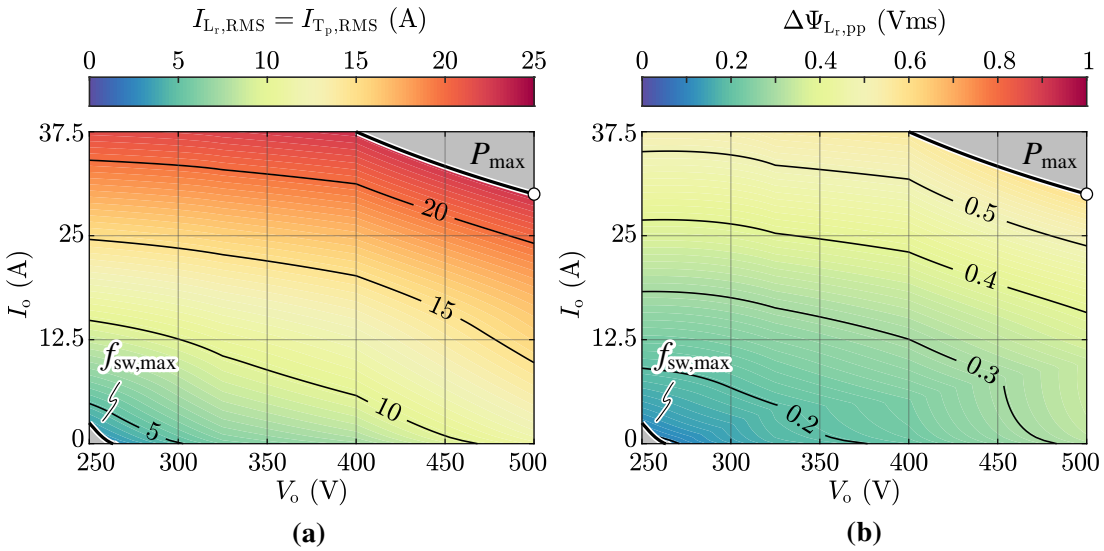


Fig. 6.13: Estimated resonant inductor **(a)** RMS current $I_{L_r,RMS}$ and **(b)** peak-to-peak flux ripple $\Delta\Psi_{L_r,pp}$ obtained with TDA, assuming the LLC circuit structure in **Fig. 6.1** (i.e., four series/parallel inductors) and the parameters in **Table 6.2**. The worst-case operating point is indicated (○). The same RMS current stress applies for the primary-side of each transformer $I_{T_p,RMS} = I_{L_r,RMS}$.

The adopted inductor optimization routine is illustrated in **Fig. 6.14** and aims to achieve the target inductance value $L_r = 7.7\,\mu H$ and simultaneously identify the optimal winding arrangement (i.e., number of turns N, number of litz strands per turn, strand diameter, etc.) for a selected core geometry and material, taking into account several

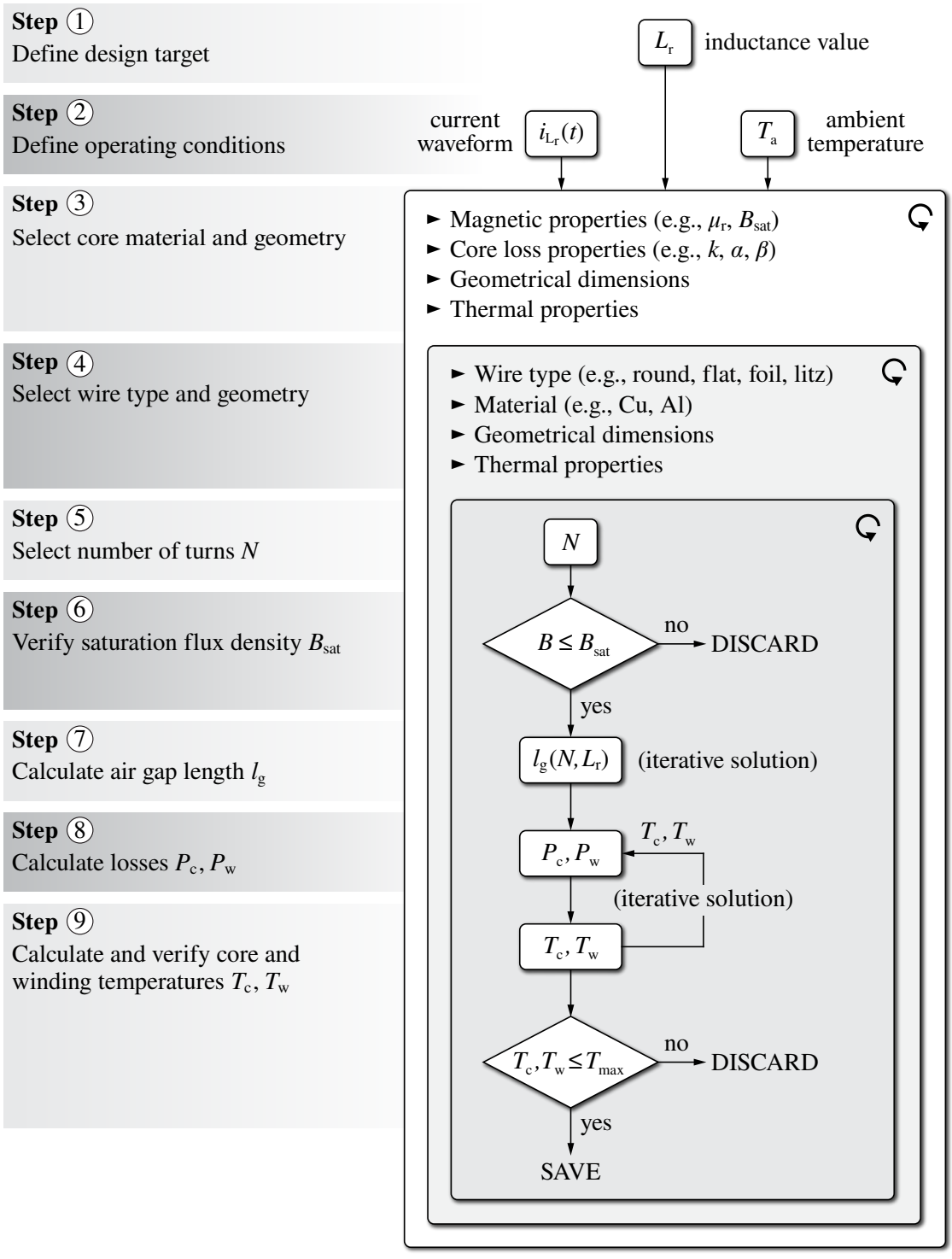


Fig. 6.14: Flowchart of the adopted resonant inductor design/optimization routine.

design constraints (e.g., core saturation flux density, maximum core/winding temperatures, etc.). The adopted reluctance, loss and thermal models, based on [21, 61, 91, 92], are described in **Section 3.2.3**. The inputs of the optimization routine are the inductor nominal operating conditions (i.e., derived with TDA at $V_i = V_o = 400\,\text{V}$, $I_o = 37.5\,\text{A}$), the complete ferrite core database from EPCOS-TDK (i.e., for the core geometry and material selection) and a customized litz wire database (i.e., for the winding design). A large number of designs is assessed by sweeping the value of N for each combination of core geometry/material and litz wire type, calculating the required air gap length to achieve the desired value of L_r, and filtering the results according to the following constraints:

- maximum core flux density: $B \leq B_{sat}$;
- maximum core/winding temperatures: T_c, $T_w \leq 100\,^\circ\text{C}$;

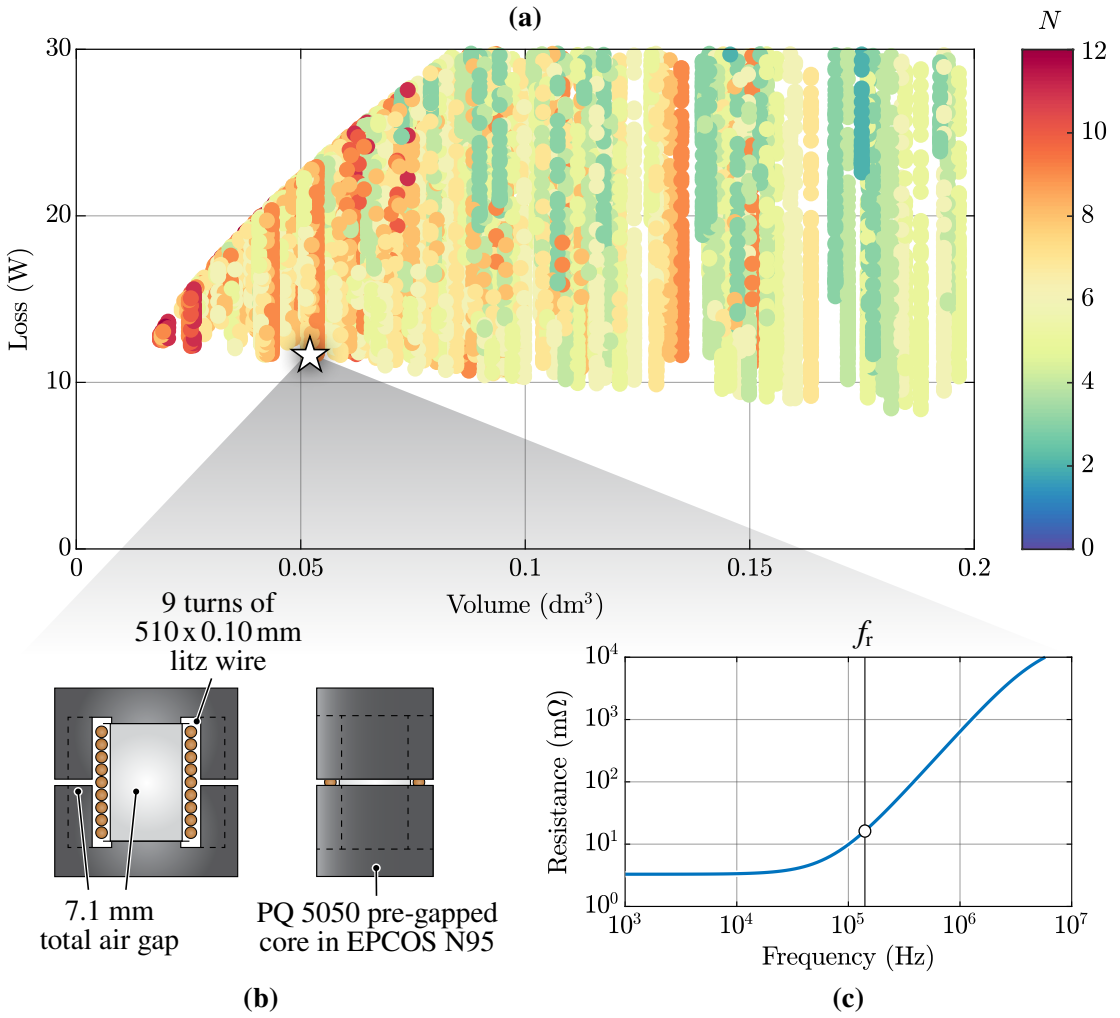


Fig. 6.15: **(a)** loss-volume performance space resulting from the adopted resonant inductor optimization procedure and **(b)–(c)** highlight of the selected design and its winding resistance value as function of frequency.

where B_{sat} is the saturation flux density of the selected core material, T_c is the core temperature and T_w is the winding temperature. The results of the optimization procedure are shown in **Fig. 6.15(a)**, where the feasible resonant inductor designs are reported in the loss-volume performance space. The final design is selected according to geometrical size considerations (i.e., to fit the magnetic components in front of the semiconductor heatsink) and is schematically illustrated in **Fig. 6.15(b)**. Additionally, **Fig. 6.15(c)** shows the estimated inductor winding resistance as function of frequency.

6.3.4 Transformer

Due to the tolerance on C_r and the related L_r adjustment, the value of the transformer magnetizing inductance L_m is modified to obtain the desired λ value as $L_m = L_r/\lambda = 25.3\,\mu H$.

The isolation transformer must be able to withstand the primary-side and secondary-side RMS current stresses (i.e., related to the winding losses) and the peak-to-peak flux ripple (i.e., related to the core losses). Also in this case, in view of the high power rating of the converter, the transformer is split in four units connected as in **Fig. 6.1**. Each unit features a $n:1$ turns ratio and must ensure the original magnetizing inductance value L_m, however it is subject to half of the current stress and half of the peak-to-peak flux ripple.

The RMS current stress applied to the primary winding of each transformer unit is the same as for the resonant inductor (cf. **Fig. 6.13(a)**), resulting in a worst-case

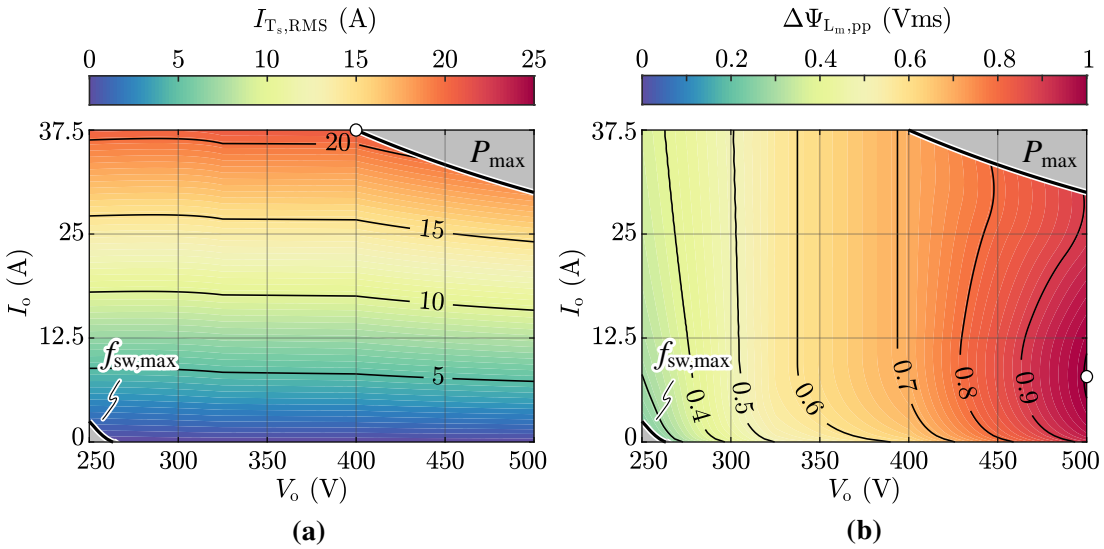


Fig. 6.16: Estimated transformer **(a)** secondary-side RMS current $I_{T_s,RMS}$ and **(b)** peak-to-peak flux ripple $\Delta\Psi_{L_m,pp}$ obtained with TDA, assuming the LLC circuit structure in **Fig. 6.1** (i.e., four series/parallel transformers) and the parameters in **Table 6.2**. The worst-case operating point is indicated (○).

value $I_{\mathrm{T_p,RMS,max}} \approx 23.2\,\mathrm{A}$. The secondary winding of the transformer is subject to a lower current stress (cf. **Fig. 6.16(a)**), since the secondary-side current is free from the magnetizing component. The worst-case stress $I_{\mathrm{T_s,RMS,max}} \approx 20.9\,\mathrm{A}$ is found in nominal conditions (i.e.,$V_\mathrm{o} = 400\,\mathrm{V}$, $I_\mathrm{o} = 37.5\,\mathrm{A}$). The transformer peak-to-peak flux ripple is illustrated in **Fig. 6.16(b)** as function of V_o and I_o. It is observed that the maximum value $\Delta\Psi_{\mathrm{L_m,pp,max}} \approx 1.01\,\mathrm{mV\,s}$ is obtained for $V_\mathrm{o} = 500\,\mathrm{V}$ and $I_\mathrm{o} \approx 8\,\mathrm{A}$.

Although an ideal transformer with turns ratio n and primary-referred magnetizing inductance L_m has been considered up to know, the primary and secondary transformer windings also feature a parasitic inductance component, which represents the leakage flux. In fact, a real transformer can be represented with the physical model illustrated in **Fig. 6.17(a)**, where $L_{\sigma,\mathrm{p}}$, $L_{\sigma,\mathrm{s}}$ are the primary and secondary winding leakage inductance components, respectively, L_μ is the transformer magnetizing inductance and t is the physical turns ratio. This model can be transformed in the all-primary-referred equivalent circuit shown in **Fig. 6.17(b)** by means of basic circuit theory [128], obtaining the following one-to-one relations with the physical quantities:

$$\begin{cases} L_\mathrm{s} = L_{\sigma,\mathrm{p}} + L_\mu \parallel t^2 L_{\sigma,\mathrm{s}} \overset{L_\mu \gg t^2 L_{\sigma,\mathrm{s}}}{\approx} L_{\sigma,\mathrm{p}} + t^2 L_{\sigma,\mathrm{s}} \\ L_\mathrm{m} = L_\mu - L_\mu \parallel t^2 L_{\sigma,\mathrm{s}} \overset{L_\mu \gg t^2 L_{\sigma,\mathrm{s}}}{\approx} L_\mu \\ n = \dfrac{t}{\sqrt{1 + L_\mathrm{s}/L_\mathrm{m}}} \overset{L_\mathrm{m} \gg L_\mathrm{s}}{\approx} t \end{cases} . \tag{6.12}$$

With the assumption that the leakage inductance component is significantly smaller than the magnetizing one (i.e., $L_{\sigma,\mathrm{p}} \approx t^2 L_{\sigma,\mathrm{s}} \ll L_\mu$), straightforward relations are obtained. In particular, the equivalent stray inductance $L_\mathrm{s} \approx L_{\sigma,\mathrm{p}} + t^2 L_{\sigma,\mathrm{s}}$ ends up in series with L_r and must therefore be taken into account when designing the resonant inductor (cf. **Section 6.3.3**).

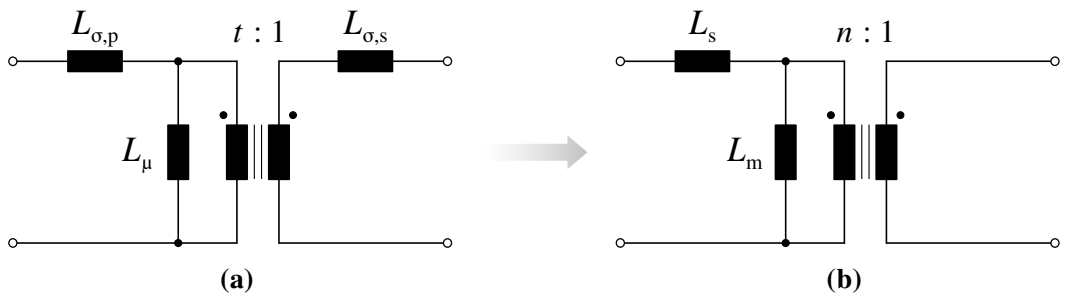


Fig. 6.17: Equivalent circuit of the transformer **(a)** physical model and **(b)** all-primary-referred model.

The adopted transformer optimization routine is similar to the one exploited for the design of the resonant inductor and is illustrated in **Fig. 6.18**. This procedure aims to achieve the specified turns ratio $n = 1$ and the target inductance value $L_m = 25.3\,\mu H$,

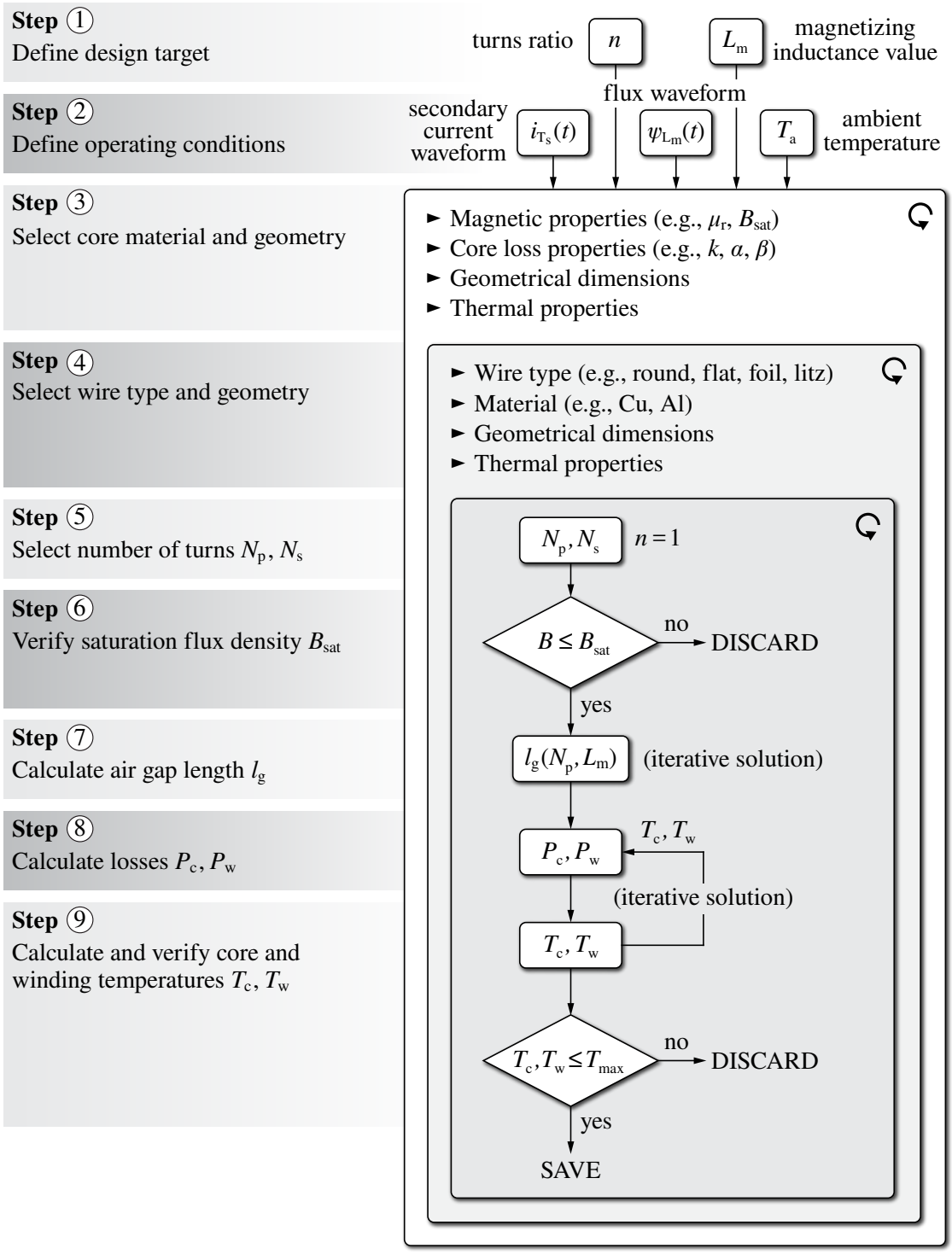


Fig. 6.18: Flowchart of the adopted transformer design/optimization routine.

meanwhile identifying the optimal winding arrangement for a selected core geometry and material, taking into account the same constraints as for the resonant inductor:

- maximum core flux density: $B \leq B_{\text{sat}}$;
- maximum core/winding temperatures: $T_{\text{c}}, T_{\text{w}} \leq 100\,^{\circ}\text{C}$.

The inputs of the optimization routine are the transformer nominal operating conditions (i.e., derived with TDA at $V_{\text{i}} = V_{\text{o}} = 400\,\text{V}$, $I_{\text{o}} = 37.5\,\text{A}$), the complete ferrite core database from EPCOS-TDK (i.e., for the core geometry and material selection) and a customized litz wire database (i.e., for the design of primary and secondary windings). A large number of designs is assessed by sweeping the value of the primary/secondary number of turns $N_{\text{p}} = N_{\text{s}}$ for each combination of core geometry/material and litz wire type, calculating the required air gap length to achieve the desired value of L_{m}, and filtering the results

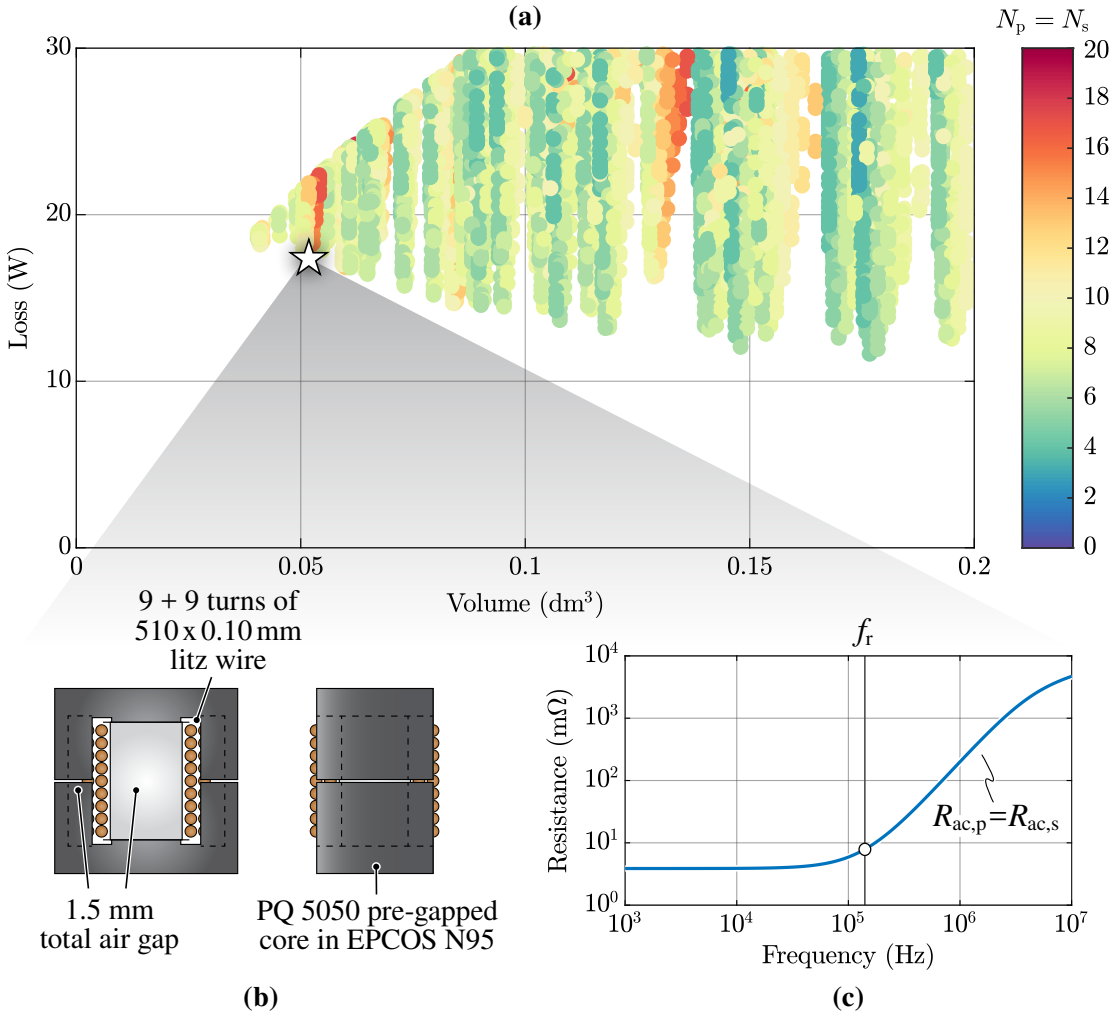


Fig. 6.19: **(a)** loss-volume performance space resulting from the adopted transformer optimization procedure and **(b)**–**(c)** highlight of the selected design and its primary/secondary winding resistance values as functions of frequency.

according to the mentioned constraints. The results of the optimization procedure are shown in **Fig. 6.19(a)**, where the feasible transformer designs are reported in the loss-volume performance space. The selected design is schematically illustrated in **Fig. 6.19(b)**, whereas **Fig. 6.19(c)** shows the estimated transformer primary and secondary winding resistance values as functions of frequency.

6.3.5 Input Filter Capacitor

The total input filter capacitance C_i required by the application is obtained as the value that satisfies both the RMS current and peak-to-peak voltage ripple constraints.

The RMS current stress is shown in **Fig. 6.20(a)** as function of V_o and I_o. The worst-case value is found for $V_\mathrm{o} = 250\,\mathrm{V}$ and $I_\mathrm{o} = 37.5\,\mathrm{A}$, resulting in $I_{\mathrm{C_i,RMS,max}} \approx 32.7\,\mathrm{A}$. The minimum capacitance value that ensures a predefined maximum peak-to-peak input voltage ripple $\Delta V_{\mathrm{i,pp,max}}$ can be calculated as $C_\mathrm{i} \geq \Delta Q_{\mathrm{C_i,pp,max}} / \Delta V_{\mathrm{i,pp,max}}$, where $\Delta Q_{\mathrm{C_i,pp,max}}$ is the worst-case peak-to-peak input charge ripple (cf. **Section 5.3.5**) within the considered operating range. The value of $\Delta Q_{\mathrm{i,pp}}$ is reported in the $(V_\mathrm{o}, I_\mathrm{o})$ plane in **Fig. 6.20(b)**, where the worst-case value $\Delta Q_{\mathrm{C_i,pp,max}} \approx 53.3\,\mathrm{V\,\mu F}$ is identified for $V_\mathrm{o} = 500\,\mathrm{V}$ and $I_\mathrm{o} \approx 10\,\mathrm{A}$. Therefore, assuming $\Delta V_{\mathrm{i,pp,max}} = 1\,\mathrm{V}$, the minimum required capacitance becomes $C_\mathrm{i} \geq 53.3\,\mu\mathrm{F}$. It is worth noting that the strict $\Delta V_{\mathrm{i,pp,max}}$ criterion is only related to the LLC converter operation (i.e., charge ripple at the switching frequency f_sw) and does not account for the low-frequency voltage oscillation generated by the AC/DC stage, which is limited by the rectifier electrolytic capacitors (cf. **Section 3.2.2**).

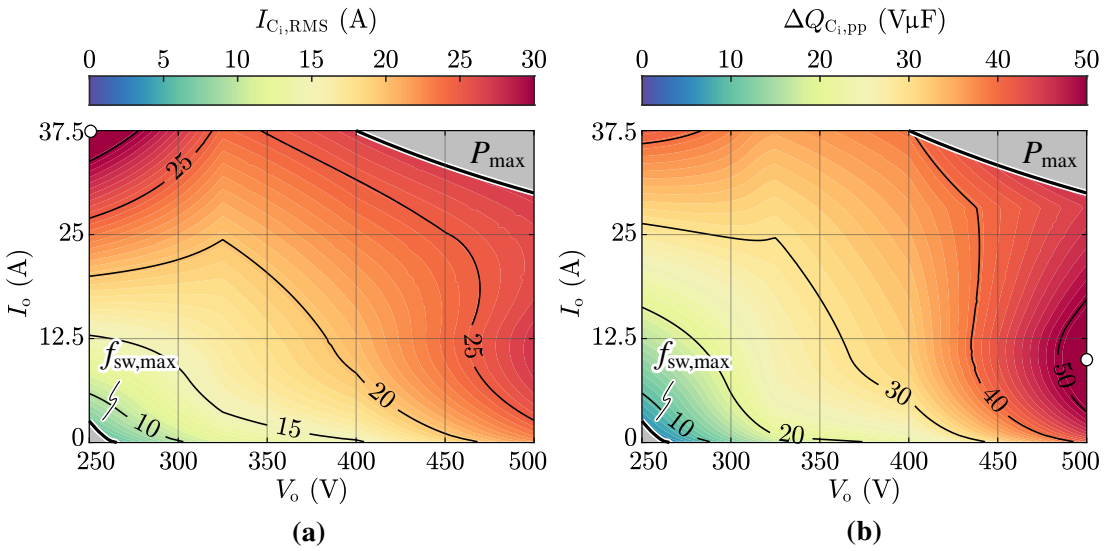


Fig. 6.20: Estimated input filter capacitor **(a)** RMS current $I_{\mathrm{C_i,RMS}}$ and **(b)** peak-to-peak charge ripple $\Delta Q_{\mathrm{C_i,pp}}$ obtained with TDA, assuming the parameters in **Table 6.2**. The worst-case operating point is indicated (○).

Due to the relatively low capacitance requirement and large RMS current stress, film capacitor technology is considered. In particular, two parallel 70 µF 600 V MKP1848C capacitors from Vishay-Roederstein are selected (i.e., for a total of 140 µF), capable of withstanding 40 A.

The losses generated by the input filter capacitor can be estimated as

$$P_{C_i} \approx R_{C_i} I^2_{C_i,RMS}, \tag{6.13}$$

where R_{C_i} is the equivalent series resistance of the input filter capacitor at the considered switching frequency.

6.3.6 Output Filter Capacitor

The sizing of the output filter capacitance C_o follows the same criteria outlined for C_i.

The RMS current stress is shown in **Fig. 6.21(a)** and the worst-case value is found for $V_o = 500\,V$ and $I_o = 30\,A$ (i.e., at $P_o = P_{o,max}$), resulting in $I_{C_o,RMS,max} \approx 22.3\,A$. The value of $\Delta Q_{C_o,pp}$ is reported in the (V_o, I_o) plane in **Fig. 6.21(b)**, where the worst-case value $\Delta Q_{C_o,pp,max} \approx 44.0\,V\,\mu F$ is also found for $V_o = 500\,V$ and $I_o = 30\,A$. Therefore, assuming $\Delta V_{o,pp,max} = 1\,V$, the minimum required capacitance becomes $C_o \geq 44.0\,\mu F$.

Also in this case, due to the relatively low capacitance requirement and large RMS current stress, the same capacitor model as for C_i is selected, connecting three units in parallel (i.e., for a total of 210 µF) to achieve enhanced battery current ripple filtering performance.

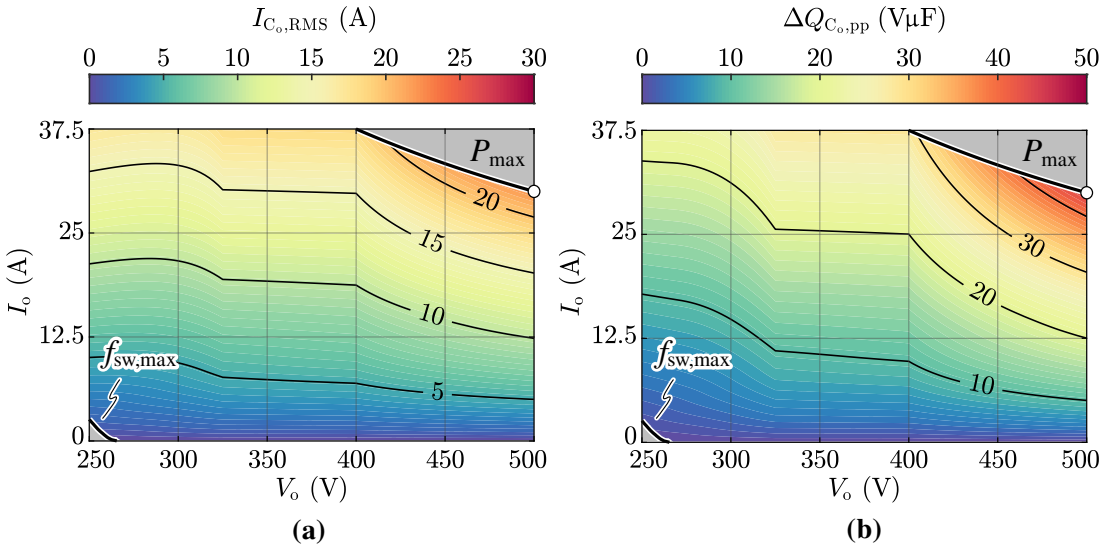


Fig. 6.21: Estimated output filter capacitor **(a)** RMS current $I_{C_o,RMS}$ and **(b)** peak-to-peak charge ripple $\Delta Q_{C_o,pp}$ obtained with TDA, assuming the parameters in **Table 6.2**. The worst-case operating point is indicated (○).

The losses generated by the output filter capacitor can be estimated as

$$P_{\mathrm{C_o}} \approx R_{\mathrm{C_o}} I^2_{\mathrm{C_o,RMS}}, \tag{6.14}$$

where $R_{\mathrm{C_o}}$ is the equivalent series resistance of the output filter capacitor at the considered switching frequency.

6.3.7 Heat Dissipation System

To dissipate the power losses, the discrete transistors and diodes are connected to two separate forced air cooled heatsinks by means of an electrically insulating, heat conducting thermal interface material (TIM). The thermal equivalent circuit of the adopted setup is illustrated in **Fig. 3.9(a)** (cf. **Chapter 3**), where the ambient temperature T_a, the semiconductor junction temperature T_j, the discrete device case temperature T_c and the heatsink temperature T_hs are indicated. As for the AC/DC converter, the aim of the heat dissipation system is to ensure that the semiconductor junction temperature of all devices complies with the maximum rating (i.e., $T_\mathrm{j,max} = 150\,^\circ\mathrm{C}$ in the present case). In particular, to account for modeling errors, a temperature margin of 25 °C is considered, thus targeting a maximum operating junction temperature of 125 °C.

Furthermore, the heatsink temperature T_hs is limited below $T_\mathrm{hs,max} = 70\,^\circ\mathrm{C}$, as its value mainly determines the ambient temperature inside the converter and affects the other components (e.g., PCB, auxiliaries, etc.). It is worth noting that the heatsink top surface is assumed to be isothermic (i.e., valid approximation for thick baseplates) and its temperature is determined by the losses of all semiconductor devices, as shown in **Fig. 3.9(b)** (cf. **Chapter 3**). Assuming a maximum ambient (i.e., air) temperature $T_\mathrm{a,max} = 40\,^\circ\mathrm{C}$ and two identical heatsinks (i.e., for simplicity of realization and converter layout), the maximum heatsink-to-ambient resistance is calculated as

$$R_\mathrm{th,hs\text{-}a} \leq \max\left[\frac{T_\mathrm{hs,max} - T_\mathrm{a,max}}{\sum P_\mathrm{T,max}}, \frac{T_\mathrm{hs,max} - T_\mathrm{a,max}}{\sum P_\mathrm{D,max}}\right] \approx 0.210\,^\circ\mathrm{C/W}, \tag{6.15}$$

where $\sum P_\mathrm{T,max} \approx 143\,\mathrm{W}$ and $\sum P_\mathrm{D,max} \approx 79\,\mathrm{W}$ represent the maximum primary-side transistor losses and the maximum secondary-side diode losses, respectively, assuming the worst-case operating conditions (i.e., $T_\mathrm{j} = 125\,^\circ\mathrm{C}$).

The case-to-heatsink thermal resistance $R_\mathrm{th,c\text{-}hs}$ is determined by the TIM layer and can be calculated as

$$R_\mathrm{th,c\text{-}hs} = \frac{r_\mathrm{th,TIM}}{A_\mathrm{TO\text{-}247}} \approx 0.675\,^\circ\mathrm{C/W}, \tag{6.16}$$

where $r_\mathrm{th,TIM} \approx 135\,\mathrm{mm^2\,^\circ C/W}$ is the specific thermal resistance of the selected TIM and $A_\mathrm{TO\text{-}247} \approx 200\,\mathrm{mm^2}$ is the TO-247 thermal interface area.

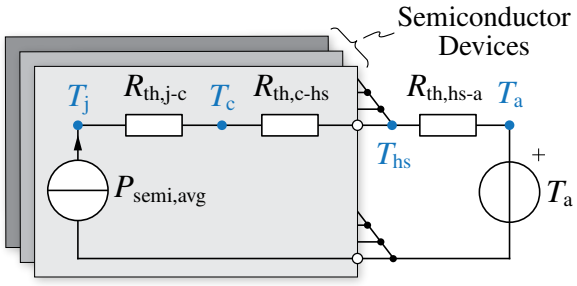


Fig. 6.22: Simplified thermal equivalent circuit of the adopted semiconductor loss dissipation setup, exploited to estimate the node temperatures.

Since the time constant of the junction-to-case thermal circuit is significantly larger than the switching period T_{sw}, the thermal impedance $Z_{th,j\text{-}c}$ in **Fig. 3.9(b)** can be simplified to a thermal resistance (i.e., $R_{th,j\text{-}c}$, provided in the manufacturer datasheet) and the average semiconductor losses can be directly exploited to estimate the semiconductor junction temperature, as illustrated in **Fig. 6.22**:

$$T_j = T_{hs} + P_{semi,avg}\left(R_{th,j\text{-}c} + R_{th,c\text{-}hs}\right). \tag{6.17}$$

Due to the temperature dependence of semiconductor losses, an iterative procedure is implemented and the worst-case junction temperature (i.e., assuming $T_{hs} = T_{hs,max}$) is calculated for all semiconductor devices, to check the compliance with the desired $T_{j,max}$ value. The results are illustrated in **Fig. 6.23**, showing that the worst-case peak value of T_j is below $T_{j,max}$ with a margin of $\approx 25\,°C$ for the primary-side MOSFETs and $\approx 40\,°C$ for

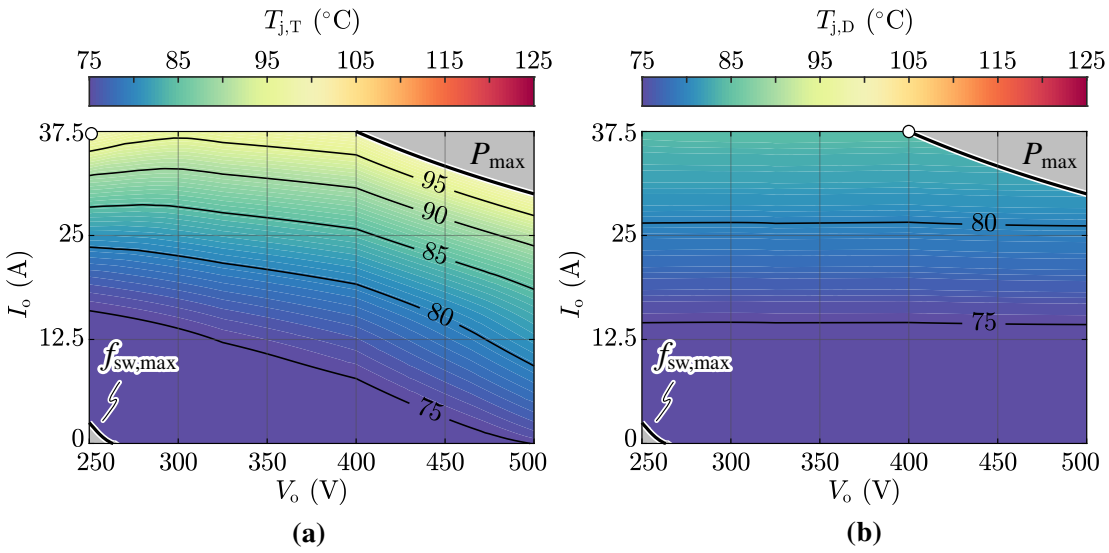


Fig. 6.23: Estimated worst-case operating junction temperature of **(a)** the primary-side transistors $T_{j,T}$ and **(b)** the secondary-side diodes $T_{j,D}$, assuming the LLC circuit structure in **Fig. 6.1** (i.e., four MOSFETs, eight diodes), the parameters in **Table 6.2** and $T_{hs} = T_{hs,max} = 70\,°C$. The worst-case operating point is indicated (○).

the secondary-side diodes (i.e., neglecting the switching losses related to reverse-recovery). Interestingly, the worst-case junction temperature for the primary-side transistors is found for $V_o = 250\,V$ and $I_o = 37.5\,A$, as the turn-off switching losses are no longer negligible with respect to conduction losses (cf. **Fig. 6.11(b)**).

Finally, the heatsink and the forced air cooling system (i.e., the fans) are sized to comply with (6.15). For reasons of simplicity, the same heatsink series as for the AC/DC stage has been adopted for the cooling of both the primary-side transistors and the secondary-side diodes (i.e., two independent heatsinks). The heat dissipation setup features a PA8-62 extruded aluminum heatsink from MeccAl with a 13.5 mm thick baseplate (i.e., for enhanced thermal spreading), a total height of 62 mm, a length of 100 mm, a width of 125 mm (i.e., to fit the four DC/DC units in 500 mm, equal to the AC/DC stage width) and two 2.9 W 60x25 mm fans from Orion Fans. This design yields a thermal resistance value $R_{th,hs\text{-}a} \approx 0.148\,^{\circ}C/W$ and ensures a 30 % margin with respect to (6.15).

6.4 Experimental Results

The constructed 15 kW LLC resonant converter protoype is illustrated in **Fig. 6.24**, featuring the parameters and component values reported in **Table 6.2**. It is worth noting that the primary-side and secondary-side boards are designed for two paralleled 15 kW LLC units, nonetheless the experimental tests are limited to a single converter unit.

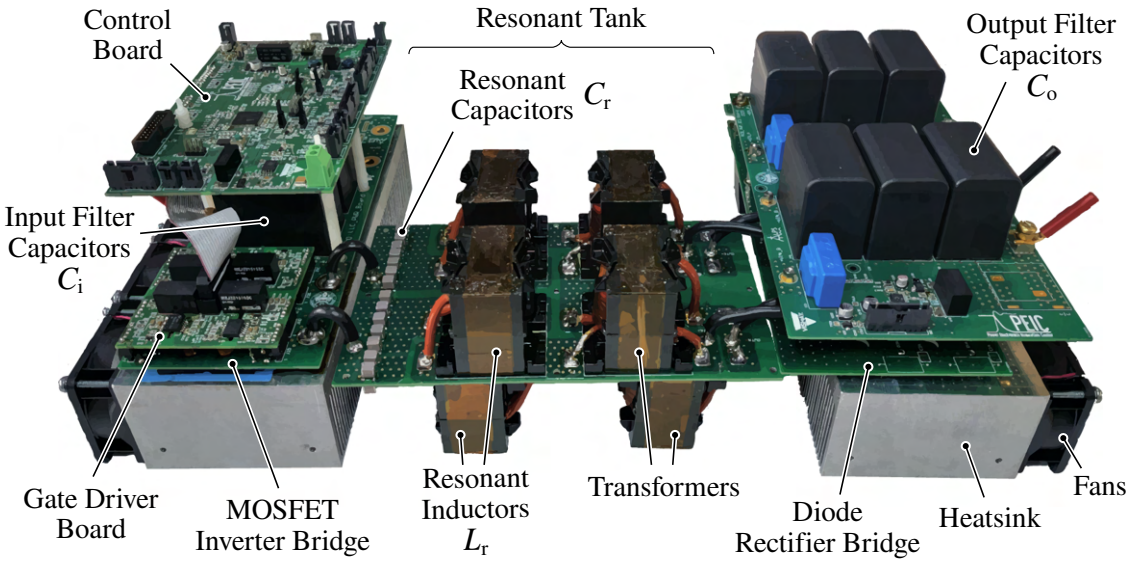


Fig. 6.24: Picture of the 15 kW LLC resonant converter prototype. Since the boards are designed for two paralleled 15 kW units, only half of the converter is utilized for testing.

Tab. 6.2: Parameters and component values of the realized LLC converter prototype.

Parameter	Description	Value
n	transformer turns ratio	1
L_r	resonant inductance	8.7 µH
C_r	resonant capacitance	147.0 nF
L_m	magnetizing inductance	25.3 µH
C_i	input filter capacitance	70 µF
C_o	output filter capacitance	210 µF
f_r	primary resonance frequency	140.6 kHz
f_m	secondary resonance frequency	71.2 kHz
λ	inductance ratio	0.34
Z_r	characteristic impedance	7.7 Ω

In this section, the converter steady-state operation and loss/efficiency performance are experimentally assessed with the test setup shown in **Figure 6.25**. At the input side, the converter is connected to a DC power supply emulating the DC-link of the AC/DC converter stage, whereas at the output side the converter is connected to an electronic load emulating the battery. As for the AC/DC converter, the measurements are performed both with a Teledyne LeCroy 500 MHz, 12-bit, 10 $^{GS}/_{s}$, 8-channel oscilloscope, and with an HBM GEN4tB 2 $^{MS}/_{s}$ data acquisition system. In particular, the data recorder leverages current and voltage sensors with high rated accuracy (i.e., $< 0.1\,\%$) and is exploited to automatically map the converter loss/efficiency over the entire operating region (cf. **Section 6.4.3**) and extract the switching frequency look-up table (LUT) used for the converter control (cf. **Chapter 7**).

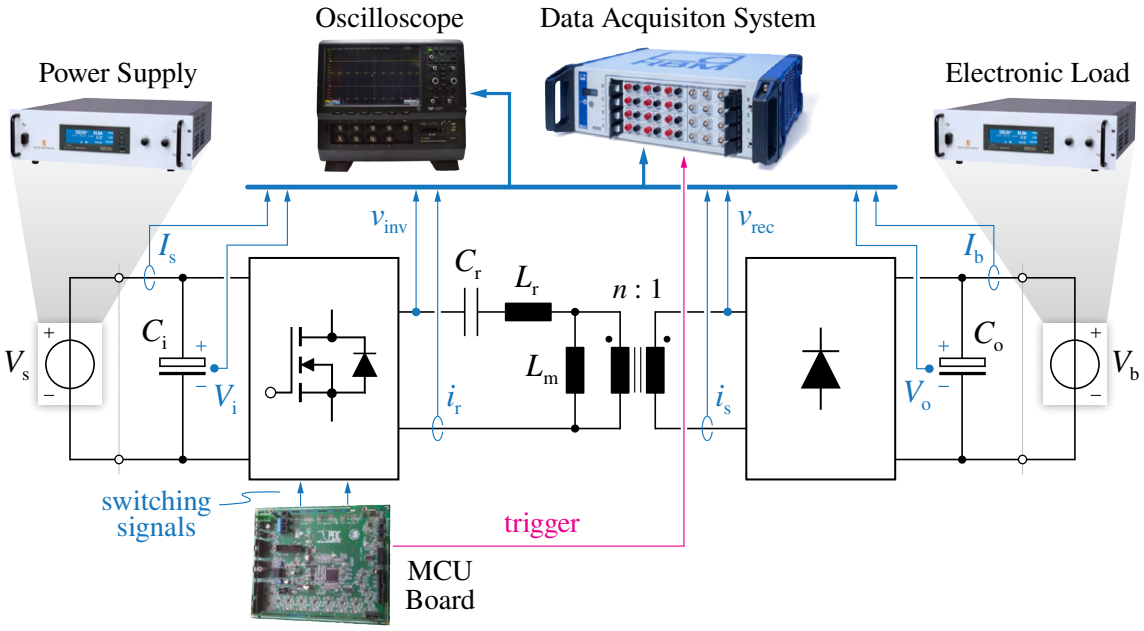


Fig. 6.25: Schematic diagram of the test setup exploited for the characterization of the converter.

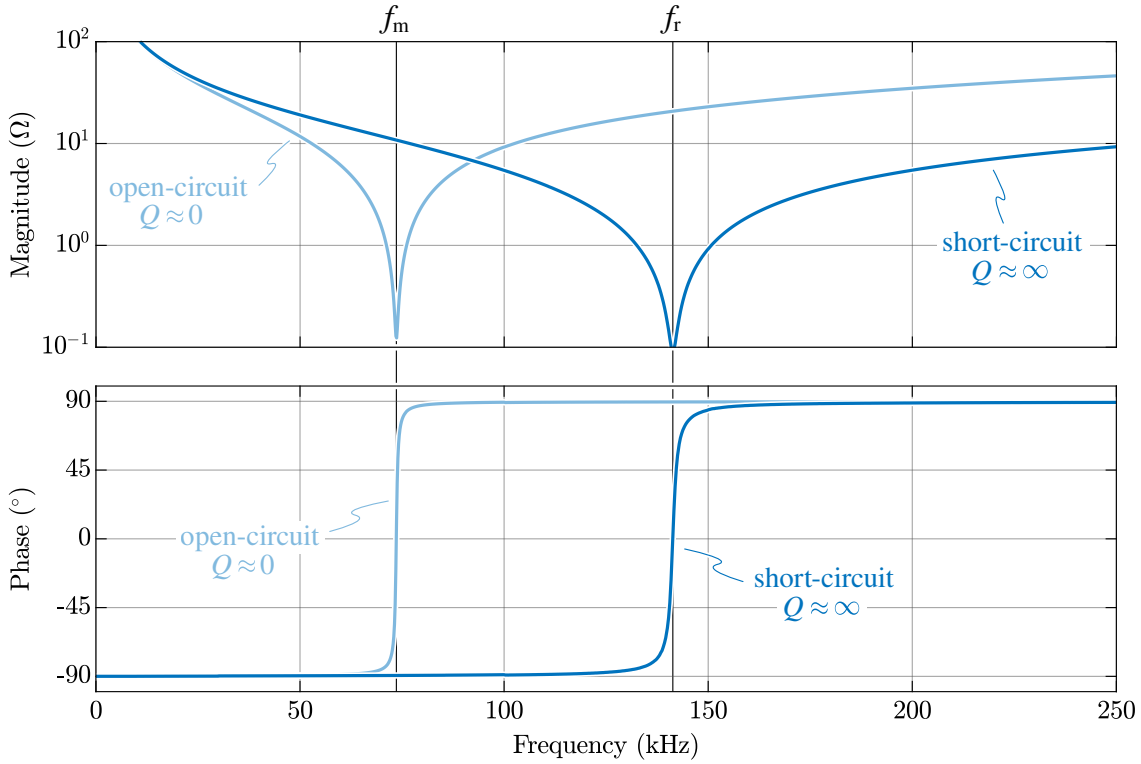


Fig. 6.26: Measured LLC resonant tank impedance with transformer secondary in open-circuit conditions ($Q \approx 0$) and in short-circuit conditions ($Q \approx \infty$).

6.4.1 Resonant Tank Impedance

The resonant tank impedance is measured in two different conditions with a HIOKI 3532-50 LCR meter, as illustrated in **Fig. 6.26**. By short-circuiting the output of the transformers, the equivalent infinite-load condition (i.e., $Q \approx \infty$) is obtained and the primary resonance frequency f_r is identified. Similarly, by disconnecting the secondary-side of the transformers (i.e., open-circuit), the equivalent zero-load condition (i.e., $Q \approx 0$) is obtained, allowing to establish the secondary resonance frequency f_m.

6.4.2 Steady-State Waveforms

The main LLC converter waveforms in stationary conditions are illustrated in **Fig. 6.27**, **Fig. 6.28**, **Fig. 6.29** and **Fig. 6.30** for boost-mode, unity-gain-mode, resonance-mode and buck-mode, respectively. In all figures, the switched current I_{sw} is indicated, highlighting that the ZVS operation of the primary-side transistors is always achieved, being $I_{sw} > 0$ when the inverter voltage transitions from $+V_i$ to $-V_i$ and vice-versa (cf. **Section 5.2.4**). In particular, it is observed that the operation at resonance (i.e., $f_{sw} = f_r$, cf. **Fig. 6.29**) does not coincide with the operation in unity-gain-mode (i.e., $M = 1$, cf. **Fig. 6.28**) because the system losses translate into an input-to-output voltage drop that is addressed by operating at $f_{sw} < f_r$.

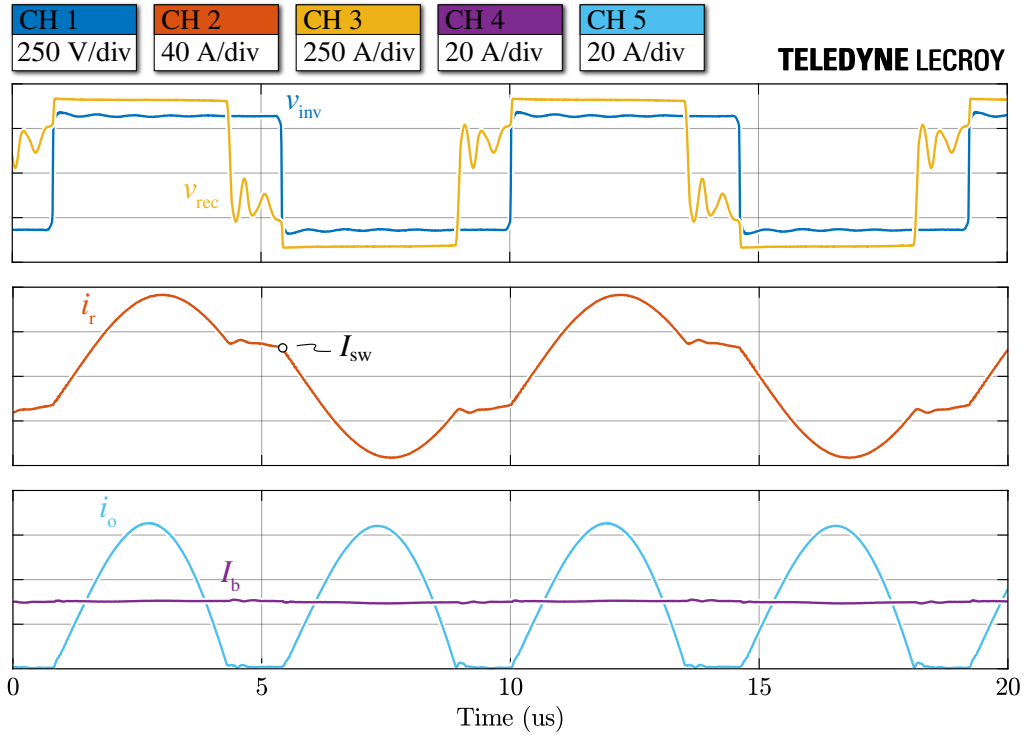


Fig. 6.27: Experimental converter waveforms in steady-state conditions with $V_i = 325\,\text{V}$, $I_o^* = 30\,\text{A}$ (cf. **Chapter 7**) in boost-mode (i.e., $V_o = 405\,\text{V}$, $M \approx 1.25$, $f_{sw} \approx 109\,\text{kHz}$): inverter voltage v_{inv}, rectifier voltage v_{rec}, resonant tank current i_r, output rectified current i_o (i.e., obtained by taking the absolute value of i_s) and battery-side current I_b. The switched current I_{sw} is highlighted.

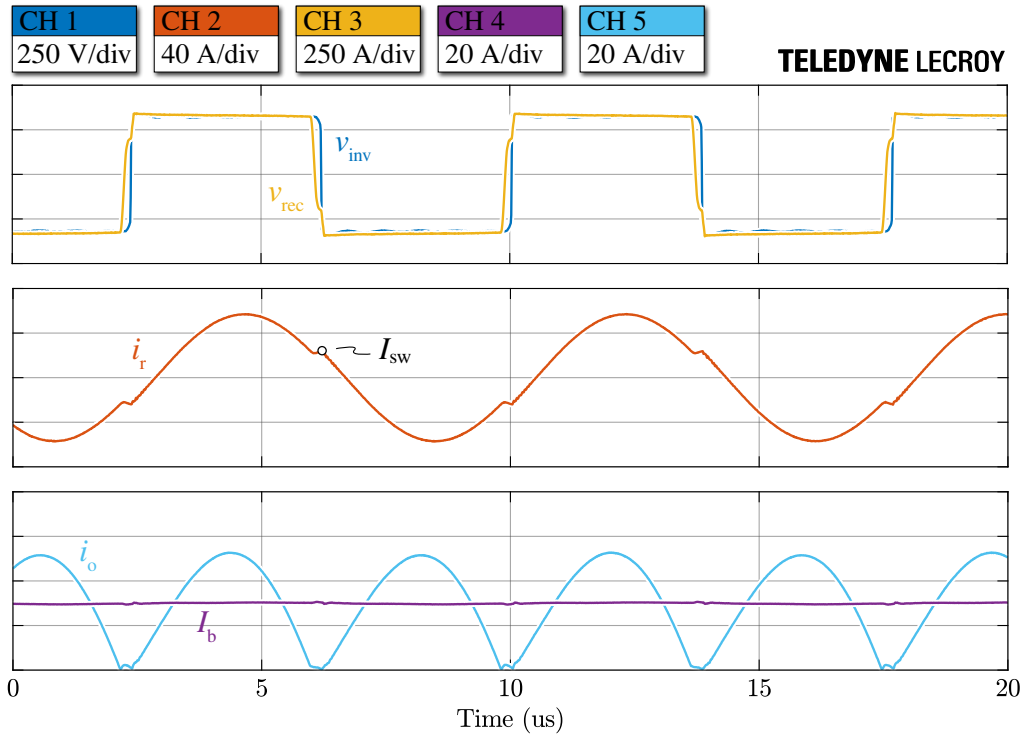


Fig. 6.28: Experimental converter waveforms in steady-state conditions with $V_i = 325\,\text{V}$, $I_o^* = 30\,\text{A}$ (cf. **Chapter 7**) in unity-gain-mode (i.e., $V_o = 325\,\text{V}$, $M = 1$, $f_{sw} \approx 131\,\text{kHz}$): inverter voltage v_{inv}, rectifier voltage v_{rec}, resonant tank current i_r, output rectified current i_o (i.e., obtained by taking the absolute value of i_s) and battery-side current I_b. The switched current I_{sw} is highlighted.

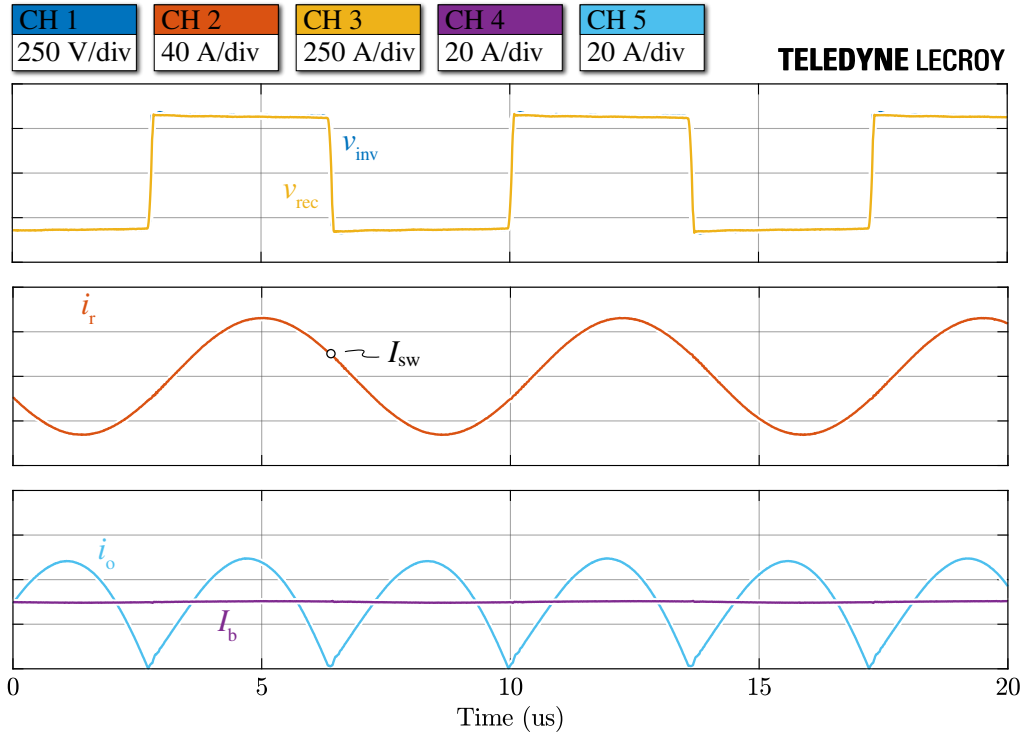


Fig. 6.29: Experimental converter waveforms in steady-state conditions with $V_i = 325\,V$, $I_o^* = 30\,A$ (cf. **Chapter 7**) at resonance (i.e., $V_o = 315\,V$, $M \approx 0.97$, $f_{sw} \approx 140\,kHz$): inverter voltage v_{inv}, rectifier voltage v_{rec}, resonant tank current i_r, output rectified current i_o (i.e., obtained by taking the absolute value of i_s) and battery-side current I_b. The switched current I_{sw} is highlighted.

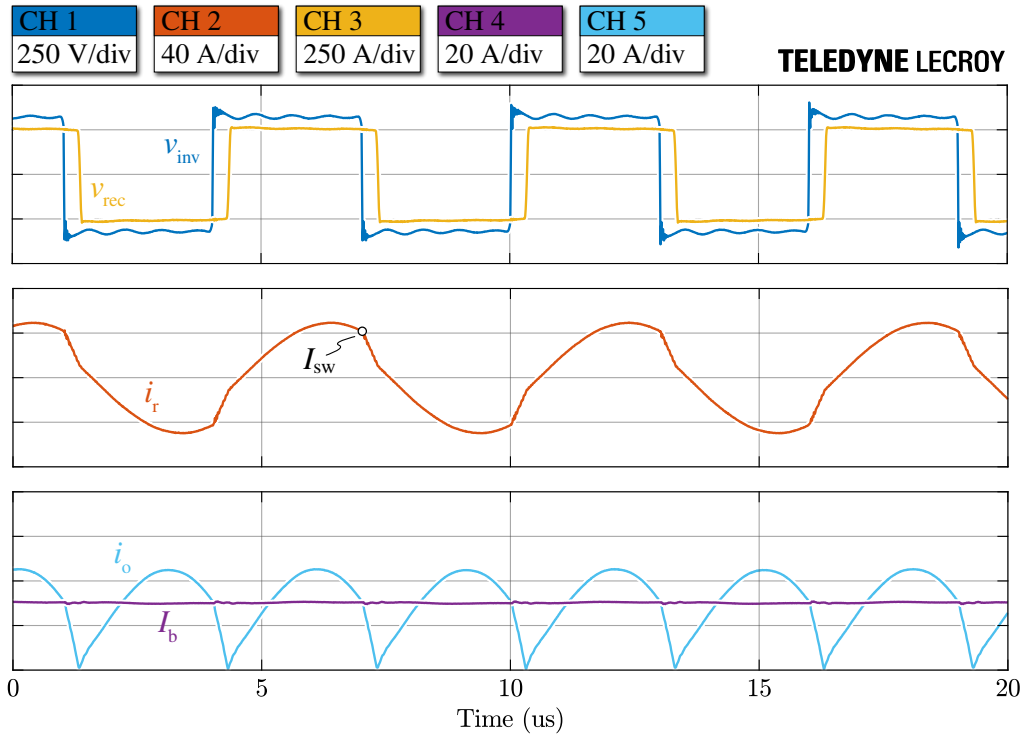


Fig. 6.30: Experimental converter waveforms in steady-state conditions with $V_i = 325\,V$, $I_o^* = 30\,A$ (cf. **Chapter 7**) in buck-mode (i.e., $V_o = 250\,V$, $M \approx 0.77$, $f_{sw} \approx 167\,kHz$): inverter voltage v_{inv}, rectifier voltage v_{rec}, resonant tank current i_r, output rectified current i_o (i.e., obtained by taking the absolute value of i_s) and battery-side current I_b. The switched current I_{sw} is highlighted.

6.4.3 Loss and Efficiency

To obtain the converter loss and efficiency, the DC input power $P_\mathrm{i} = V_\mathrm{i} I_\mathrm{s}$ and the DC output power $P_\mathrm{o} = V_\mathrm{o} I_\mathrm{b}$ are measured with the automated test setup of **Fig. 6.25**.

The LLC converter loss (i.e., $P_\mathrm{i} - P_\mathrm{o}$) and efficiency (i.e., $P_\mathrm{o}/P_\mathrm{i}$) are shown for the entire design operating region in **Fig. 6.31**, where they are compared to the analytical/numerical estimations based on the models presented in **Section 6.3**. It is observed that the converter features 97.6 % efficiency in nominal operating conditions (i.e., $V_\mathrm{i} = V_\mathrm{o} = 400\,\mathrm{V}$, $I_\mathrm{o} = 37.5\,\mathrm{A}$) satisfying and significantly exceeding the initial design target (i.e., $> 97\,\%$, cf. **Tab. 6.1**). Furthermore, a peak efficiency value of 97.8 % is achieved at $V_\mathrm{i} = V_\mathrm{o} = 400\,\mathrm{V}$ and $I_\mathrm{o} \approx 28\,\mathrm{A}$ (i.e., $M = 1$, $P_\mathrm{o} \approx 11.2\,\mathrm{kW}$).

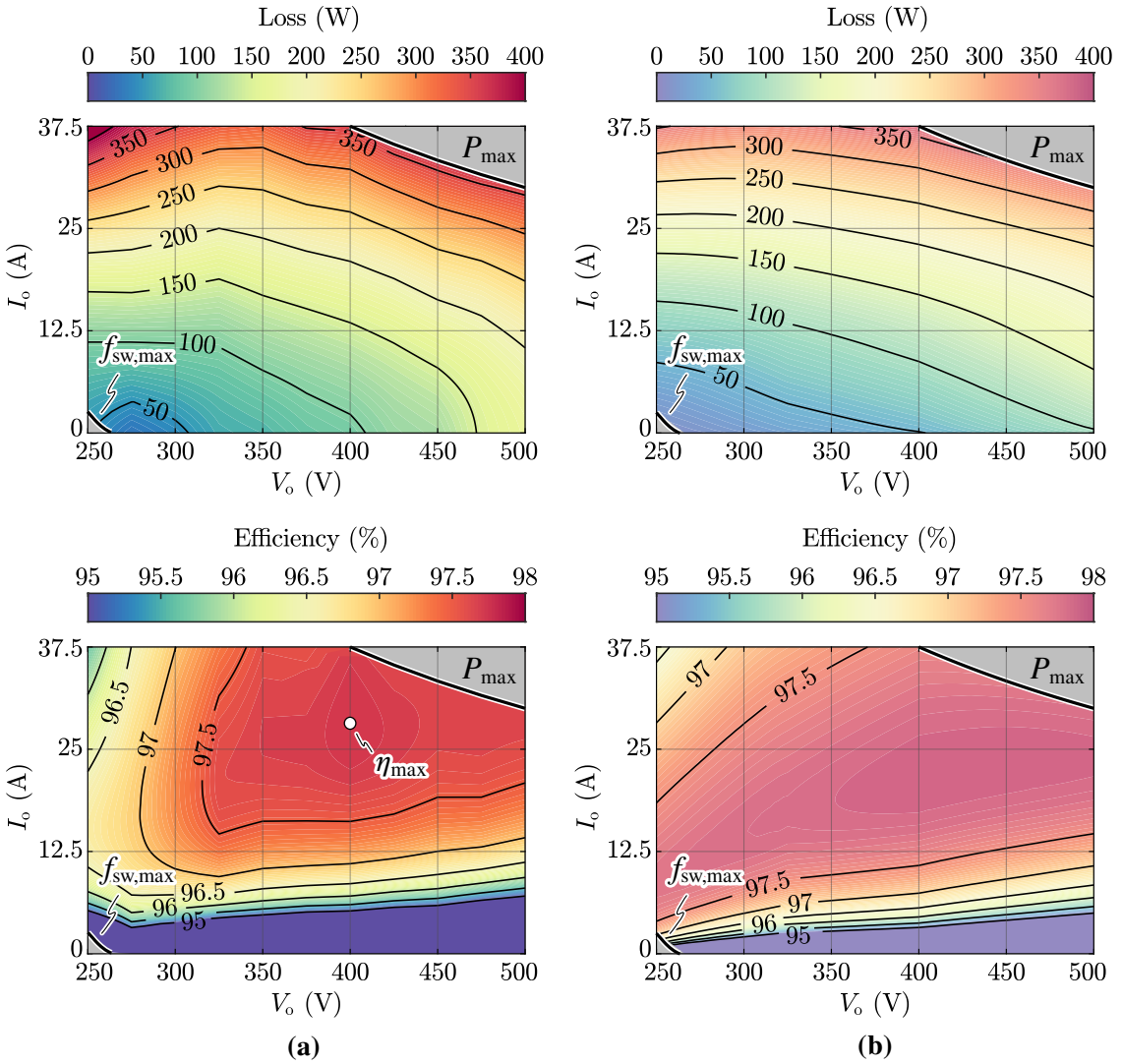


Fig. 6.31: Comparison between **(a)** measured and **(b)** estimated total converter losses and efficiency as functions of the output voltage V_o and the output current I_o over the entire converter operating region.

Overall, good agreement is observed between the analytical/numerical estimations and the experimental results, thus supporting the validity of the proposed design procedure and the accuracy of the adopted loss models. In particular, the loss/efficiency estimation is very accurate in unity-gain-mode (i.e., $325\,\mathrm{V} \leq V_\mathrm{o} \leq 400\,\mathrm{V}$) and in boost-mode (i.e., $V_\mathrm{o} > 400\,\mathrm{V}$), however it becomes less accurate in buck-mode (i.e., $V_\mathrm{o} < 325\,\mathrm{V}$), since the reverse-recovery losses of the diodes are not modeled (cf. **Section 6.3.1**).

6.5 Summary

This chapter has reported the complete design process of the isolated DC/DC converter stage of the considered electric vehicle (EV) ultra-fast battery charger. A novel iterative design procedure for resonant LLC converters, aimed at minimizing the total converter conduction losses, has been proposed and described in detail. This procedure has been then applied to the considered modular 4x15 kW application, assuming an unconventional LLC circuit structure to split the power rating of the magnetic components (i.e., enabling the use of commercially available magnetic cores) and the current rating of the output rectifier diodes (i.e., allowing for the adoption of discrete Si semiconductor devices). Therefore, the selection, sizing and/or optimization of all main converter active and passive components has been performed, including the semiconductor devices (i.e., MOSFETs and diodes), the resonant capacitor, the resonant inductors, the isolation transformers, the input/output filter capacitors and the heat dissipation system (i.e., heatsink and fans). Furthermore, the adopted models for the estimation of the component losses have been reported. Finally, a 15 kW LLC converter prototype has been built and its performance in terms of loss and efficiency has been assessed experimentally, achieving a nominal efficiency of 97.6 % and a peak efficiency of 97.8 %, successfully satisfying the initial design requirements. The validity of the proposed design procedure and the accuracy of the adopted loss models has been supported by the good agreement between analytical/numerical estimations and experimental results.

Chapter 7

DC/DC Converter – Control

Abstract

The DC/DC converter stage of an electric vehicle (EV) ultra-fast battery charger must achieve fast control dynamics and strong disturbance rejection capability to ensure a limited battery-side current ripple. Despite its excellent performance in terms of efficiency, power density and wide output load/voltage regulation, the considered LLC resonant converter is a complex high-order system characterized by a strong non-linear behavior, featuring large variations of the small-signal gain/phase and pole location depending on the operating point. As a consequence, these features pose significant challenges in designing a closed-loop controller and providing constant dynamical performance over a wide operating range. Therefore, this chapter focuses on the design, tuning and experimental assessment of a high-performance digital multi-loop control strategy for the considered LLC resonant converter, aiming at constant closed-loop bandwidth, fast response dynamics and strong disturbance rejection across the complete converter operating region. The control scheme consists of two cascaded voltage and current loops. To design and tune these controllers, a novel simplified LLC dual first order small-signal model is proposed. The system non-linear behavior affecting the current control loop is counteracted by a real-time controller gain adaptation process, which ensures constant control bandwidth. In particular, the adaptive gain values are provided by a static switching frequency look-up table (LUT) obtained experimentally. Moreover, the steady state switching frequency value is fed forward at the output of the current loop regulator, providing a further dynamical performance enhancement. Finally, the steady-state and dynamical performance of the current control loop are verified both in circuit simulation and experimentally on the 15 kW LLC converter prototype, adopting a general purpose microcontroller unit (MCU) for the digital control implementation. The results demonstrate the superior reference tracking and disturbance rejection performance of the proposed control strategy with respect to a state-of-the-art solution based on a proportional-integral (PI) regulator.

7.1 Introduction

The control requirements of the considered LLC resonant converter can be summarized in

- regulated output current, to control the charging process;
- low battery-side current ripple, to limit the premature aging of the battery itself [119];
- strong disturbance rejection capability, especially to avoid the low-frequency input voltage oscillation generated by the AC/DC stage (cf. **Section 2.4.2**) to pass through;
- consistent dynamical performance across the complete operating range (i.e., under variable input/output voltages and output load).

All of these tasks must be addressed with a proper converter control strategy featuring adequate dynamical performance, which is therefore the subject of this chapter.

The main challenges in achieving the mentioned control requirements are related to the non-linear multi-resonant nature of the LLC converter, which causes large system transfer function variations with varying input/output voltage gain and load [154, 155]. The system dynamics are in fact highly dependent on the operating point, leading to a challenging control design if fast, consistent and stable control performance must be achieved.

Most low-power LLC converters directly control the voltage across a resistive load, therefore the most widespread control solution is based on an analog closed-loop control of the output voltage, exploiting a voltage-controlled oscillator (VCO) to regulate the switching frequency [151, 170]. However, battery chargers operate most of the time in constant-current (CC) mode, therefore the direct closed-loop control of the converter output current must be provided. Moreover, due to the advent of modern powerful and low-cost digital signal processors (DSPs), industry is increasingly pushing for digital control implementations. The benefits of digital controllers are well known and mainly consist in high degree of reproducibility, strong noise immunity and great flexibility, together with the opportunity of implementing complex control strategies and look-up tables (LUTs) [100]. Nevertheless, the digital implementation is affected by some drawbacks, such as sampling and quantization effects, limited resolution is generating output signals, limited computational speed and zero-order hold (ZOH) effects. In particular, for variable-frequency resonant converter applications, the limited DSP clock resolution may cause limit-cycle oscillations during normal operation [153].

In recent years, several LLC digital control strategies have been published, either implementing a single-loop direct output voltage control [171, 172] (i.e., not applicable to battery charging applications) or a direct output current control with/without an external

voltage loop, depending on the load kind (e.g., resistive, battery, LED) [173–178]. The authors in [173] propose a dual-loop control strategy for wide input/output voltage gain battery charging applications, featuring a direct output current control. However, no details on the controller design and/or tuning procedure are provided and no assessment of the dynamical control performance is carried out. A current loop controller design procedure is reported in [174], aiming to stabilize the performance of the outer voltage loop by providing high-enough closed-loop current control bandwidth and thus sufficient dynamical decoupling between the two loops. Nevertheless, also in this case no detailed controller tuning procedure is provided and the control dynamics are assessed focusing on the outer voltage loop, providing no insight on the inner current control loop performance. An effective approach to attenuate the typical input DC-link voltage oscillation of single-phase converters is proposed in [175] and [176], where a resonant controller tuned at the disturbance frequency is placed in parallel to a conventional proportional-integral (PI) or purely integral (I) controller. Both solutions obtain excellent disturbance rejection results, achieving little output current ripple in steady-state conditions. However, the resonant controller does not enhance the control performance outside its tuning frequency, leaving the closed-loop dynamics unaltered with respect to a conventional PI/I controller implementation and thus subject to the large system gain variations. A load feedback linearization approach is adopted in [177] to counteract the system non-linear behavior and provide consistent dynamical performance across the LLC operating range. In particular, FHA is leveraged to derive a linearization function used inside the output current control loop to compensate the system gain variations. Nevertheless, several system simplifications are made to obtain a practical model for the real-time control implementation and significant inaccuracy is obtained as a result. This inaccuracy directly translates into an imperfect compensation of the system gain and thus inconsistent closed-loop dynamical performance. No assessment of the current control dynamics is provided in [177], as only the outer voltage loop is experimentally verified. Finally, in [178] a dual-loop voltage-current controller is designed leveraging analytically derived expressions, providing a simple and straightforward controller design procedure. Specifically, the PI regulator of the inner current control loop is tuned at the resonance frequency, identified as the most critical operating point in terms of gain/phase margin. However, the linear PI regulator in [178] cannot counteract the large system gain variations with the operating point, therefore resulting in poor dynamical performance when moving away from resonance. Also in this case, the experimental assessment is only performed for the outer voltage loop, thus providing no insight on the current control loop performance.

Therefore, this chapter describes in detail the design, tuning, simulation and experimental verification of a novel digital multi-loop control strategy for LLC resonant converters

targeting constant control bandwidth and strong disturbance rejection across the complete converter operating region. In particular, the fast and consistent dynamical performance required by the application is mainly achieved with a real-time controller gain adaptation process complemented by a feedforward action, leveraging a static switching frequency LUT obtained by experimental characterization of the converter. Remarkably, to enable a straightforward analytical tuning of the cascaded voltage and current controllers, a novel simplified dual first order small-signal model of the LLC converter is proposed.

Part of the content of this chapter has been published in [179] and [157].

7.2 System Small-Signal Model

The equivalent circuit schematic of the considered full-bridge LLC resonant converter system is illustrated in **Fig. 5.2**. Nevertheless, it is worth noting that all considerations can be extended to the half-bridge LLC topology by simply considering half of the input voltage square-wave amplitude. Assuming an ideal input voltage source (i.e., $R_\mathrm{s} \approx 0$, $V_\mathrm{s} \approx V_\mathrm{i}$), the system is characterized by four state variables: the resonant inductor current i_r, the resonant capacitor voltage v_c, the transformer magnetizing current i_m and the output capacitor voltage V_o. Since the inverter full-bridge is assumed to be controlled by frequency modulation at 50 % duty cycle (i.e., no phase-shift control), the only system input variable is the inverter switching frequency f_sw, whereas the input capacitor voltage V_i, the battery equivalent series resistance R_b and the battery open-circuit voltage V_b can be considered as system parameters or disturbances. Due to the high order of the system and the non-linear behavior of both inverter and rectifier stages, the LLC control design is fairly complicated and requires appropriate mathematical models.

Therefore, this section aims to provide a complete analysis of the LLC resonant converter small-signal behavior and provide useful tools for the controller design and tuning. In particular, the well known LLC seventh order model is explained in **Section 7.2.1** and the transfer function linking the switching frequency to the output current is analyzed in detail. In **Section 7.2.2**, a recently developed LLC third order model is briefly described, acting as foundation for the following section. Finally, a novel decoupled dual first order small-signal model (i.e., divided in two dynamically independent AC and DC subsystems), is proposed in **Section 7.2.3**, aiming to provide simple and straightforward plant transfer functions for the design of the current and voltage controllers.

7.2.1 Full 7th Order System Model

The most widespread approach to derive an accurate small-signal model of the LLC resonant converter is the extended describing function (EDF) method [171, 176–178, 180, 181], which is described in the following.

The LLC converter may be functionally divided into different subsystems, namely the input source, the inverter bridge, the resonant tank, the diode rectifier bridge and the output load, as illustrated in **Fig. 5.3**. The inverter bridge behaves as a non-linear block and generates an output square wave $v_{\text{inv}}(t)$ containing a fundamental component and an infinite number of harmonics, as reported in (5.1). These harmonics are heavily attenuated by the band-pass filtering action of the resonant tank (i.e., when $f_{\text{sw}} \approx f_{\text{r}}$), which in turn generates a pseudo-sinusoidal resonant current i_{r} [180]. The difference between the resonant current i_{r} and the magnetizing current i_{m} (i.e., the primary-side transformer current i_{p}) is rectified by the diode bridge, which also behaves as a non-linear block. In turn, the diode bridge generates a voltage square wave $v_{\text{rec}}(t)$ at its input and performs a frequency shift of $i_{\text{s}} = n\, i_{\text{p}}$ at its output, yielding the output rectified current i_{o}. Finally, the output load behaves as a low-pass filter, attenuating the harmonics of i_{o} and making sure that a DC current flows into the battery. Therefore, the system state-space model can be described by a set of non-linear equations:

$$
\begin{cases}
\dfrac{\mathrm{d}i_{\text{r}}(t)}{\mathrm{d}t} = \dfrac{1}{L_{\text{r}}}\left[v_{\text{inv}}(t) - v_{\text{c}}(t) - n\, v_{\text{rec}}(t)\right] & (7.1)\\[2ex]
\dfrac{\mathrm{d}v_{\text{c}}(t)}{\mathrm{d}t} = \dfrac{1}{C_{\text{r}}}\, i_{\text{r}}(t) & (7.2)\\[2ex]
\dfrac{\mathrm{d}i_{\text{m}}(t)}{\mathrm{d}t} = \dfrac{1}{L_{\text{m}}}\, n\, v_{\text{rec}}(t) & (7.3)\\[2ex]
\dfrac{\mathrm{d}V_{\text{o}}(t)}{\mathrm{d}t} = \dfrac{1}{C_{\text{o}}}\left(i_{\text{o}}(t) - \dfrac{V_{\text{o}}(t) - V_{\text{b}}}{R_{\text{b}}}\right) & (7.4)
\end{cases}
$$

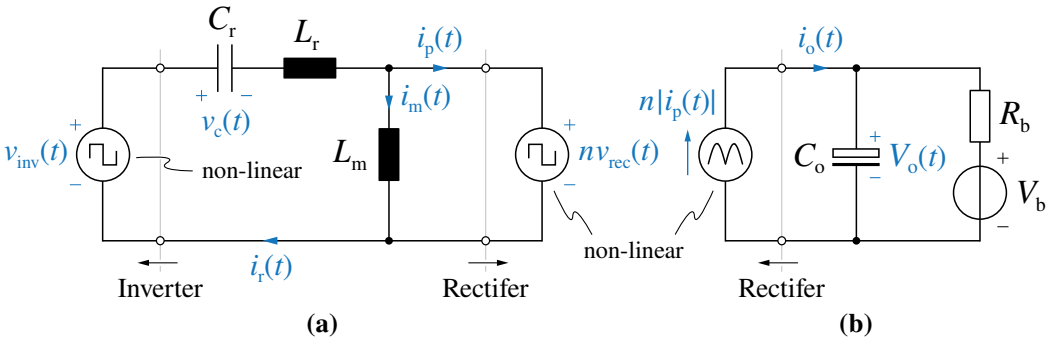


Fig. 7.1: Equivalent circuit representation of the considered full-bridge LLC converter state-space model, separated into **(a)** AC subsystem and **(b)** DC subsystem.

where the non-linear terms are represented by $v_{\mathrm{inv}}(t)$, $v_{\mathrm{rec}}(t) = V_{\mathrm{o}}(t)\,\mathrm{sign}[i_{\mathrm{r}}(t) - i_{\mathrm{m}}(t)]$ and $i_{\mathrm{o}}(t) = n\,|i_{\mathrm{r}}(t) - i_{\mathrm{m}}(t)|$. The equivalent circuit representation of (7.1)–(7.4) is reported in **Fig. 7.1**, highlighting the functional separation between AC and DC subsystems.

Because of the band-pass filtering action of the resonant tank, the higher order harmonics of the tank variables can be neglected without incurring in a significant loss of accuracy (cf. **Section 5.2.1**). Therefore, FHA is applied and pure sinusoidal quantities are considered within the AC subsystem. This allows to express a generic AC state variable $x(t)$ with frequency f_{sw} as a combination of two independent sine and cosine components, as

$$x(t) = X_{\mathrm{s}}(t)\,\sin(2\pi f_{\mathrm{sw}} t) - X_{\mathrm{c}}(t)\,\cos(2\pi f_{\mathrm{sw}} t), \tag{7.5}$$

leading to the following derivative expression

$$\frac{\mathrm{d}x(t)}{\mathrm{d}t} = \left[\frac{\mathrm{d}X_{\mathrm{s}}(t)}{\mathrm{d}t} + 2\pi f_{\mathrm{sw}} X_{\mathrm{c}}(t)\right]\sin(2\pi f_{\mathrm{sw}} t) - \left[\frac{\mathrm{d}X_{\mathrm{c}}(t)}{\mathrm{d}t} - 2\pi f_{\mathrm{sw}} X_{\mathrm{s}}(t)\right]\cos(2\pi f_{\mathrm{sw}} t). \tag{7.6}$$

As a consequence of the sine/cosine component split, six AC state variables are obtained, namely I_{rs}, I_{rc}, V_{cs}, V_{cc}, I_{ms}, I_{mc}. In a similar manner, due to the low-pass filtering action of the output load, only average (i.e., DC) components are taken into account within the DC subsystem, transforming i_{o} into I_{o}.

The non-linear terms within (7.1)–(7.4), namely $v_{\mathrm{inv}}(t)$, $v_{\mathrm{rec}}(t)$ and $i_{\mathrm{o}}(t)$, can be linearized by considering their fundamental components (for AC quantities) or their average components (for DC quantities). These linearized expressions are referred to as extended describing functions [180]:

$$v_{\mathrm{inv}}(t) = \frac{4}{\pi} V_{\mathrm{i}}\,\sin(2\pi f_{\mathrm{sw}} t), \tag{7.7}$$

$$v_{\mathrm{rec}}(t) = \frac{4}{\pi} V_{\mathrm{o}} \left[\frac{I_{\mathrm{rs}} - I_{\mathrm{ms}}}{I_{\mathrm{p}}}\sin(2\pi f_{\mathrm{sw}} t) - \frac{I_{\mathrm{rc}} - I_{\mathrm{mc}}}{I_{\mathrm{p}}}\cos(2\pi f_{\mathrm{sw}} t)\right], \tag{7.8}$$

$$i_{\mathrm{o}}(t) = I_{\mathrm{o}} = \frac{2}{\pi} n I_{\mathrm{p}}, \tag{7.9}$$

where I_{p} is the amplitude of the transformer primary current, defined as

$$I_{\mathrm{p}} = \sqrt{(I_{\mathrm{rs}} - I_{\mathrm{ms}})^2 + (I_{\mathrm{rc}} - I_{\mathrm{mc}})^2}. \tag{7.10}$$

Finally, substituting the sinusoidal expressions (7.5), (7.6) and the linearized terms (7.7)–(7.9) into (7.1)–(7.4) and separating sine and cosine components, the following

system state equations are obtained:

$$\begin{cases} \dfrac{\mathrm{d}I_{\mathrm{rs}}}{\mathrm{d}t} = -2\pi f_{\mathrm{sw}} I_{\mathrm{rc}} + \dfrac{1}{L_{\mathrm{r}}}\left(\dfrac{4}{\pi}V_{\mathrm{i}} - V_{\mathrm{cs}} - \dfrac{4}{\pi}nV_{\mathrm{o}}\dfrac{I_{\mathrm{rs}} - I_{\mathrm{ms}}}{I_{\mathrm{p}}}\right) & (7.11) \\ \dfrac{\mathrm{d}I_{\mathrm{rc}}}{\mathrm{d}t} = 2\pi f_{\mathrm{sw}} I_{\mathrm{rs}} - \dfrac{1}{L_{\mathrm{r}}}\left(V_{\mathrm{cc}} + \dfrac{4}{\pi}nV_{\mathrm{o}}\dfrac{I_{\mathrm{rc}} - I_{\mathrm{mc}}}{I_{\mathrm{p}}}\right) & (7.12) \\ \dfrac{\mathrm{d}V_{\mathrm{cs}}}{\mathrm{d}t} = -2\pi f_{\mathrm{sw}} V_{\mathrm{cc}} + \dfrac{1}{C_{\mathrm{r}}} I_{\mathrm{rs}} & (7.13) \\ \dfrac{\mathrm{d}V_{\mathrm{cc}}}{\mathrm{d}t} = 2\pi f_{\mathrm{sw}} V_{\mathrm{cs}} + \dfrac{1}{C_{\mathrm{r}}} I_{\mathrm{rc}} & (7.14) \\ \dfrac{\mathrm{d}I_{\mathrm{ms}}}{\mathrm{d}t} = -2\pi f_{\mathrm{sw}} I_{\mathrm{mc}} + \dfrac{1}{L_{\mathrm{m}}}\dfrac{4}{\pi}nV_{\mathrm{o}}\dfrac{I_{\mathrm{rs}} - I_{\mathrm{ms}}}{I_{\mathrm{p}}} & (7.15) \\ \dfrac{\mathrm{d}I_{\mathrm{mc}}}{\mathrm{d}t} = 2\pi f_{\mathrm{sw}} I_{\mathrm{ms}} + \dfrac{1}{L_{\mathrm{m}}}\dfrac{4}{\pi}nV_{\mathrm{o}}\dfrac{I_{\mathrm{rc}} - I_{\mathrm{mc}}}{I_{\mathrm{p}}} & (7.16) \\ \dfrac{\mathrm{d}V_{\mathrm{o}}}{\mathrm{d}t} = \dfrac{1}{C_{\mathrm{o}}}\left(\dfrac{2}{\pi}nI_{\mathrm{p}} - \dfrac{V_{\mathrm{o}} - V_{\mathrm{b}}}{R_{\mathrm{b}}}\right) & (7.17) \end{cases}$$

Remarkably, the subdivision of each AC variable into its sine and cosine components leads to an increase of the system order, from four to seven. The system state equations (7.11)–(7.17) represent the large-signal model of the LLC resonant converter and can be

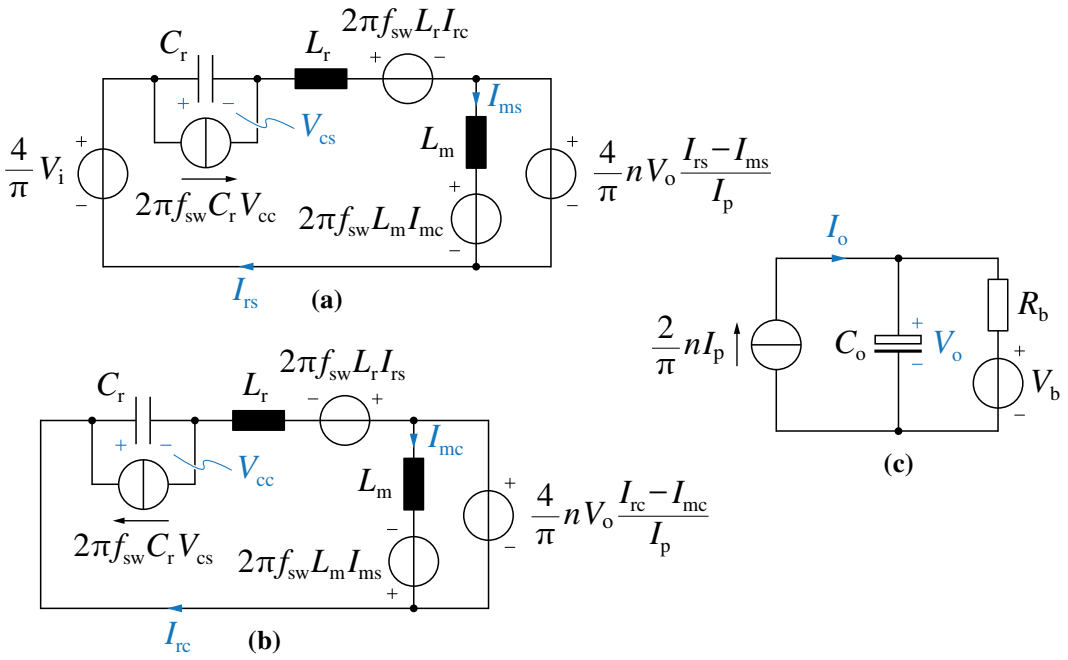


Fig. 7.2: Seventh order large-signal equivalent circuit of the considered full-bridge LLC converter: **(a)** sine components of the AC subsystem (7.11), (7.13), (7.15), **(b)** cosine components of the AC subsystem (7.12), (7.14), (7.16), **(c)** DC subsystem (7.17).

alternatively expressed with a set of coupled electrical equivalent circuits, as illustrated in **Fig. 7.2**. In particular, **Fig. 7.2(a)** and **(b)** represent the AC subsystem (7.11)–(7.16) (i.e., the resonant tank dynamics), whereas **Fig. 7.2(b)** represents the DC subsystem (7.17) (i.e., the output filter dynamics).

It is worth noting that, even though the EDF method linearizes the input inverter operation through FHA, the approximated output rectifier operation still yields non-linear voltage and current terms, arising from the product of two or more state variables. Therefore, to achieve a linear state-space representation of the system, equations (7.11)–(7.17) must be linearized around the converter operating point. The non-linear system equations can be represented in the form

$$\begin{cases} \dot{X}(t) = F(X(t), U(t)) \\ Y(t) = G(X(t), U(t)) \end{cases}, \tag{7.18}$$

where $X = [I_{\mathrm{rs}}, I_{\mathrm{rc}}, V_{\mathrm{cs}}, V_{\mathrm{cc}}, I_{\mathrm{ms}}, I_{\mathrm{mc}}, V_{\mathrm{o}}]^{\mathrm{T}}$ is the state vector, $U = f_{\mathrm{sw}}$ is the input vector and Y is the output vector (i.e., $Y = V_{\mathrm{o}}$ or $Y = I_{\mathrm{o}}$, depending on the desired system output). In order to proceed with a small-signal perturbation analysis, (7.18) must be linearized around an equilibrium working point. The general steady-state solution $(\bar{X}, \bar{Y})$ of a non-linear system in response to a constant input $\bar{U}$ is found by solving numerically

$$\begin{cases} 0 = F(\bar{X}, \bar{U}) \\ \bar{Y} = G(\bar{X}, \bar{U}) \end{cases}. \tag{7.19}$$

Introducing a small-signal perturbation at the input $\tilde{U} = \tilde{f}_{\mathrm{sw}}$, the state and output perturbations $\tilde{X}$ and $\tilde{Y}$ are obtained. Developing a first-order Taylor expansion of functions G and F around the operating point $(\bar{X}, \bar{U})$, the linearized system

$$\begin{cases} \dot{\tilde{X}} \approx A\tilde{X} + B\tilde{U} \\ \tilde{Y} \approx C\tilde{X} + D\tilde{U} \end{cases} \tag{7.20}$$

is obtained, where $A = \frac{\partial F}{\partial X}\big|_{\bar{X},\bar{U}}$, $B = \frac{\partial F}{\partial U}\big|_{\bar{X},\bar{U}}$, $C = \frac{\partial G}{\partial X}\big|_{\bar{X},\bar{U}}$ and $D = \frac{\partial G}{\partial U}\big|_{\bar{X},\bar{U}}$ are the system Jacobian matrices evaluated at the selected equilibrium operating point $(\bar{X}, \bar{U})$ and their expressions are provided in **Appendix 7.A**. In particular, the eigenvalues of matrix A represent the poles of the seventh order system linearized around an equilibrium point and thus determine the system dynamical response to a perturbation. The complete small-signal model of the LLC converter can be represented with the set of coupled equivalent electrical circuits reported in **Fig. 7.3**.

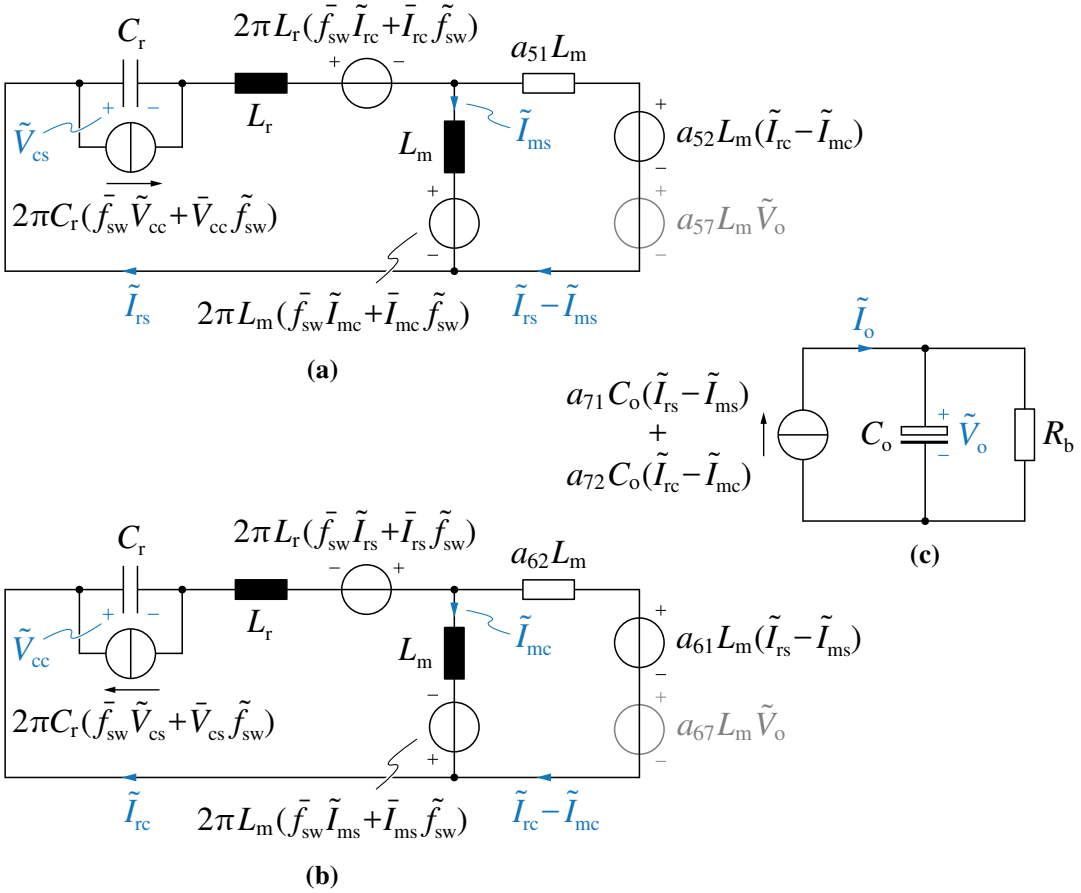


Fig. 7.3: Linearized seventh order small-signal equivalent circuit of the considered full-bridge LLC converter assuming a switching frequency perturbation $\tilde{f}_{sw}$: **(a)** sine components of the AC subsystem, **(b)** cosine components of the AC subsystem, **(c)** DC subsystem. The two voltage sources related to $\tilde{V}_o$ are transparent since they can be disregarded when the output voltage dynamics are neglected (i.e., $V_o \approx \bar{V}_o$). The values of a_{ij} are reported in **Appendix 7.A**.

Since the main LLC control design and tuning challenges are related to the current control loop (cf. **Section 7.3**), a particular focus is dedicated to the switching frequency-to-output current transfer function $\tilde{I}_o(s)/\tilde{f}_{sw}(s)$, considering $\tilde{Y} = \tilde{I}_o$ as system output in (7.20). It is worth noting that the sixth order AC subsystem (7.11)–(7.16) and the first order DC subsystem (7.17) are considered to be completely decoupled in the following, since the resonant tank dynamics are typically much faster than the output filter ones [177] and the adopted dual-loop control strategy features a switching frequency feedforward term within the current control loop that directly compensates the output voltage variations (cf. **Section 7.3.1**). Therefore, V_o can be considered as a given parameter (i.e., equal to the equilibrium value $\bar{V}_o$) in (7.11)–(7.16), simplifying the current control plant transfer function $\tilde{I}_o(s)/\tilde{f}_{sw}(s)$. A qualitative overview of the pole location p_i and transfer function shape in boost-mode ($V_o > V_i$), unity-gain-mode ($V_o = V_i$) and buck-mode ($V_o < V_i$) is reported in **Fig. 7.4(a)**, **(b)** and **(c)**, respectively, highlighting the pole movement and the transfer function variation with the converter quality factor Q (i.e., related to the equilibrium load point $\bar{I}_o$).

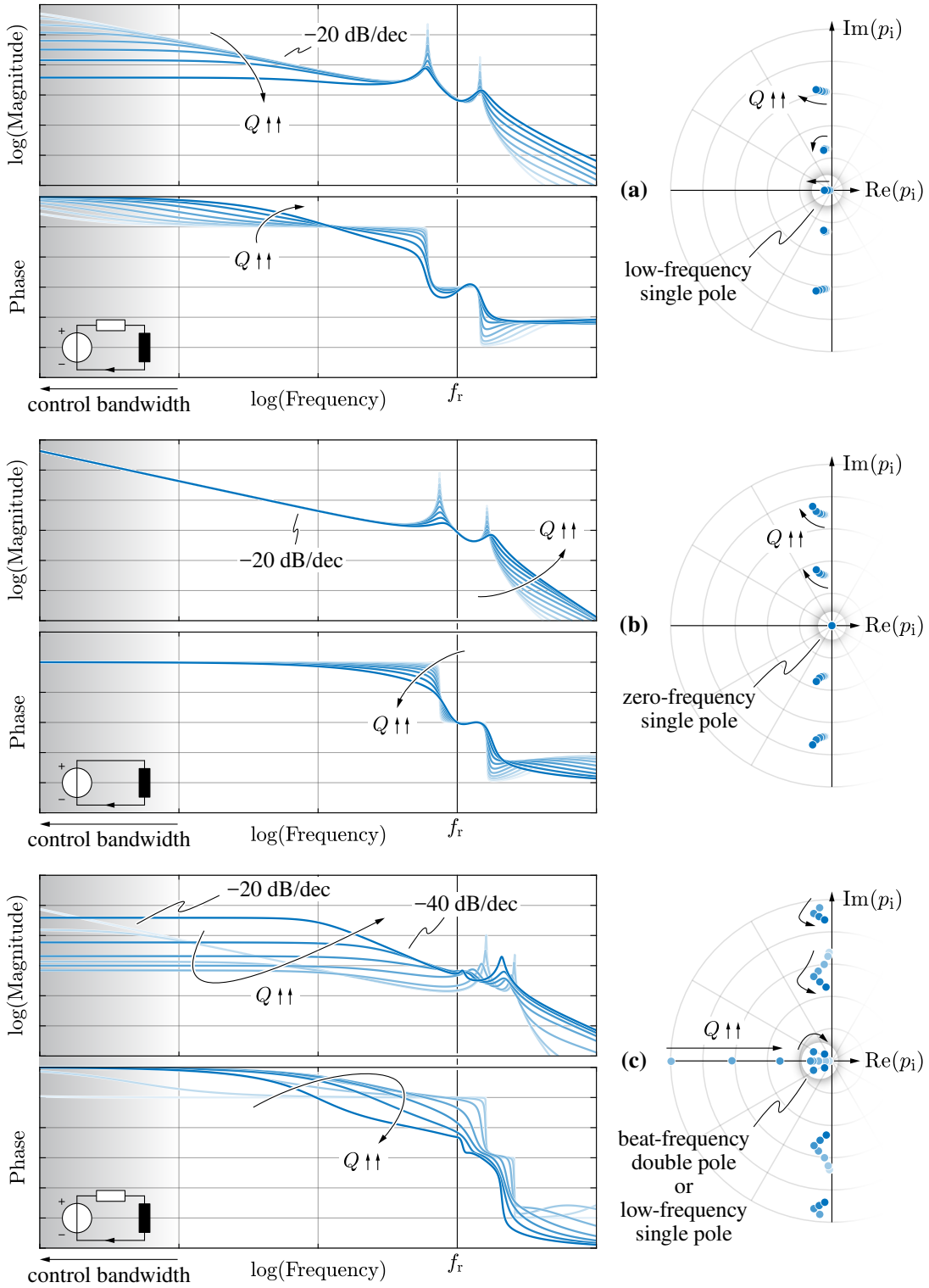


Fig. 7.4: Qualitative overview of the sixth order AC subsystem transfer function $\tilde{I}_o(s)/\tilde{f}_{sw}(s)$ poles p_i, magnitude and phase in **(a)** boost-mode operation ($V_o > V_i$), **(b)** unity-gain-mode operation ($V_o = V_i$) and **(c)** buck-mode operation ($V_o < V_i$) for different values of quality factor Q. The AC and DC subsystems are assumed to be decoupled (i.e., $V_o \approx \bar{V}_o$). The dominant pole or pole pair is highlighted. The typical region of interest for the controller design is located 1–2 decades below the resonance frequency f_r, where the system approximately behaves as a first-order low-pass filter (i.e., RL circuit) in **(a)** and **(c)**, or as a pure integrator (i.e., L circuit) in **(b)**.

Fig. 7.4(b) represents the LLC small-signal operation in unity-gain-mode, where the inverter switching frequency f_{sw} is equal to the resonance frequency f_r. It is observed that the transfer function is characterized by a single dominant pole in the origin of the root locus and both low-frequency gain and phase are unaffected by the load current value, which only modifies the high-frequency behavior of the transfer function. Therefore, being the controller bandwidth typically placed 1–2 decades lower than the resonance frequency f_r, in this region the system practically behaves as a pure integrator.

A similar behavior is observed for boost-mode operation in **Fig. 7.4(a)**, where $f_{sw} < f_r$. The low-frequency system transfer function features a first order low-pass filter characteristic with a single dominant pole that moves towards the origin of the root locus for decreasing load values (i.e., increasing f_{sw}).

Finally, **Fig. 7.4(c)** represents the system operation in buck-mode, where $f_{sw} > f_r$. A very different behavior is observed in this case, as the system transfer function shape and characteristics change significantly with the output load. In particular, in light load conditions the system features a single dominant pole near the origin of the root locus. The load increase and the simultaneous reduction of the switching frequency shift the dominant pole location to higher frequencies, up to when this pole encounters another real pole, merging into an imaginary dominant pole pair known as beat-frequency double pole (i.e., $f_b = f_{sw} - f_r$) [180]. Increasing further the system output load, the beat-frequency reduces, the small-signal steady-state gain increases and the imaginary pole pair gets more and more damped. Therefore, when the output load exceeds a specified threshold value dependent on the input/output voltage gain (i.e., referred to as the *V* region in series resonant converters [180]) the double pole splits again and a single dominant pole is obtained. As the beat-frequency double pole typically in no conditions gets near to the control bandwidth region (i.e., either due to the pole splitting when $V_o \approx V_i$, or due to the high pole frequency at maximum load for $V_o < V_i$), the system transfer function may be treated as a first order low-pass filter, similarly to boost-mode operation.

Therefore, even though the AC subsystem can only be fully characterized with a sixth order model, the transfer function analysis highlights the opportunity of representing the main system features with a simplified small-signal model, valid within the frequency region of interest for the controller design.

7.2.2 Reduced 3rd Order System Model

A reduced LLC third order small-signal model is derived in [182], adopting the same approach of [180] and [183] developed for the series resonant converter. The model order reduction is mainly obtained by approximating the resonant capacitor C_r small-signal

behavior as the one of an equivalent inductor. This approximation is described in detail in [183] and maintains validity for perturbation frequency values much lower than the converter switching frequency (i.e., $|j\omega| \ll 2\pi f_{sw}$). Treating the resonant capacitor as an equivalent inductor allows to directly reduce the order of the system by two (i.e., from seven to five), as the newly defined equivalent inductor is in series with L_r. Moreover, by leveraging the superimposition principle and performing several circuit manipulations, the considered system is further simplified in [182] and a reduced third order small-signal model is obtained.

This model is represented in equivalent circuit form in **Fig. 7.5**, assuming $\tilde{f}_{sw}$ as the only system perturbation. The expressions of the circuit component values are reported in [182]. It is observed that AC and DC subsystems are coupled through $\tilde{V}_o$ and $\tilde{I}_p$, as the dynamics of the two circuits are not assumed to be independent. The passive components within the AC subsystem model different small-signal features, namely:

- R_e represents the total resonant tank impedance at the operating switching frequency [184, 185], as it determines the small-signal current value at steady-state. Therefore, $R_e = 0$ at $f_{sw} = f_r$ and increases in buck and boost modes [184, 185]. It is worth noting that [182] considers $R_e \approx 0$ in boost-mode operation due to the typically low resonant tank impedance value, nevertheless this is not valid in general.
- L_e represents the integral behavior of the resonant tank and in unity-gain-mode and boost-mode directly defines the high-frequency dynamical evolution of the small-signal current.
- C_e represents the buck-mode beat-frequency double pole dynamics, being defined as $C_e = 1/4\pi^2 L_e (f_{sw} - f_r)^2$ for $f_{sw} > f_r$ and $C_e = 0$ for $f_{sw} \leq f_r$. In particular, the pole splitting phenomenon is determined by $R_e/\sqrt{L_e/C_e} > 0.5$ and is either achieved for large values of R_e (i.e., light-load conditions, $f_{sw} \gg f_r$) or for large values of C_e (i.e., heavy-load conditions, $f_{sw} \approx f_r$) [184, 185].

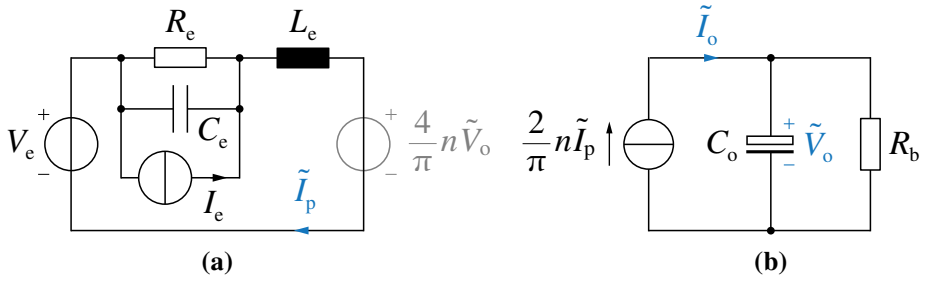


Fig. 7.5: Reduced third order small-signal equivalent circuit of the half-bridge LLC converter reported in [182] assuming a switching frequency perturbation $\tilde{f}_{sw}$: **(a)** AC subsystem, **(b)** DC subsystem. The voltage source related to $\tilde{V}_o$ is transparent, as it can be disregarded when the output voltage dynamics are neglected (i.e., $V_o \approx \bar{V}_o$). The values of V_e, I_e, R_e, L_e and C_e are reported in [182].

Unfortunately, the third order model presented in [182] is still unsuited for a straightforward controller design, mainly due to the $L_e C_e$ resonance, the presence of two sources (i.e., V_e, I_e) and the coupling of AC and DC subsystems. Therefore a further model simplification is proposed in the following.

7.2.3 Proposed Dual 1st Order System Model

Based on the considerations reported in **Section 7.2.1**, the small-signal equivalent circuit model of [182] is here simplified further based on the following assumptions:

- the AC and DC subsystem dynamics can be considered decoupled;
- the buck-mode beat-frequency double pole dynamics can be disregarded (i.e., $C_e \approx 0$), as the imaginary pole pair is typically placed outside the region of interest for the controller design (cf. **Fig. 7.4**).

The first assumption allows to disregard the voltage source related to $\tilde{V}_o$ in **Fig. 7.5(a)**, obtaining the equivalent circuit shown in **Fig. 7.6(a)**, where the voltage source $V_e = 2\pi K_d \tilde{f}_{sw}$ and the current source $I_e = 2\pi G_d \tilde{f}_{sw}$ [182] have been multiplied by 2, due to the considered full-bridge implementation of the converter (i.e., as opposed to the original half-bridge implementation in [182]). Neglecting the beat-frequency double pole dynamics in buck-mode operation, according to the second assumption, the equivalent capacitor C_e can be disregarded, obtaining the equivalent circuit of **Fig. 7.6(b)**. By applying the Thevenin theorem to the current source, the circuit in **Fig. 7.6(c)** is derived. Since the aim of the AC

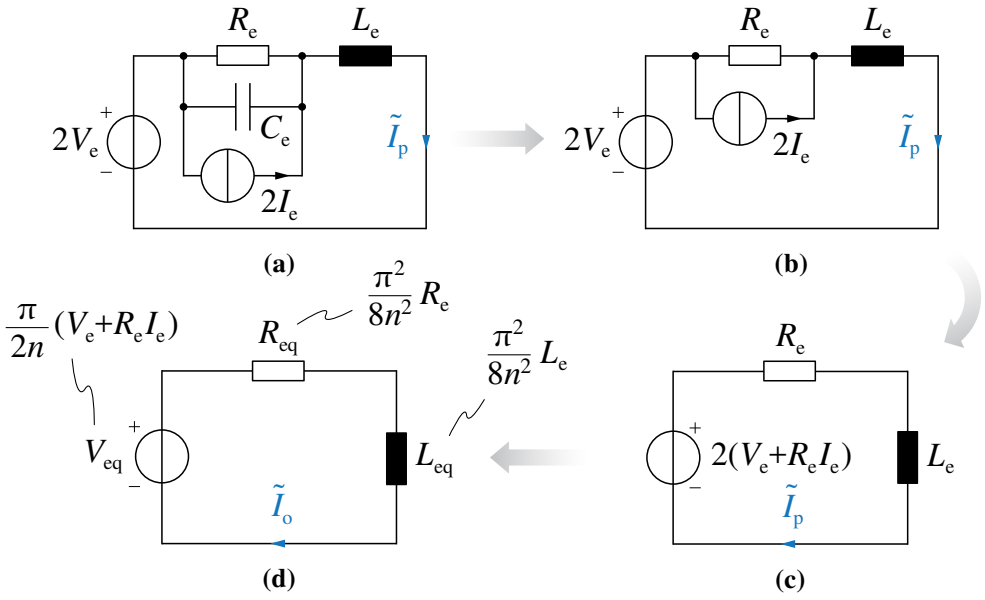


Fig. 7.6: Overview of the step-by-step simplification process from the equivalent circuit of **Fig. 7.5(a)** to the equivalent circuit of **Fig. 7.7(a)**.

subsystem model is to link the small-signal frequency perturbation $\tilde{f}_{sw}$ (i.e., contained in V_e and I_e) to the output current variation $\tilde{I}_o$, the equivalent circuit components in **Fig. 7.6(c)** must be modified according to the equivalent transformer ratio $\tilde{I}_p/\tilde{I}_o = \pi/2n$. Additionally, to obtain more compact expressions, all circuit component values are divided by 2 (i.e., leaving unaffected the relation between $\tilde{f}_{sw}$ and $\tilde{I}_o$). Therefore, the AC subsystem equivalent circuit reported in **Fig. 7.6(d)** is obtained, where

$$V_{eq} = \frac{\pi}{2n}\left(V_e + R_e I_e\right), \quad R_{eq} = \frac{\pi^2}{8n^2} R_e, \quad L_{eq} = \frac{\pi^2}{8n^2} L_e. \tag{7.21}$$

According to the performed simplifications, the LLC small-signal behavior can be represented with the two decoupled and dynamically-independent first order systems illustrated in equivalent circuit form in **Fig. 7.7**. The system small-signal state-space equations can be thus expressed as:

$$\begin{cases} \dfrac{d\tilde{I}_o}{dt} = \dfrac{1}{L_{eq}}\left(R_{eq}\tilde{I}_o + V_{eq}\right) & (7.22) \\ \dfrac{d\tilde{V}_o}{dt} = \dfrac{1}{C_o}\left(\tilde{I}_o - \dfrac{\tilde{V}_o - V_b}{R_b}\right) & (7.23) \end{cases}$$

which define the dynamical evolution of the two control state variables I_o and V_o.

While the physical meaning of the equivalent circuit parameters of the DC subsystem is straightforward, being directly related to the output filter and load, the understanding of the AC subsystem active and passive components requires further insight. Recalling the static converter voltage gain M and quality factor Q definitions (cf. **Chapter 5**)

$$M = \frac{nV_o}{V_i}, \qquad Q = \frac{\pi^2}{8n^2} Z_r \frac{I_o}{V_o}, \tag{7.24}$$

where $Z_r = \sqrt{L_r/C_r}$ is the characteristic impedance of the resonant tank, it is possible to completely identify a generic converter steady-state operating point in the inductive region (i.e., the stable region) with the sole parameter pair (M, Q).

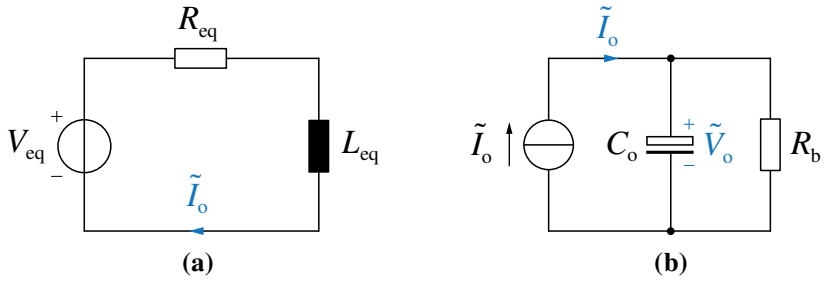


Fig. 7.7: Proposed dual first order simplified small-signal equivalent circuit of the considered full-bridge LLC converter assuming a switching frequency perturbation $\tilde{f}_{sw}$: **(a)** AC subsystem, **(b)** DC subsystem.

It is derived from [182] that the equivalent circuit voltage source V_{eq} represents the static output voltage gain variation induced by a small-signal switching frequency perturbation $\tilde{f}_{sw}$ and is expressed by

$$V_{eq} = \frac{\partial V_o}{\partial f_{sw}} \tilde{f}_{sw} = \frac{V_i}{n} \frac{\partial M}{\partial f_{sw}} \tilde{f}_{sw}, \tag{7.25}$$

It is worth noting that $\partial M/\partial f_{sw} < 0$, since an increase of the switching frequency leads to a lower static output voltage. The expression of V_{eq} has been independently confirmed at resonance in [110, 178] and is here extended to all operating conditions.

The physical meaning of R_{eq} remains the same as for R_e in [182, 184, 185], i.e., representing the overall static resonant tank impedance and linking the steady-state output current variation to the steady-state output voltage variation as

$$R_{eq} = \frac{\partial V_o/\partial f_{sw}}{\partial I_o/\partial f_{sw}} = \frac{\pi^2}{8n^2} Z_r \frac{1}{M} \frac{\partial M/\partial f_{sw}}{\partial Q/\partial f_{sw}}. \tag{7.26}$$

It can be observed from (7.25) and (7.26), that the ratio V_{eq}/R_{eq} correctly provides the static small-signal current value $\tilde{f}_{sw} \cdot \partial I_o/\partial f_{sw}$.

Finally, L_{eq} is directly obtained by multiplying the L_e expressions found in [182] by $\pi^2/8n^2$ (i.e., due to the performed equivalent circuit adjustments in **Fig. 7.6**) obtaining

$$L_{eq} = \begin{cases} \dfrac{\pi^2}{8} \dfrac{L_r}{n^2} \left[1 + \dfrac{f_r^2}{f_{sw}^2} + \dfrac{1}{\lambda} \left(1 - \dfrac{f_{sw}}{f_r} \right) \right] & f_{sw} < f_r \\ \dfrac{\pi^2}{4} \dfrac{L_r}{n^2} & f_{sw} = f_r \\ \dfrac{\pi^2}{8} \dfrac{L_r}{n^2} \left(1 + \dfrac{f_r^2}{f_{sw}^2} \right) & f_{sw} > f_r \end{cases}, \tag{7.27}$$

where $\lambda = L_r/L_m$ is the LLC inductance ratio defined in **Chapter 5**. It is observed that the expression of the equivalent inductance depends on the LLC operating mode (i.e., boost-mode, unity-gain-mode, buck-mode) and varies with the switching frequency. In particular, in boost-mode (i.e., $f_{sw} < f_r$) L_{eq} also depends on λ, as the magnetizing inductance affects the resonant tank operation during the time interval at the end of each half-cycle, when $i_r = i_m$ (cf. **Section 5.2.3**). The L_{eq} variation is illustrated in **Fig. 7.8** as function of the normalized switching frequency f_{sw}/f_r and the inductance ratio λ. Intuitively, a larger value of L_m (i.e., a lower value of λ) translates into a larger value of L_{eq}. It is worth noting that the L_{eq} expression at resonance has been also independently confirmed in [110, 178].

The simplified first order transfer function of the AC subsystem can be therefore derived from (7.22) as

$$\frac{\tilde{I}_o(s)}{\tilde{f}_{sw}(s)} = \frac{1}{\tilde{f}_{sw}} \frac{V_{eq}}{R_{eq} + s L_{eq}}. \tag{7.28}$$

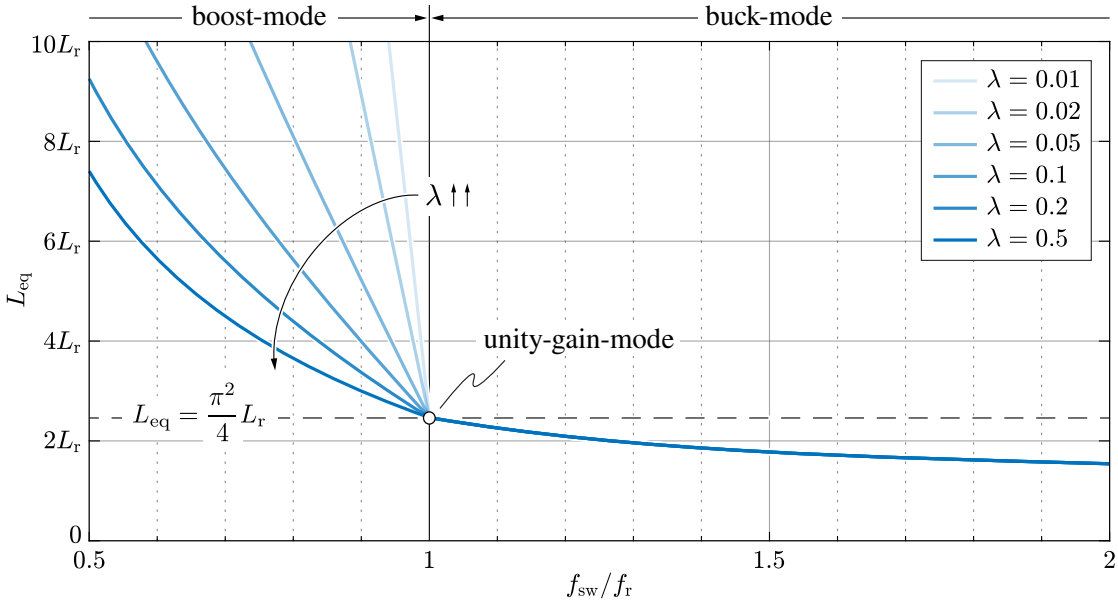


Fig. 7.8: Small-signal equivalent inductance L_{eq} as function of the normalized switching frequency f_{sw}/f_r and the inductance ratio λ, according to (7.27).

It can be observed that the small-signal steady-state gain

$$\left.\frac{\tilde{I}_o(s)}{\tilde{f}_{sw}(s)}\right|_{s\to 0} = \frac{1}{\tilde{f}_{sw}} \frac{V_{eq}}{R_{eq}} = \frac{8n^2}{\pi^2} \frac{1}{Z_r} V_o \frac{\partial Q}{\partial f_{sw}} \tag{7.29}$$

is proportional to $\partial Q/\partial f_{sw}$, whereas the dynamic (i.e., high-frequency) small-signal gain

$$\left.\frac{\tilde{I}_o(s)}{\tilde{f}_{sw}(s)}\right|_{s\to \infty} = \frac{1}{\tilde{f}_{sw}} \frac{V_{eq}}{sL_{eq}} = \frac{V_i/n}{sL_{eq}} \frac{\partial M}{\partial f_{sw}} \tag{7.30}$$

is proportional to $\partial M/\partial f_{sw}$. The static values of M and Q obtained in (5.14) and (5.20), respectively (cf. **Chapter 5**), can be expressed as functions of f_{sw}, as

$$M = \frac{1}{\sqrt{\left(1+\lambda-\lambda\frac{f_r^2}{f_{sw}^2}\right)^2 + Q^2\left(\frac{f_{sw}}{f_r}-\frac{f_r}{f_{sw}}\right)^2}}\,, \tag{7.31}$$

$$Q = \frac{\sqrt{\frac{1}{M^2} - \left(1+\lambda-\lambda\frac{f_r^2}{f_{sw}^2}\right)^2}}{\left|\frac{f_{sw}}{f_r}-\frac{f_r}{f_{sw}}\right|}\,. \tag{7.32}$$

Deriving these expressions with respect to the switching frequency, the desired derivative

values are obtained as

$$\frac{\partial M}{\partial f_{\mathrm{sw}}} = -\frac{1}{f_{\mathrm{sw}}} \frac{2\lambda \frac{f_{\mathrm{r}}^2}{f_{\mathrm{sw}}^2}\left(1+\lambda-\lambda\frac{f_{\mathrm{r}}^2}{f_{\mathrm{sw}}^2}\right)+Q^2\left(\frac{f_{\mathrm{sw}}^2}{f_{\mathrm{r}}^2}-\frac{f_{\mathrm{r}}^2}{f_{\mathrm{sw}}^2}\right)}{\left[\sqrt{\left(1+\lambda-\lambda\frac{f_{\mathrm{r}}^2}{f_{\mathrm{sw}}^2}\right)^2+Q^2\left(\frac{f_{\mathrm{sw}}}{f_{\mathrm{r}}}-\frac{f_{\mathrm{r}}}{f_{\mathrm{sw}}}\right)^2}\right]^3} \tag{7.33}$$

and

$$\frac{\partial Q}{\partial f_{\mathrm{sw}}} = -\frac{1}{f_{\mathrm{sw}}} \frac{2\lambda \frac{f_{\mathrm{r}}^2}{f_{\mathrm{sw}}^2}\left(1+\lambda-\lambda\frac{f_{\mathrm{r}}^2}{f_{\mathrm{sw}}^2}\right)+Q^2\left(\frac{f_{\mathrm{sw}}^2}{f_{\mathrm{r}}^2}-\frac{f_{\mathrm{r}}^2}{f_{\mathrm{sw}}^2}\right)}{Q\left(\frac{f_{\mathrm{sw}}}{f_{\mathrm{r}}}-\frac{f_{\mathrm{r}}}{f_{\mathrm{sw}}}\right)^2}\,. \tag{7.34}$$

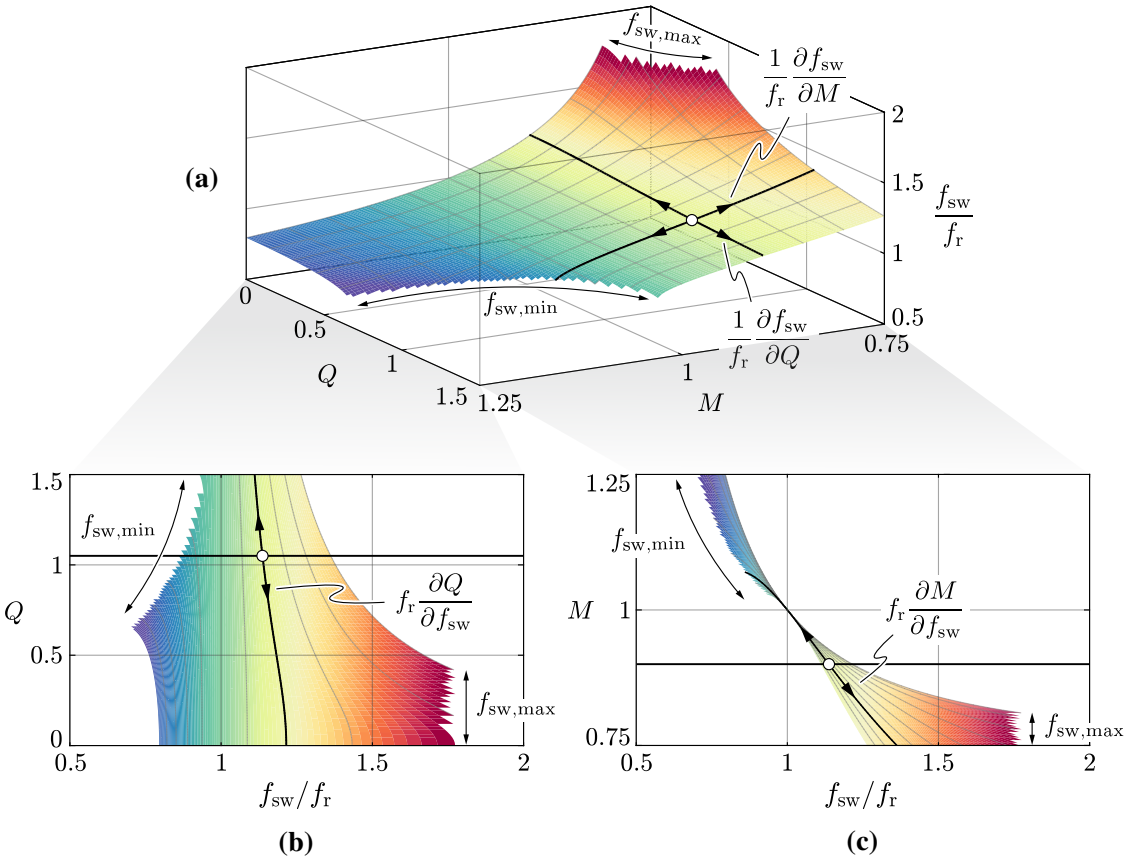


Fig. 7.9: Normalized static switching frequency $f_{\mathrm{sw}}/f_{\mathrm{r}}$ as function of the converter input/output voltage gain M and quality factor Q obtained with FHA: **(a)** 3D surface plot $f_{\mathrm{sw}}(M,Q)$, **(b)** 2D contour plot $Q(f_{\mathrm{sw}},M)$, **(c)** 2D contour plot $M(f_{\mathrm{sw}},Q)$. The system maximum and minimum switching frequency limits $f_{\mathrm{sw,min}}$, $f_{\mathrm{sw,max}}$ are indicated. The ∘ symbol indicates the considered operating point and the values of $\partial Q/\partial f_{\mathrm{sw}}$, $\partial M/\partial f_{\mathrm{sw}}$ are represented by the slope of the isolines in **(b)** and **(c)**, respectively.

The static value of $f_{sw}(M,Q)$ can be found numerically by solving either (7.31) or (7.32), and is illustrated in **Fig. 7.9**, assuming the LLC circuit parameters reported in **Chapter 6**. In particular, **Fig. 7.9(b)** and **(c)** highlight the strong system non-linearity, translating into large variations of both $\partial M/\partial f_{sw}$ and $\partial Q/\partial f_{sw}$ depending on the operating point. These variations in turn modify the small-signal system transfer function according to (7.29) and (7.30), translating into a first order system with variable gain and moving pole and posing significant control challenges.

The availability of the M and Q derivative expressions (7.33), (7.34) allows to evaluate numerically V_{eq} and R_{eq} depending on the system operating point. Therefore, the magnitude and phase trends of the simplified transfer function $\tilde{I}_o(s)/\tilde{f}_{sw}(s)$ reported in (7.28) can be compared to the ones obtained for the complete sixth order AC subsystem model (7.11)–(7.16) to assess the validity of the performed approximations. This comparison is provided in **Fig. 7.10**, where the LLC system parameters and operating limits reported in **Chapter 6** are assumed. In particular, three operating modes are considered, namely boost-mode ($M = 1.25$), unity-gain-mode ($M = 1$) and buck-mode ($M \approx 0.77$), evaluating the system transfer functions in both minimum and maximum load conditions. It is immediately observed that the simplified first order transfer functions accurately match the full order model up to high frequency values (i.e., 10–100 kHz) in all operating conditions. Notably, a very limited low-frequency error is observed also in buck-mode, even though the simplified model disregards the beat-frequency double pole. In fact, the high-frequency location of the double pole does not significantly affect the full order transfer function in the control region of interest, thus leaving unaltered the accuracy of the simplified model.

A different point of view is provided on the right side of **Fig. 7.10**, where a comparison between the two models is carried out in the time domain, assessing the open-loop system response to a reference step in buck-mode, unity-gain-mode and boost-mode (i.e., assuming $\bar{I}_o = 10\,\text{A}$). The waveforms confirm the good accuracy of the proposed simplified model, especially in unity-gain-mode (i.e., inductive behavior) and in boost-mode (i.e., first-order low-pass filter behavior). Furthermore, the time-domain response in buck-mode demonstrates that, even though the simplified model achieves a lower overall accuracy with respect to the other operating modes, it is able to correctly reproduce the low-frequency dynamics of the system (i.e., the main requirement for the design and tuning of the closed-loop control).

Case Study – Operation at Resonance

The LLC converter operation in unity-gain-mode (i.e., $f_{sw} = f_r$) is characterized by $M = 1$ independently of the converter load (cf. **Section 5.2.1**). In particular, the reduced first

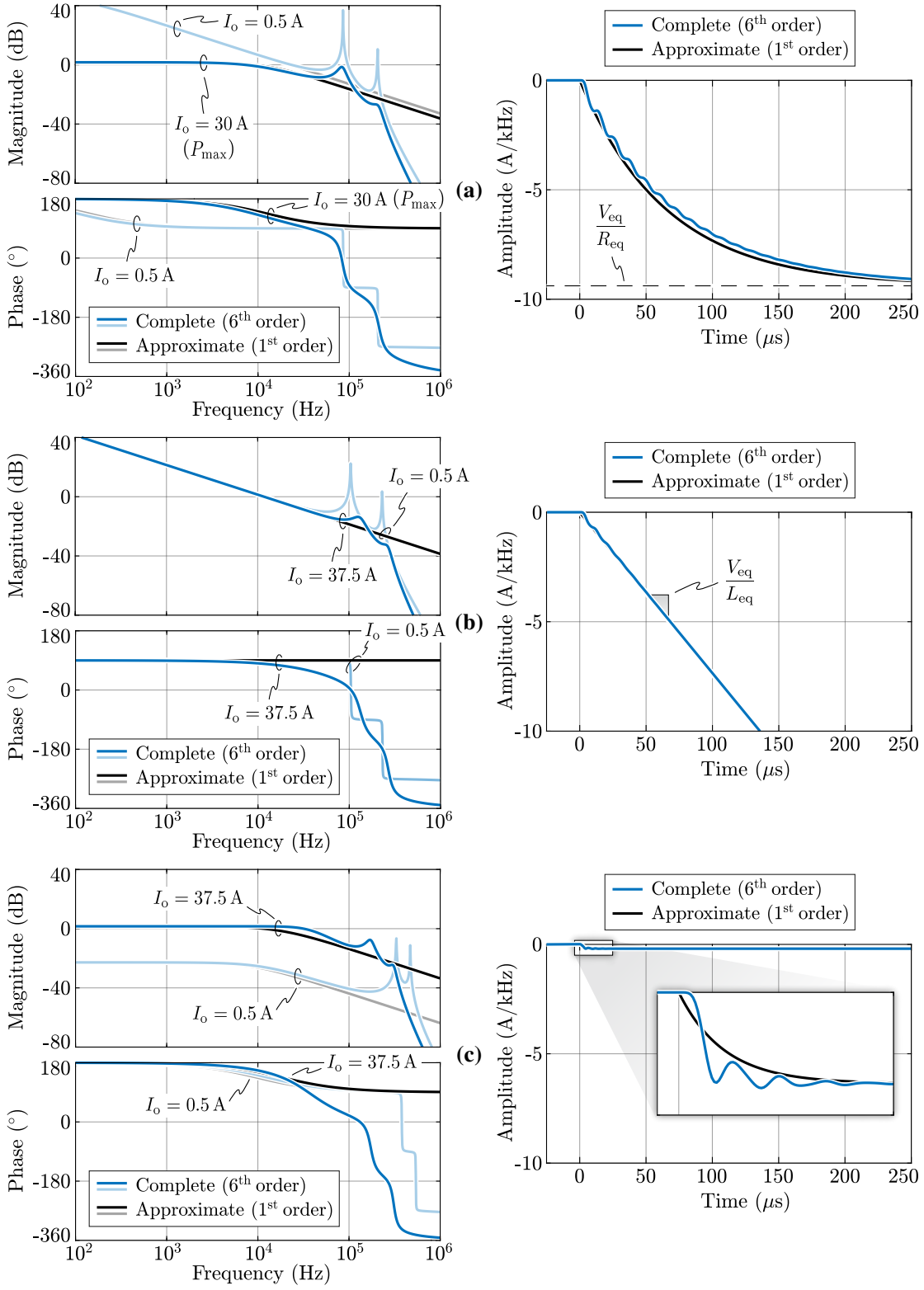


Fig. 7.10: Small-signal transfer function and open-loop step response of $\tilde{I}_o(s)/\tilde{f}_{sw}(s)$, comparing the full sixth order model (cf. **Fig. 7.3(a)–(b)**) to the proposed simplified first order model (cf. **Fig. 7.7(a)**): **(a)** boost-mode operation ($V_i = 400\,V$, $V_o = 500\,V$, i.e. $M = 1.25$), **(b)** unity-gain-mode operation ($V_i = V_o = 325\,V$, i.e. $M = 1$) and **(c)** buck-mode operation ($V_i = 325\,V$, $V_o = 250\,V$, i.e. $M \approx 0.77$). The system parameters and limits reported in **Chapter 6** are considered. The transfer functions are reported both in minimum and maximum load conditions, whereas an output current step of 10 A is considered for the time-domain response.

order small-signal model (7.28) is simplified further, as $R_{eq} = 0$ and thus

$$\left.\frac{\partial M}{\partial f_{sw}}\right|_{f_{sw}=f_r} = -\frac{2\lambda}{f_r}, \quad \left.\frac{\partial Q}{\partial f_{sw}}\right|_{f_{sw}=f_r} = -\infty. \tag{7.35}$$

Therefore, the expression of V_{eq} becomes

$$V_{eq}\big|_{f_{sw}=f_r} = -\frac{2\lambda}{f_r}\frac{V_i}{n}\tilde{f}_{sw}, \tag{7.36}$$

differently from what previously reported in [110, 178].

Therefore, a significant circuit simplification is obtained, as the system behavior becomes load-independent, the dominant pole moves to the origin of the root locus and the resonant tank behaves as an equivalent inductor.

7.3 Controller Design

In this section, the adopted cascaded digital dual-loop control scheme is described, consisting of an outer voltage control loop (V_o) and an inner current control loop (I_o), as schematically illustrated in **Fig. 7.11**. The I_o control loop aims to provide tight output current regulation by acting on the switching frequency of the input bridge. The V_o control loop, instead, only plays an active role during start-up and constant-voltage battery charging (i.e., at the very end of the charging process), as the voltage reference is always set to the fully-charged maximum battery voltage value $V_{b,max}$, which is provided by the vehicle itself. During most of the time, the output of the voltage regulator is saturated to the

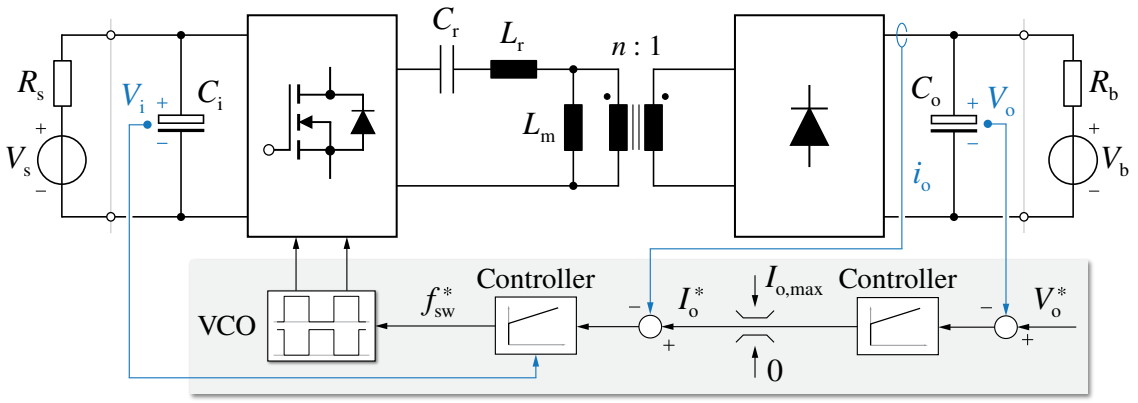


Fig. 7.11: Simplified control diagram of the LLC converter, including the output current I_o and output voltage V_o controllers. Detailed schematics of the control loops are provided in **Fig. 7.12** and **Fig. 7.15**, respectively. The voltage controlled oscillator (VCO) is implemented by digital means.

maximum charging current value $I_{o,max}$, either limited by the vehicle battery management system (BMS) or by the converter current/power boundaries. As a consequence, the voltage control dynamics are not of primary importance in the present application. Nevertheless, for reasons of completeness, a design and tuning procedure for both I_o and V_o controllers is provided in this section.

7.3.1 Output Current Control Loop

The proposed output current control scheme is illustrated in **Fig. 7.12**. The current is measured at the output of the diode bridge (i.e., as a rectified sine wave) and is passed through a second-order filter with a 25 kHz corner frequency $f_{f,i}$ to obtain its average value I_o. Overall, the control loop consists of the filter applied to the current measurement, a proportional-integral (PI) regulator, two gain adaptation blocks and a feedforward contribution obtained with a single LUT, a minimum/maximum frequency saturation block, a delay deriving from the digital control implementation and the plant itself (i.e., the frequency-to-current transfer function).

The transfer function of the second-order filter applied to the current measurement has the following expression:

$$G_{f,i}(s) = \frac{\omega_{f,i}^2}{(s+\omega_{f,i})^2}, \tag{7.37}$$

where $\omega_{f,i} = 2\pi f_{f,i}$ is the filter corner frequency.

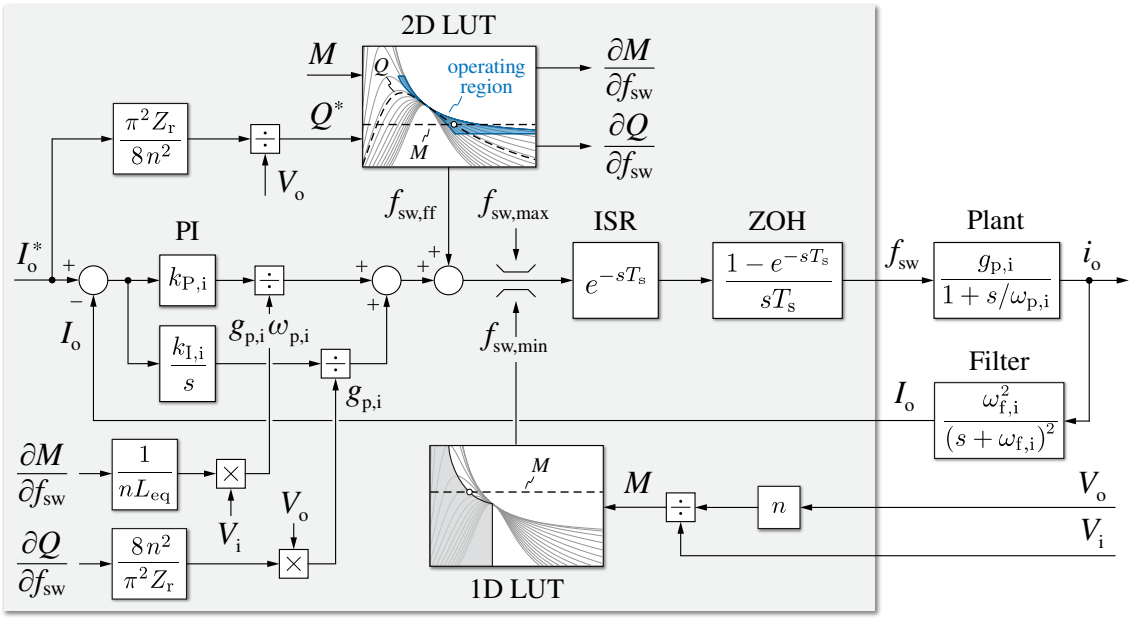


Fig. 7.12: Detailed block diagram of the I_o current control loop.

The digital sampling and update processes are performed at a constant frequency $f_s = 1/T_s$ (i.e., the sampling or control frequency). To accurately tune the current control loop performance, the system delays introduced by the digital controller implementation must be taken into account, as each delay reduces the achievable control bandwidth and/or decreases the closed-loop stability margin [116, 117]. The first delay component is directly related to the digital interrupt service routine (ISR), which introduces a one sampling period delay T_s between input and output signals. The second component is linked to the ZOH effect of one sampling period T_s introduced by the digital update process of the output switching frequency. Even though the ZOH does not result in a pure delay effect (i.e., as it affects also the system gain), if the control bandwidth is sufficiently lower than the Nyquist frequency it can be considered as an ideal $T_s/2$ delay. Therefore, the total delay introduced by the digital control implementation is $T_d = 3T_s/2$, which can be approximated with a rational Padè transfer function

$$G_{d,i}(s) = e^{-s\,3\,T_s/2} \approx \frac{1 - s\,3\,T_s/4}{1 + s\,3\,T_s/4}. \tag{7.38}$$

The linearized plant transfer function, linking a small-signal switching frequency perturbation $\tilde{f}_{sw}$ to the resulting output current $\tilde{I}_o$, has been derived in **Section 7.2** and has been simplified to a first-order transfer function in (7.28). The small-signal steady-state gain is obtained by setting $s = 0$ into (7.28), as

$$g_{p,i} = \frac{1}{\tilde{f}_{sw}} \frac{V_{eq}}{R_{eq}} = \frac{8n^2}{\pi^2} \frac{1}{Z_r} V_o \frac{\partial Q}{\partial f_{sw}}, \tag{7.39}$$

whereas the pole frequency is directly derived from the denominator of (7.28), as

$$\omega_{p,i} = \frac{R_{eq}}{L_{eq}} = \frac{\pi^2}{8n^2} Z_r \frac{1}{M} \frac{\partial M/\partial f_{sw}}{\partial Q/\partial f_{sw}} \frac{1}{L_{eq}}. \tag{7.40}$$

Therefore, the simplified plant transfer function can be expressed as

$$G_{p,i}(s) = \frac{\tilde{I}_o(s)}{\tilde{f}_{sw}(s)} \approx \frac{g_{p,i}}{1 + s/\omega_{p,i}}. \tag{7.41}$$

Expression (7.41) shows that the system approximately behaves as a first-order low-pass filter with both a variable steady-state gain and a moving pole, as both $g_{p,i}$ and $\omega_{p,i}$ vary considerably with the operating point (cf. **Fig. 7.13**). For instance, at resonance (i.e., $f_{sw} = f_r$, $M = 1$) the ideal system behaves as a pure integrator, being $\partial Q/\partial f_{sw} \approx -\infty$. In fact, the pole frequency $\omega_{p,i}$ moves to zero and an infinite steady-state gain $g_{p,i}$ is obtained. Notably, the large variation of the system gain and pole location during normal operation is a critical aspect of the LLC converter and must be taken into account within the current controller design.

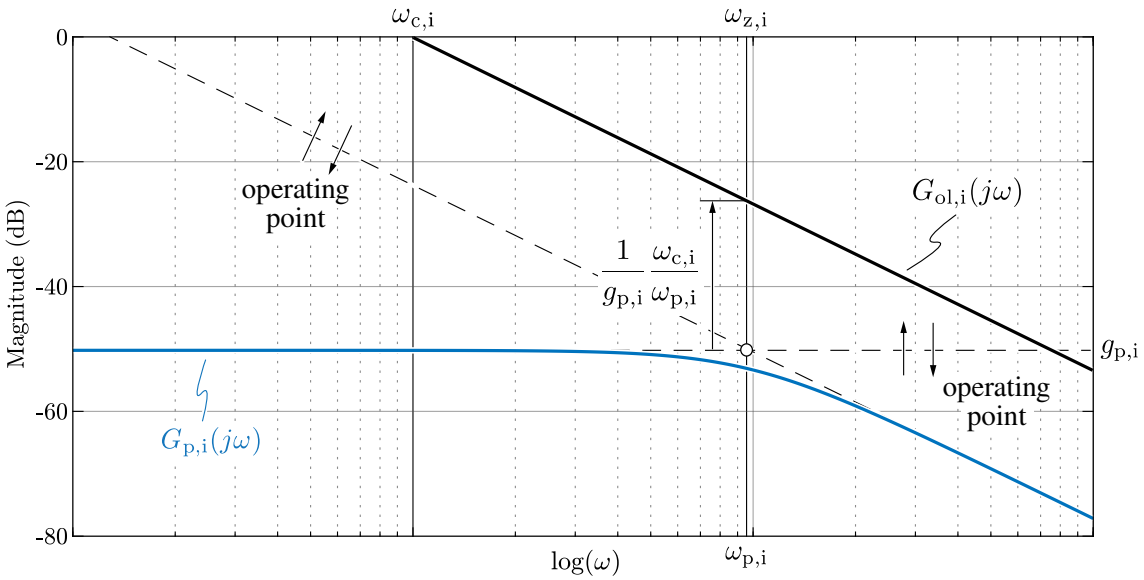


Fig. 7.13: Qualitative representation of the simplified first order plant transfer function $G_{p,i}(j\omega) = \tilde{I}_o(j\omega)/\tilde{f}_{sw}(j\omega)$, highlighting the variable gain $g_{p,i}$ and moving pole $\omega_{p,i}$. The target constant open-loop control transfer function $G_{ol,i}(j\omega)$ is also indicated.

Since the plant shows an integral behavior only at resonance, a PI regulator is selected to ensure a zero steady-state tracking error in all operating conditions and improved disturbance rejection capabilities with respect to a simple proportional regulator. To counteract the system gain/pole movement and ensure constant control bandwidth, the same approach proposed in [115] is adopted: the values of $g_{p,i}$ and $\omega_{p,i}$ are calculated in real-time and a controller gain adaptation is performed. In particular, the output of the proportional regulator is divided by the moving pole frequency $\omega_{p,i}$, while the overall PI output is divided by the variable steady-state gain $g_{p,i}$, obtaining the following controller transfer function:

$$G_{c,i}(s) = \frac{1}{g_{p,i}}\left(\frac{1}{\omega_{p,i}}k_{P,i} + \frac{k_{I,i}}{s}\right), \tag{7.42}$$

where $k_{P,i}$ and $k_{I,i}$ are the proportional and integral regulator coefficients, respectively. Being the system open-loop transfer function defined as

$$G_{ol,i}(s) = G_{f,i}(s)\,G_{c,i}(s)\,G_{d,i}(s)\,G_{p,i}(s), \tag{7.43}$$

the following expression is obtained substituting (7.41) and (7.42) into (7.43):

$$G_{ol,i}(s) = k_{P,i}\,\frac{s + \omega_{p,i}\,k_{I,i}/k_{P,i}}{s\,(s+\omega_{p,i})}\,G_{f,i}(s)\,G_{d,i}(s). \tag{7.44}$$

To compensate the plant pole $\omega_{\mathrm{p,i}}$ with the controller zero (i.e., $\omega_{\mathrm{z,i}} = \omega_{\mathrm{p,i}} k_{\mathrm{I,i}}/k_{\mathrm{P,i}}$), the ratio $k_{\mathrm{I,i}}/k_{\mathrm{P,i}}$ is set to 1, leading to a plant-independent open-loop transfer function expression:

$$G_{\mathrm{ol,i}}(s) = \frac{k_{\mathrm{P,i}}}{s} \frac{\omega_{\mathrm{f,i}}^2}{(s+\omega_{\mathrm{f,i}})^2} \frac{1 - s\,3\,T_{\mathrm{s}}/4}{1 + s\,3\,T_{\mathrm{s}}/4}. \tag{7.45}$$

Therefore, the controller coefficients $k_{\mathrm{P,i}}$ and $k_{\mathrm{I,i}}$ can be easily set to achieve the desired value of open-loop 0 dB cross-over frequency $\omega_{\mathrm{c,i}}$. In particular, assuming $\omega_{\mathrm{c,i}} \ll \omega_{\mathrm{f,i}}$ and solving $|G_{\mathrm{ol,i}}(j\omega_{\mathrm{c,i}})| = 1$, the following coefficients are obtained:

$$\begin{cases} k_{\mathrm{P,i}} \approx \omega_{\mathrm{c,i}} \\ k_{\mathrm{I,i}} \approx \omega_{\mathrm{c,i}} \end{cases}. \tag{7.46}$$

Notably, $k_{\mathrm{P,i}} = k_{\mathrm{I,i}}$ since the gain adaptation process extracts the variable terms $g_{\mathrm{p,i}}$ and $\omega_{\mathrm{p,i}}$ from the proportional and integral coefficients, as shown in (7.42).

Since the open-loop transfer function has been expressed in rational form in (7.45), the tuning of $\omega_{\mathrm{c,i}}$ can be performed in the continuous time domain employing conventional techniques. In the present work, a phase margin tuning criterion is adopted, therefore $\omega_{\mathrm{c,i}}$ is expressed as function of the desired phase margin in radians m_φ by solving $\angle G_{\mathrm{ol,i}}(j\omega_{\mathrm{c,i}}) = -\pi + m_\varphi$ and assuming $\omega_{\mathrm{c,i}} \ll \omega_{\mathrm{f,i}}$, as

$$\omega_{\mathrm{c,i}} \approx \frac{1}{T_{\mathrm{s}}} \left[-\tan(m_\varphi) + \sqrt{1 + \tan^2(m_\varphi)} \right]. \tag{7.47}$$

In the following, $m_\varphi = 60^\circ$ is considered, ensuring both fast reference step response and enhanced disturbance rejection capability. For the system at hand (i.e., with $f_{\mathrm{f,i}} = 25\,\mathrm{kHz}$, $f_{\mathrm{s}} = 20\,\mathrm{kHz}$, $T_{\mathrm{s}} = 50\,\mu\mathrm{s}$, cf. **Section 7.5**), an open-loop cross-over frequency $f_{\mathrm{c,i}} \approx 1.1\,\mathrm{kHz}$ is obtained.

A key feature of the proposed control scheme in **Fig. 7.12** is the inclusion of a feedforward contribution, namely the steady-state switching frequency in the desired operating conditions. This feature essentially allows to unburden the integral part of the PI regulator, counteract the non-linear nature of the system, and ensure the small-signal operation of the controller. Additionally, the feedforward term allows to instantaneously compensate the dynamical output voltage variations, effectively decoupling the small-signal AC and DC subsystems (cf. **Section 7.2**) and thus eliminating the impact of the resonance between L_{eq} and C_{o} on the current control phase margin. The steady-state f_{sw} values, obtained as functions of the operating voltage gain M and quality factor Q, are stored in a LUT and the desired feedforward value is extracted by linear interpolation (cf. **Appendix 7.B**). The exploitation of M and Q allows to normalize the converter operating conditions and

uniquely identify a working point in the inductive region (i.e., the stable region) with only two parameters, thus requiring a simple two-dimensional (2D) LUT. In essence, the feedforward f_{sw} contribution serves the purpose of unloading the PI regulator from the major frequency steps, leaving to the regulator the tasks of counteracting the dynamical perturbations around equilibrium and addressing the LUT steady-state error. Furthermore, the LUT inherently stores the information regarding $\partial M/\partial f_{\mathrm{sw}}$ and $\partial Q/\partial f_{\mathrm{sw}}$ (cf. **Appendix 7.B**), which are both required for the controller gain adaptation in (7.39) and (7.40), in case the analytical FHA expressions (7.33) and (7.34) are not used.

The simplest way to extract the $f_{\mathrm{sw}}(M,Q)$ LUT is by numerically inverting the FHA gain expression (7.31), however yielding approximate and inaccurate results. Better methods, ensuring increasing accuracy at the expense of a higher realization effort, consist in solving a time-domain analysis (TDA) of the system operating modes (cf. **Chapter 5**), carrying out an extensive set of circuit simulations, or characterizing the real converter prototype with experimental measurements. In particular, the TDA method yields the exact same results as the extensive circuit simulations, however requiring far lower computational effort and time [159]. A comparison of the LUTs obtained with FHA, TDA and experimental characterization is provided in **Fig. 7.14**, assuming the converter specifications reported in **Table 6.1** and **Table 6.2** (cf. **Chapter 6**). For reasons of completeness, the minimum switching frequency limit $f_{\mathrm{sw,min}}(M)$ and maximum switching frequency limit $f_{\mathrm{sw,max}} = 250\,\mathrm{kHz}$ are superimposed to graphically identify the feasible operating region of the converter. While for FHA and TDA the value of $f_{\mathrm{sw,min}}(M)$ is determined as the boundary frequency between inductive and capacitive regions, in the experimental characterization $f_{\mathrm{sw,min}}(M)$ is determined either by the converter maximum output current $I_{\mathrm{o,max}} = 37.5\,\mathrm{A}$ (for $M \leq 1$ and $V_{\mathrm{i}} \leq 400\,\mathrm{V}$) or by the converter maximum output power rating $P_{\mathrm{o,max}} = 15\,\mathrm{kW}$ (for $M > 1$ and $V_{\mathrm{i}} = 400\,\mathrm{V}$), as explained in **Section 7.5**. It can be observed that the FHA method yields a wider operating frequency range with respect to TDA for the same (M,Q) values, as anticipated in **Chapter 5**. Moreover, the behavior at low quality factors is extremely different between the two, as only the TDA method correctly predicts the necessary frequency increase at light load: for instance, with the FHA method the steady-state switching frequency for $M = 1$ is equal to f_{r} and is load independent, which is not the case for TDA. Therefore, since the TDA method is characterized by better accuracy and only requires a slightly higher computational effort compared to FHA, it is the preferred choice for the LUT extraction when an experimental characterization of the converter is not available. Nevertheless, if a complete characterization of the converter is performed (cf. **Section 7.5.1**), the highest accuracy is obtained. Comparing **Fig. 7.14(c)** with **Fig. 7.14(b)**, a significant difference between the iso-frequency curve slopes is observed, translating into a larger frequency variation for a given M value in experimental

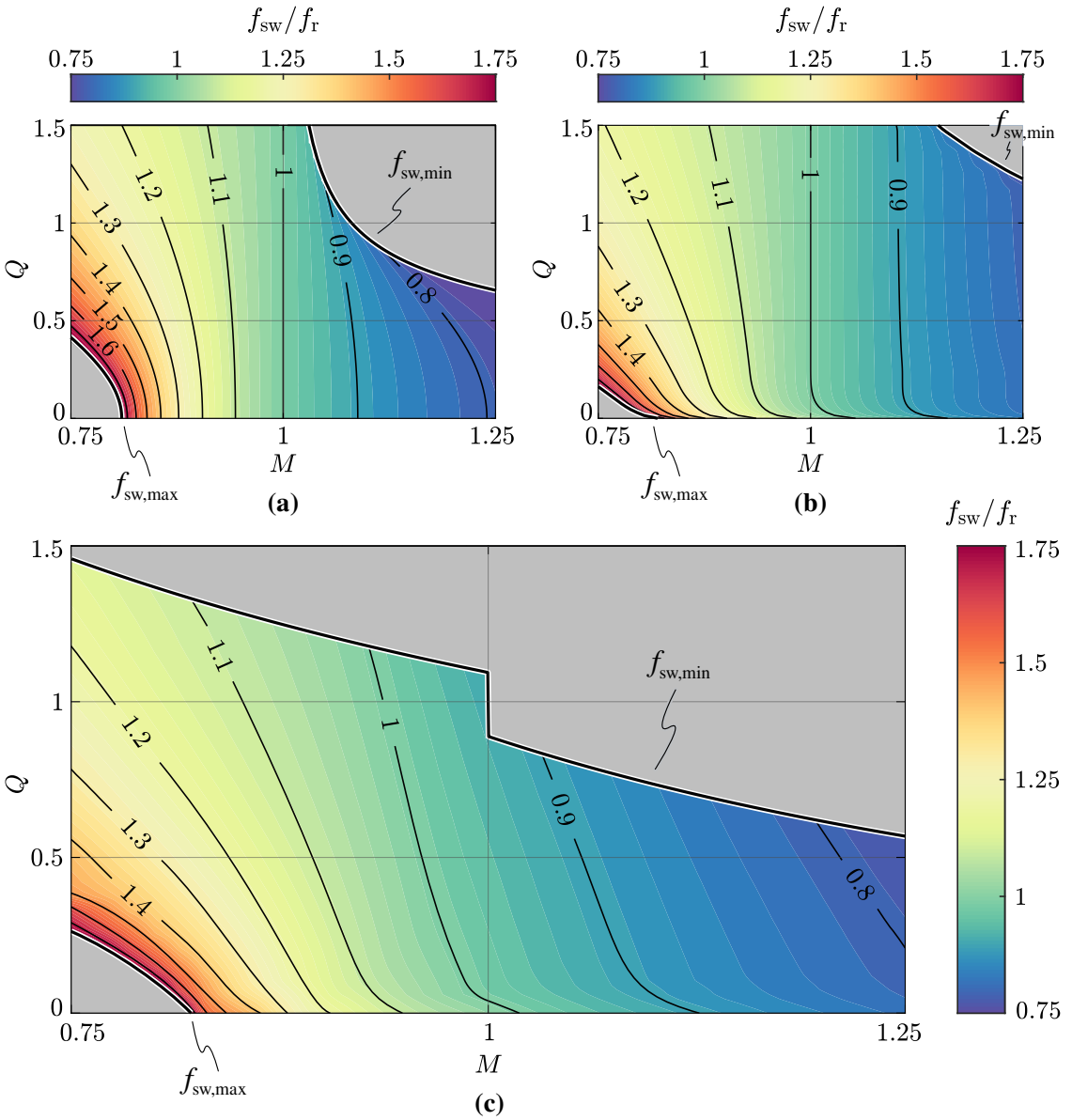


Fig. 7.14: 101x101 steady-state switching frequency $f_{sw}(M,Q)$ LUTs (i.e., normalized with respect to f_r) extracted with **(a)** first harmonic approximation (FHA), **(b)** time domain analysis (TDA) and **(c)** experimental characterization (cf. **Section 7.5.1**). The minimum frequency $f_{sw,min}$ and maximum frequency $f_{sw,max}$ limits are indicated.

practice. Other than component non-idealities and tolerances, the main reason behind this discrepancy can be attributed to the converter losses [186], mostly generated by the semiconductor devices, the resonant inductor/s, the resonant capacitor/s and the transformer/s. These losses increase significantly with the converter load and thus require a lower value of switching frequency (i.e., a higher voltage boosting) to get compensated. Furthermore, the converter losses largely reduce the value of $\partial Q/\partial f_{sw}$ around the unity voltage gain region, limiting the plant gain/pole variation and greatly decreasing the sensitivity of the

control system with respect to the LUT discretization. Overall, only the LUT obtained by experimental characterization of the converter can provide sufficient accuracy for the proposed high-performance control strategy, as it provides the real converter steady-state switching frequency in the feedforward path and addresses the FHA and TDA small-signal gain/pole modeling errors by providing the experimental values of $\partial M/\partial f_{\mathrm{sw}}$ and $\partial Q/\partial f_{\mathrm{sw}}$ for a correct controller gain adaptation.

Finally, as illustrated in **Fig. 7.12**, a switching frequency saturation block (with integrated anti-windup scheme) must be present in the forward control path, to ensure that the converter operation remains inside the minimum and maximum frequency design boundaries. As previously mentioned, the minimum switching frequency limit is a function of the voltage gain M, therefore $f_{\mathrm{sw,min}}(M)$ is also stored in a one-dimensional (1D) LUT (cf. **Section 7.5.1**).

7.3.2 Output Voltage Control Loop

The output voltage V_{o} controller is responsible for adjusting the output current I_{o} to regulate the voltage across the output filter capacitor C_{o}. The main requirements for this controller are zero steady-state error and sufficient dynamical performance to properly reject system disturbances (e.g., the battery current, if not fed forward).

The complete output voltage control schematic is illustrated in **Fig. 7.15** and consists of a PI regulator, an optional feedforward contribution, a maximum current saturation block, the output current control loop and the plant itself.

The plant transfer function is obtained from (7.23) considering the battery voltage V_{b} as a disturbance component:

$$G_{\mathrm{p,v}}(s) = \frac{\tilde{V}_{\mathrm{o}}(s)}{\tilde{I}_{\mathrm{o}}(s)} = \frac{R_{\mathrm{b}}}{1 + sR_{\mathrm{b}}C_{\mathrm{o}}}. \tag{7.48}$$

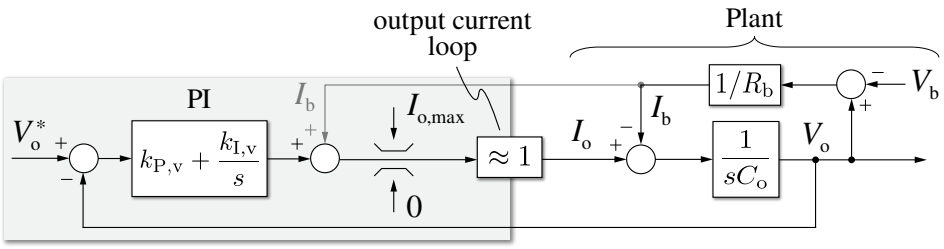


Fig. 7.15: Detailed block diagram of the V_{o} voltage control loop.

Since the measurement of the battery current I_b is normally available, its value can be fed forward. In such case, the compensated plant behaves as a pure integrator:

$$G_{\mathrm{p,v}}(s) \approx \frac{1}{sC_\mathrm{o}}. \tag{7.49}$$

Nevertheless, a PI regulator is selected to improve the controller dynamical performance and to ensure zero steady-state error when I_b is not known and cannot be fed forward:

$$G_{\mathrm{c,v}}(s) = k_{\mathrm{P,v}} + \frac{k_{\mathrm{I,v}}}{s}. \tag{7.50}$$

The output of the regulator is then saturated between 0 and $I_{\mathrm{o,max}}$ (i.e., either limited by the vehicle BMS or by the converter current/power boundaries) with an anti-windup scheme, thus becoming the reference for the inner current control loop. Since this loop is characterized by much faster dynamics with respect to the voltage control one, the current loop can be considered as an ideal actuator (i.e., a unity gain block). Therefore, the V_o control open-loop transfer function can be expressed as

$$G_{\mathrm{ol,v}}(s) = G_{\mathrm{c,v}}(s)\, G_{\mathrm{p,v}}(s). \tag{7.51}$$

If the open-loop 0 dB cross-over frequency $\omega_{\mathrm{c,v}}$ is set sufficiently below the current control loop one $\omega_{\mathrm{c,i}}$, the dynamics of the two loops do not interfere with each other. Therefore, $\omega_{\mathrm{c,v}}$ is set to $\omega_{\mathrm{c,i}}/10$, resulting in the present case in an open-loop cross-over frequency $f_{\mathrm{c,v}} \approx 110\,\mathrm{Hz}$. Therefore, the PI coefficients can be obtained substituting (7.49)–(7.50) into (7.51) and setting $|G_{\mathrm{ol,v}}(j\omega_{\mathrm{c,v}})| = 1$, leading to simple tuning expressions:

$$\begin{cases} k_{\mathrm{P,v}} = \omega_{\mathrm{c,v}} C_\mathrm{o} \\ k_{\mathrm{I,v}} = \omega_{\mathrm{z,v}}\, k_{\mathrm{P,v}} \end{cases}, \tag{7.52}$$

where the PI zero $\omega_{\mathrm{z,v}} = k_{\mathrm{I,v}}/k_{\mathrm{P,v}}$ is set to $\omega_{\mathrm{c,v}}/5$ in order to improve the closed-loop disturbance rejection capabilities.

7.4 Simulation Results

The converter small-signal behavior is verified in circuit simulation, where the proposed control strategy is implemented by means of a custom C-code script in PLECS environment. To accurately simulate the discretized nature of the digital system, the control execution is

triggered once every control period $T_s = 50\,\mu s$ (i.e., $f_s = 20\,kHz$), while the control outputs are updated at the following trigger instant.

It is worth noting that the output voltage v_o control loop is not verified here, since achieving high voltage control dynamics is not of primary importance in battery charging applications, as the voltage control loop actively operates only during start-up and constant-voltage (CV) battery charging. Furthermore, the V_o control loop structure is well known and does not feature fundamental differences with respect to conventional solutions employed in battery chargers, such as [115].

To verify the tuning and performance consistency of the output current I_o controller, both the open-loop transfer function $G_{ol,i}$ and the closed-loop transfer function $G_{cl,i}$ are investigated in different operating conditions, namely boost-mode, unity-gain-mode and buck-mode. In particular, the LUT extracted with TDA in **Fig. 7.14(b)** is employed, as it accurately represents the ideal LLC converter operation implemented in circuit simulation (i.e., without resistive terms). Moreover, to independently assess the small-signal response of the designed control loop, the feedforward contribution $f_{sw,ff}$ is disabled. Several simulations are performed by setting sinusoidal references with different frequencies at the control input, measuring the system response and calculating its magnitude and phase. A DC offset is added to the I_o reference, in order to comply with the unidirectional nature of the LLC converter.

The results of this analysis are illustrated in **Fig. 7.16**, **Fig. 7.17** and **Fig. 7.18** for boost-mode ($M = 1.25$), unity-gain-mode ($M = 1$) and buck-mode ($M \approx 0.77$), respectively. Although the simulations have been performed for different values of quality factor Q, the small-signal transfer functions are indistinguishable in the considered frequency range. The circuit simulation results are compared to their simplified analytical counterparts derived in **Section 7.3.1**, i.e. considering the first-order plant approximation in (7.41) and the FHA-based expressions of $\partial M/\partial f_{sw}$ and $\partial Q/\partial f_{sw}$ in (7.33) and (7.34), respectively. It is observed that the simplified analytical models show a high-level of correspondence with circuit simulations over the full control frequency range, demonstrating the validity and accuracy of the proposed controller design/tuning procedure. Furthermore, **Fig. 7.16**–**Fig. 7.18** highlight the consistency of the open-loop cross-over frequency and phase margin with variable voltage gain M and quality factor Q, verifying the fundamental role of the proposed controller gain adaptation process in ensuring approximately constant control performance. It can be observed that a $-3\,dB$ closed-loop control bandwidth $f_{bw,\text{-}3dB} \approx 2\text{–}3\,kHz$ is obtained in all operating conditions.

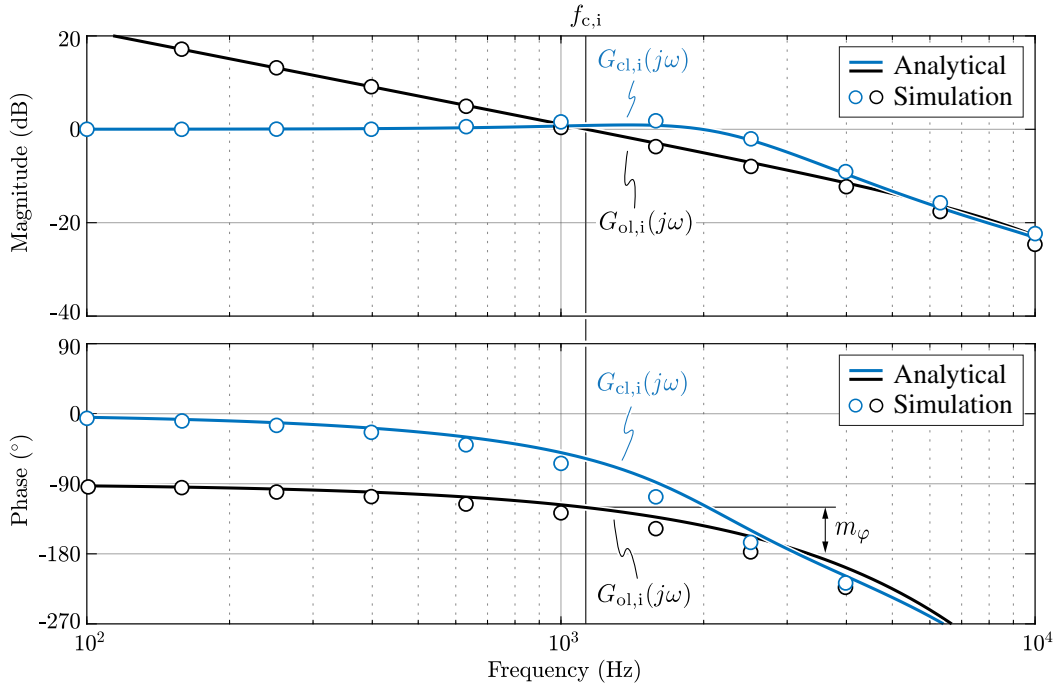


Fig. 7.16: Comparison between analytically derived and simulated output current control open-loop transfer function $G_{ol,i}$ and closed-loop transfer function $G_{cl,i}$ in boost-mode (i.e., $V_i = 400\,V$, $V_o = 500\,V$, $M = 1.25$). Thanks to the proposed gain adaptation of the controller, no visible influence of Q (i.e., I_o) on either analytical or simulated results is observed in the considered frequency range, therefore the results are only reported for $\bar{I}_o = 20\,A$.

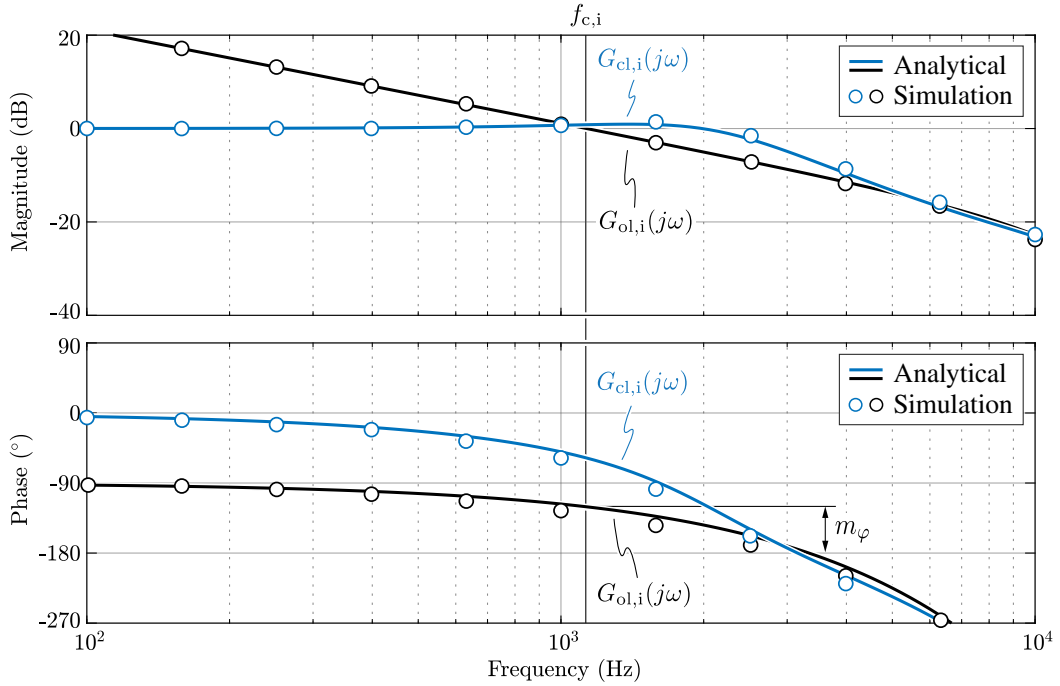


Fig. 7.17: Comparison between analytically derived and simulated output current control open-loop transfer function $G_{ol,i}$ and closed-loop transfer function $G_{cl,i}$ in unity-gain-mode (i.e., $V_i = V_o = 325\,V$, $M = 1$). Thanks to the proposed gain adaptation of the controller, no visible influence of Q (i.e., I_o) on either analytical or simulated results is observed in the considered frequency range, therefore the results are only reported for $\bar{I}_o = 20\,A$.

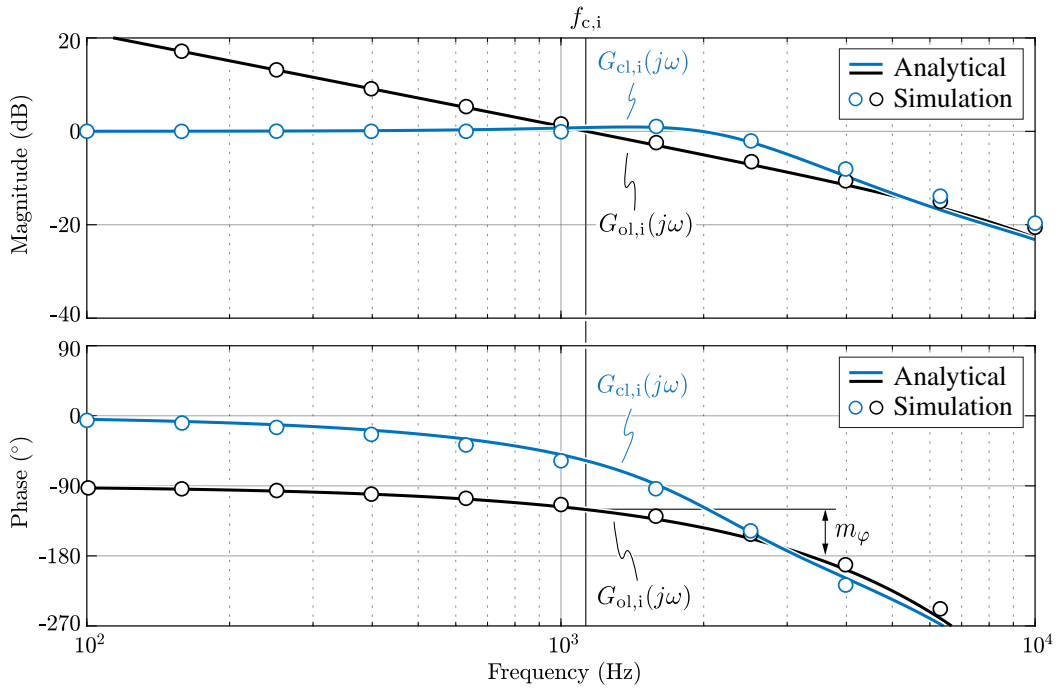


Fig. 7.18: Comparison between analytically derived and simulated output current control open-loop transfer function $G_{ol,i}$ and closed-loop transfer function $G_{cl,i}$ in buck-mode (i.e., $V_i = 325\,V$, $V_o = 250\,V$, $M \approx 0.77$). Thanks to the proposed gain adaptation of the controller, no visible influence of Q (i.e., I_o) on either analytical or simulated results is observed in the considered frequency range, therefore the results are only reported for $\bar{I}_o = 20\,A$.

7.5 Experimental Results

The output current controller design procedure described in **Section 7.3.1** is here validated on the 15 kW LLC converter prototype shown in **Fig. 6.24**. Even though the circuit structure of this converter is unconventional, due to the adoption of four series/parallel resonant inductors and two pairs of input-parallel/output-series transformers (cf. **Chapter 6**), from the control perspective the prototype is equivalent to a traditional LLC converter with the specifications and operating region reported in **Table 6.1** and **Table 6.2**. In particular, the input voltage of the LLC converter is adjusted during operation by the AC/DC stage in order to maximize the LLC operation around resonance (i.e., $f_{sw} \approx f_r$), being the highest efficiency point. **Fig. 7.19** summarizes the LLC operating conditions and highlights the converter limits in terms of output current $I_{o,max}$ and quality factor Q_{max}, which directly affect the feasible region of the LUT reported in **Fig. 7.14(c)**.

The converter closed-loop control is implemented on a STM32G474VE microcontroller unit (MCU) from ST Microelectronics, with an ISR running at $f_s = 20\,kHz$ to ensure sufficient calculation time for the dual-loop control. The corner frequency of the second

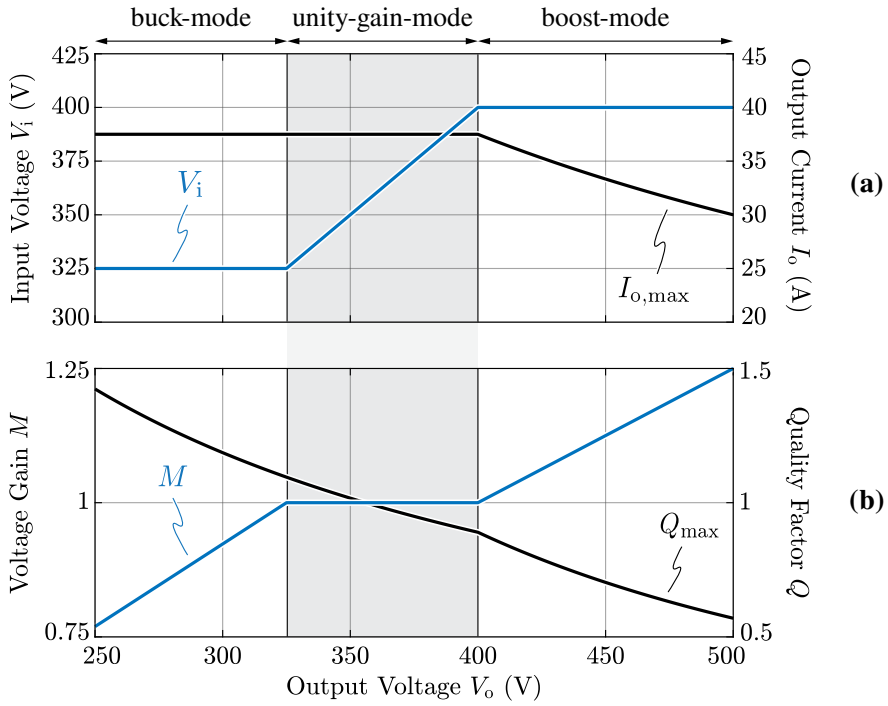


Fig. 7.19: Graphical representation of the LLC operating conditions and limits as functions of the output voltage V_o. **(a)** input voltage V_i and maximum output current $I_{o,max}$ (i.e., $I_{o,max} = 37.5\,A$ for $V_o \leq 400\,V$, $I_{o,max} = P_{o,max}/V_o$ for $V_o > 400\,V$), **(b)** voltage gain M and maximum quality factor Q_{max}. The interval where the AC/DC stage adjusts $V_i = V_o$ to maximize the LLC operation around resonance is highlighted in grey.

order filter applied to i_o is placed at $f_{f,i} = 25\,kHz$, providing the necessary attenuation at the minimum switching frequency and negligible phase delay in the control loop feedback (i.e., $f_{f,i} \gg f_{c,i} \approx 1.1\,kHz$). The 101x101 $f_{sw}(M,Q)$ 2D LUT reported in **Fig. 7.14(c)** and the 101x1 $f_{sw,min}(M)$ 1D LUT are stored on the MCU internal memory (i.e., 32 bit floating-point numbers, requiring a total of 41.2 kB of memory), allowing fast access to the data during the interpolation process. The PWM signals are generated by a sawtooth counter realized with a high-resolution timer unit. The MCU clock frequency is 170 MHz and the timer unit internal clock can be sped up 16 times, yielding a PWM resolution of 368 ps. As highlighted in the timing diagram of **Fig. 7.20**, whenever f_{sw} is not an integer multiple of f_s, the PWM frequency is updated in correspondence of the counter roll-over following the start of the ISR. This solution ensures that the generated PWM signal maintains 50 % duty-cycle when transitioning from a control period to the next one, i.e. making sure that no DC component is injected. However, a mismatch between the ISR and the switching frequency update is obtained, introducing an additional (variable) delay component in the control loop, depending on the converter switching frequency itself. Nevertheless, the effect of this delay can be neglected in a first approximation, as the minimum f_{sw}/f_s ratio considered herein is always > 5.

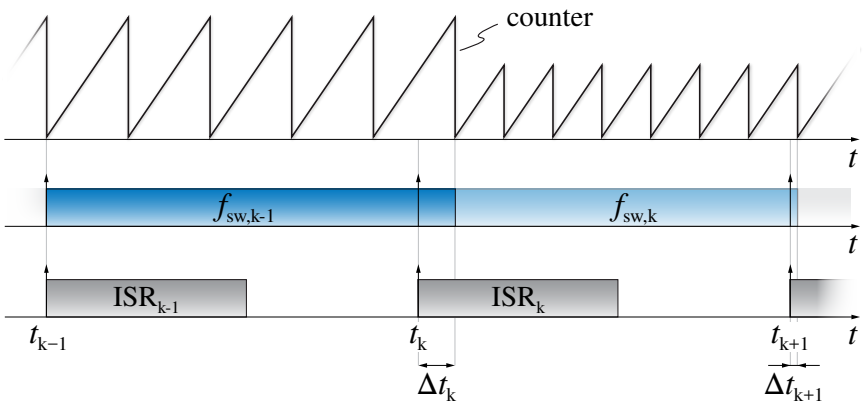


Fig. 7.20: Functional schematic and timing diagram of the implemented PWM update process. The switching frequency is updated in correspondence of the counter roll-over following the start of the ISR, in order to preserve the 50 % duty cycle constraint. A variable update delay Δt_k is introduced.

The experimental tests are performed leveraging the setup illustrated in **Fig. 6.25** (cf. **Chapter 6**), using two independent bidirectional DC supplies operated in constant-voltage mode respectively connected at the input and at the output of the converter. In this section, the static switching frequency LUT extraction procedure is described and the LLC output current control performance is assessed both in steady-state and dynamical conditions.

7.5.1 Look-Up Table (LUT) Extraction

The automated test setup described in **Section 6.4** (cf. **Fig. 6.25**) is exploited to extract both the $f_{sw}(M,Q)$ 2D LUT and the $f_{sw,min}(M)$ 1D LUT, required by the proposed output current control scheme shown in **Fig. 7.12**. In particular, MATLAB® environment has been exploited to communicate with the DC supplies and the MCU.

Fig. 7.21(a) shows the schematic diagram of the implemented control strategy for the LUT extraction, where a fixed reference input voltage $V_i^* = 325\,V$ is assumed for the whole procedure. Each LUT point is defined by a reference value pair (M^*,Q^*) with a sequential index k, which identifies the element number starting from the lower-left corner of the LUT (i.e., $M = M_{min}$, $Q = Q_{min}$), as illustrated in **Fig. 7.21(b)**. All references are provided through the MATLAB® interface. Specifically, the reference input voltage V_i^* is directly sent to the input DC supply, the reference voltage gain M^* is translated into and equivalent reference output voltage value V_o^* and sent to both the output DC supply and the MCU, and the reference quality factor Q^* is directly sent to the MCU. In the present case, the extraction procedure targets a 101x101 2D LUT and a 101x1 1D LUT with $0.75 \leq M^* \leq 1.25$ and $0 \leq Q^* \leq 1.5$, where the value of Q^* is saturated to the maximum allowed value $Q_{max}(M)$ reported in **Fig. 7.19(b)**, so that no LUT points located outside the LLC operating region are extracted.

Once the MCU receives the reference quality factor value Q^*, this is directly translated into a reference I_o^* for the current control loop. In this case, however, the control loop is simplified with respect to **Fig. 7.12**, as the required LUTs are still not available and the dynamical control performance is not of interest. Therefore, a purely integral regulator with a small gain k_I is adopted, featuring a slow but stable response and ensuring zero steady-state error (i.e., the primary goal of the controller). In general, the maximum switching frequency $f_{sw,max} = 250\,\text{kHz}$ should be fed forward at the output of the regulator, so that the converter always operates in the stable (i.e., inductive) region. Nevertheless, to speed up the transient, the last switching frequency value $f_{sw}[k-1]$ can be fed forward, leaving a significantly lower frequency error to be addressed by the integral regulator. In all cases, the reference output frequency is saturated to $f_{sw,max}$ and, once the specified time interval is over (i.e., 50 ms in the present case) the final switching frequency value is stored as $f_{sw}[k]$.

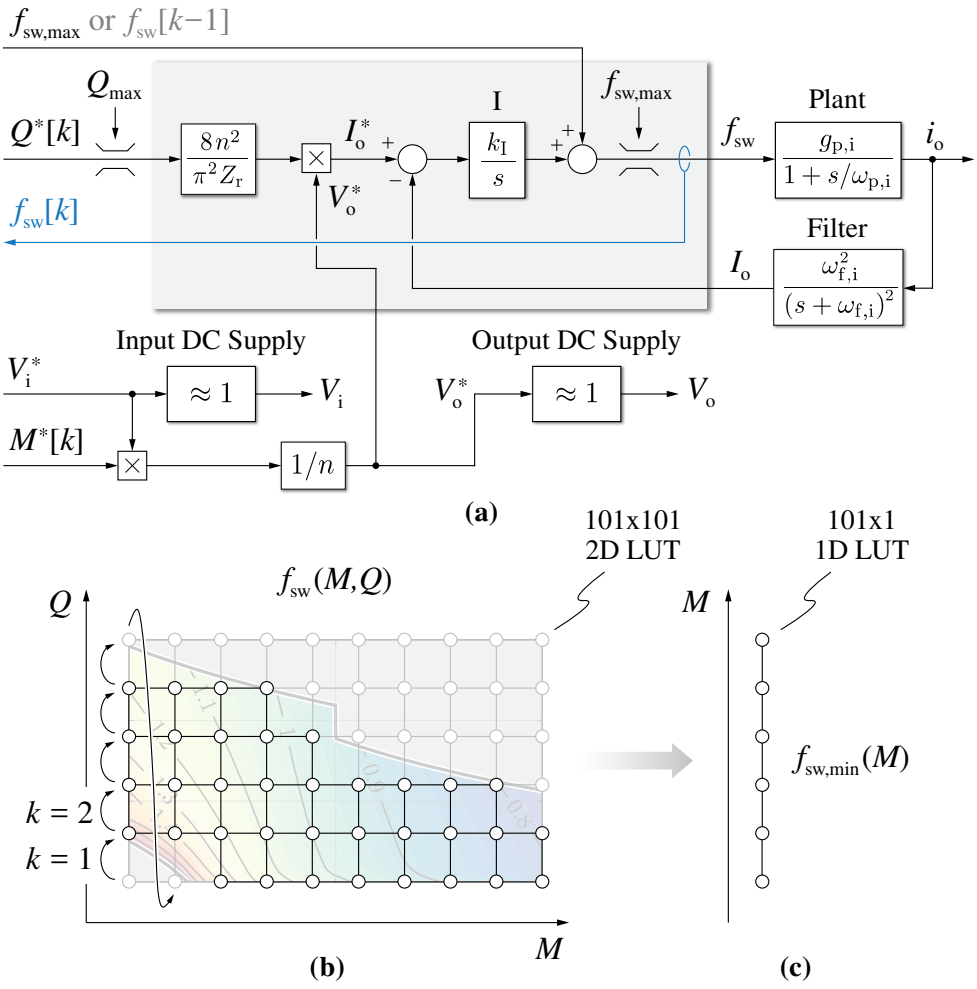


Fig. 7.21: **(a)** detailed schematic diagram of the implemented control strategy for the LUT extraction procedure, **(b)** $f_{sw}(M,Q)$ 2D LUT with highlight of the extraction sequence, **(c)** $f_{sw,min}(M)$ 1D LUT.

Depending on the total number of LUT elements, on the controller transient time and on the time allocated for the communication of the results, the 2D LUT extraction time can vary widely. In the present case, the overall time required for the complete LUT extraction is less than 1 hour, being the total number of LUT points ≈ 6700 (i.e., lower than 101x101 due to the $Q_{\max}$ limit) and the total time allocated to a single point $\approx 0.5\,\mathrm{s}$ (i.e., including communication).

Once the $f_{\mathrm{sw}}(M,Q)$ 2D LUT is obtained (cf. **Fig. 7.14(c)**), the $f_{\mathrm{sw,min}}(M)$ 1D LUT can be directly extracted by identifying the minimum switching frequency value for each value of M, found in correspondence of $Q = Q_{\max}(M)$ (i.e., the upper limit of the 2D LUT).

As a final remark, it is worth noting that, even though the 2D LUT is extracted assuming a single value of $V_{\mathrm{i}} = 325\,\mathrm{V}$, the $f_{\mathrm{sw}}(M,Q)$ values can be considered approximately independent of V_{i} and have broad applicability. In fact, the main V_{i}-dependent phenomena affecting the value of $f_{\mathrm{sw}}(M,Q)$ are the converter losses, which generate an input-to-output voltage drop and thus affect the real converter voltage gain M. However, since the M value is in direct proportion with the converter efficiency (e.g., a 3 % efficiency drop translates into a $\approx 3\,\%$ gain drop), only the V_{i} impact on efficiency affects the $f_{\mathrm{sw}}(M,Q)$ LUT. Therefore, as long as the ratio between losses and transferred power remains approximately unchanged with V_{i} (i.e., typically valid when V_{i} varies within a limited range), the extracted LUT maintains a high level of accuracy.

7.5.2 Steady-State Operation

The main converter steady-state waveforms are reported in **Fig. 6.27**–**Fig. 6.30** in **Section 6.4.2**. Nonetheless, a highlight of the instantaneous rectified current i_{o} and the battery-side current I_{b} (i.e., $\approx I_{\mathrm{o}}$) is reported in **Fig. 7.22** considering $V_{\mathrm{i}} = 325\,\mathrm{V}$ and $I_{\mathrm{o}}^{*} = 30\,\mathrm{A}$. In particular, the waveforms are reported for **(a)** boost-mode ($V_{\mathrm{o}} = 405\,\mathrm{V}$, $M \approx 1.25$, $f_{\mathrm{sw}} \approx 109\,\mathrm{kHz}$), **(b)** unity-gain-mode ($V_{\mathrm{o}} = 325\,\mathrm{V}$, $M = 1$, $f_{\mathrm{sw}} \approx 131\,\mathrm{kHz}$), **(c)** resonance-mode ($V_{\mathrm{o}} = 315\,\mathrm{V}$, $M \approx 0.97$, $f_{\mathrm{sw}} \approx 140\,\mathrm{kHz}$) and **(d)** buck-mode ($V_{\mathrm{o}} = 250\,\mathrm{V}$, $M \approx 0.77$, $f_{\mathrm{sw}} \approx 167\,\mathrm{kHz}$).

It is observed that the closed-loop current controller ensures zero steady-state error in all operating modes, including buck and boost (i.e., when the plant does not behave as a pure integrator), as a result of the integral part of the PI regulator. Moreover, as previously mentioned in **Section 6.4.2**, it is worth noting that the operation at resonance frequency (i.e., $f_{\mathrm{sw}} = f_{\mathrm{r}}$) does not take place at $M = 1$, but at slightly lower voltage gain values (i.e., $M \approx 0.97$ for $I_{\mathrm{o}} = 30\,\mathrm{A}$), as the system losses translate into an input-to-output voltage drop that is addressed by operating at $f_{\mathrm{sw}} < f_{\mathrm{r}}$.

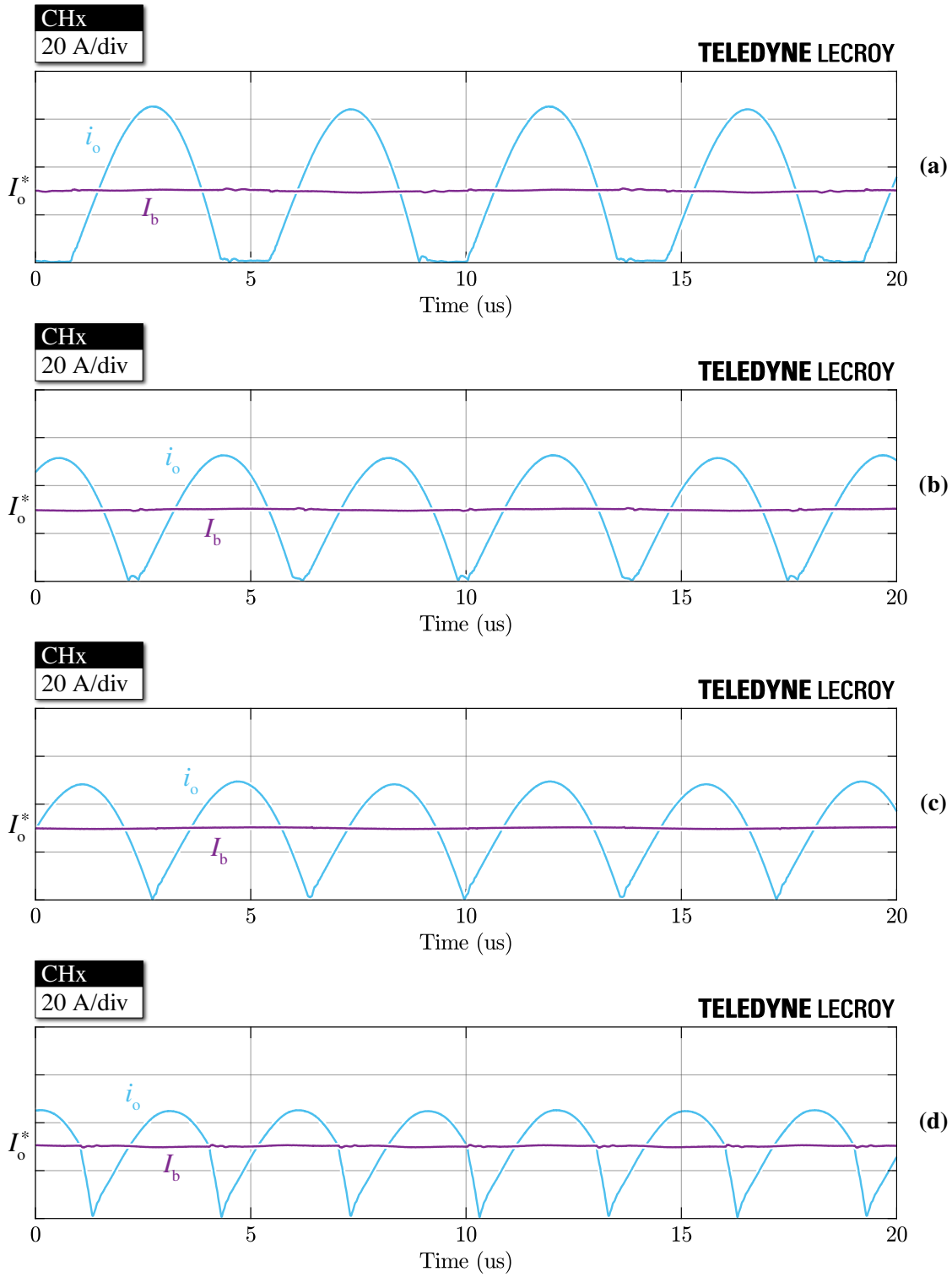


Fig. 7.22: Experimental converter waveforms in steady-state conditions with $V_i = 325\,V$, $I_o^* = 30\,A$ (cf. **Chapter 7**): output rectified current i_o and battery-side current $I_b \approx I_o$. The waveforms are obtained for **(a)** boost-mode (i.e., $V_o = 405\,V$, $M \approx 1.25$, $f_{sw} \approx 109\,kHz$), **(b)** unity-gain-mode (i.e., $V_o = 325\,V$, $M = 1$, $f_{sw} \approx 131\,kHz$), **(c)** resonance-mode (i.e., $V_o = 315\,V$, $M \approx 0.97$, $f_{sw} \approx 140\,kHz$), **(d)** buck-mode (i.e., $V_o = 250\,V$, $M \approx 0.77$, $f_{sw} \approx 167\,kHz$).

7.5.3 Dynamical Operation

In this section, the dynamical performance of the output current control is verified by assessing experimentally the response to a reference step, the ability to follow a 150 Hz sinusoidal reference and the rejection capability of a 150 Hz input voltage sinusoidal disturbance. In particular, to highlight the benefits of the proposed control scheme described in **Section 7.3.1** (i.e., in the following referred to as *PI + Adaptive Gain + Feedforward*), several control solutions are compared.

Reference Step Response

Fig. 7.23 shows the closed-loop control response to a current reference step from 10 A to 15 A in **(a)** boost-mode ($V_\mathrm{o} = 405\,\mathrm{V}$, $M \approx 1.25$), **(b)** unity-gain-mode ($V_\mathrm{o} = 325\,\mathrm{V}$, $M = 1$) and **(c)** buck-mode ($V_\mathrm{o} = 250\,\mathrm{V}$, $M \approx 0.77$). The rectifier output current i_o, the battery-side current I_b, the reference output current I_o^* and the feedback current I_o are reported. Both I_o^* and I_o are measured at the output of two separate MCU digital-to-analog converters (DACs) with a 0–3.3 V scale, therefore the measured signals are properly rescaled. It is observed that all responses feature a $T_\mathrm{s} = 50\,\mu\mathrm{s}$ discretization of the sampled current I_o and a $2\,T_\mathrm{s}$ delay between the I_o^* reference step and the first I_o current sample (i.e., due to discretized update of the DACs at the end of the control period). It is worth noting that, even though the battery-side current I_b seems to directly represent the mean value of the rectified current i_o, the real dynamics of the system should be directly observed from the envelope of i_o, as I_b is measured at the output of the filter capacitor C_o and thus includes a time delay.

The first control strategy is reported on top and represents the reference case (i.e., state-of-the-art). This strategy adopts a conventional PI regulator tuned to achieve the desired current control open-loop cross-over frequency $f_\mathrm{c,i} \approx 1.1\,\mathrm{kHz}$ with the methodology reported in [178], setting the PI zero to $f_\mathrm{c,i}/5$. Specifically, this controller design approach should ensure the desired controller bandwidth under unity-gain-mode operation and lower dynamical performance in boost-mode and buck-mode, due to the non-adaptive controller gain. However, the results in **(b)** show that the target controller bandwidth is not achieved in resonance/unity-gain mode, as the response is much slower than expected. The main reason behind this discrepancy resides in the resistive nature of the real system, which does not behave as a pure integrator at the resonance frequency, as demonstrated by the experimental switching frequency LUT in **Fig. 7.14(c)**. In fact, due to the first order low-pass filter behavior of the system, the controller tuning proposed in [178] is no longer effective. Furthermore, the absence of an adaptive controller gain leads to a large variation of the closed-loop dynamics, especially in buck-mode (cf. **Fig. 7.23(c)**), where the system open-loop gain drops significantly.

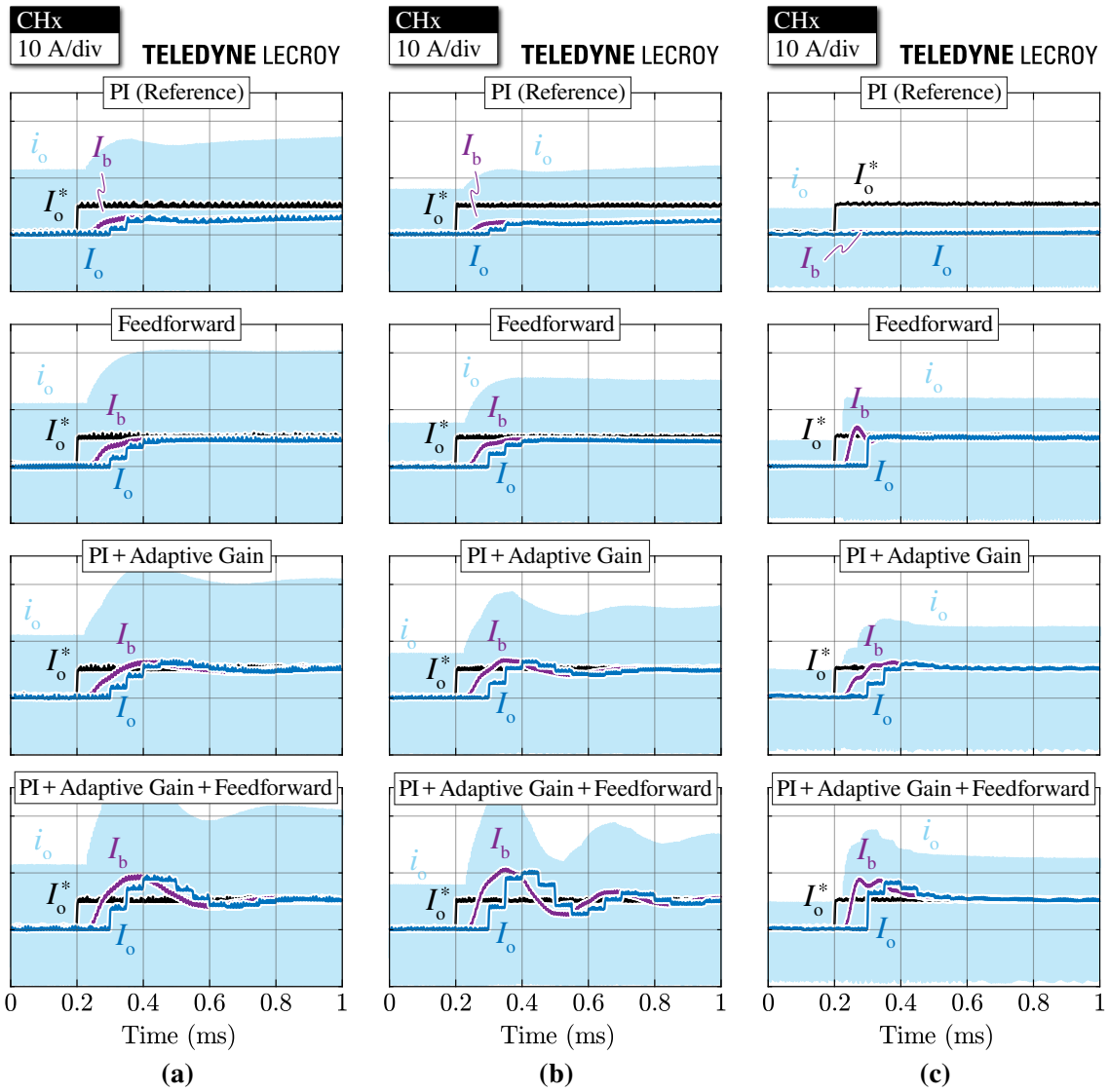


Fig. 7.23: Experimental reference step response of the output current control loop between $I_o^* = 10\,\text{A}$ and $I_o^* = 15\,\text{A}$. The waveforms of the rectifier output current i_o, the battery-side current I_b, the reference output current I_o^* and the feedback current I_o are shown for $V_i = 325\,\text{V}$ in **(a)** boost-mode ($V_o = 405\,\text{V}$, $M \approx 1.25$), **(b)** unity-gain-mode ($V_o = 325\,\text{V}$, $M = 1$) and **(c)** buck-mode ($V_o = 250\,\text{V}$, $M \approx 0.77$). I_o^* and I_o are measured at the output of two separate MCU digital-to-analog converters (DACs) with a 0–3.3 V scale, therefore they are properly rescaled. Four control strategies are compared, from top to bottom: *PI* (reference case), *Feedforward*, *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward* (i.e., the adopted strategy).

The second set of waveforms from the top shows the results obtained with the sole use of the feedforward term coming from the LUT interpolation. These waveforms provide a useful insight on the LLC system dynamics, as they highlight the open-loop system response to a switching frequency step. It is observed that the response in buck-mode is significantly faster and less damped than in unity-gain-mode and boost-mode, as buck-mode operation features an imaginary beat-frequency double pole located at higher frequency

than the real dominant pole in the other two modes (cf. **Fig. 7.4**). Even though the LUT is very precise in the present situation, it must be noted that such an open-loop control strategy cannot ensure zero steady-state error in all conditions, mainly due to LUT inaccuracies, converter tolerances and temperature dependence of the system parameters. Therefore, the feedforward approach is typically complemented by an integral regulator with slow dynamical characteristics with the only aim of correcting the steady-state feedforward error. Anyhow, this integral regulator does not ensure a constant and/or controlled bandwidth, therefore this approach will not be considered for the following tests.

The third control strategy reproduces the control scheme of **Fig. 7.12** without implementing the feedforward term, therefore only exploiting the PI and the gain adaptation process. This strategy allows to verify the controller tuning and the consistent closed-loop bandwidth throughout the LLC operating region, decoupling the PI operation from the feedforward contribution. Even though the system small-signal steady-state gain changes by more than one order of magnitude between buck-mode and boost-mode, the experimental waveforms show that the output current step response remains mostly unaffected by the converter operating point. Moreover, the consistent rise-time $t_\mathrm{r} \approx 150\,\mu\mathrm{s}$ translates into a constant closed-loop bandwidth

$$f_{\mathrm{bw,\text{-}3dB}} \approx \frac{0.35}{t_\mathrm{r}} \tag{7.53}$$

of approximately 2.3 kHz, closely matching the simulated transfer functions in **Fig. 7.16**–**Fig. 7.18**.

Finally, the last set of waveforms is obtained with the complete control strategy reported in **Fig. 7.12**, i.e., adding the feedforward term at the output of the PI regulator with adaptive gain. It is observed that the step responses feature significantly higher overshoot and lower damping than in the previous case. The reason behind this is the overlap between the feedforward term and the proportional part of the PI regulator, as they both act instantaneously in correspondence of the reference step and cause an excessive switching frequency response, which generates the current overshoot and the subsequent oscillation. In general, all solutions featuring a high performance PI regulator together with a feedforward block are not suited for reference step changes, because of the mentioned reasons. Nevertheless, in battery charger applications reference step changes are not required, as the target charging current is typically ramped up/down with a finite slope and output current steps are unnecessary. Therefore, due to the combined action of feedforward and PI regulator with adaptive gain, this control strategy features the most promising dynamical performance, particularly needed for the disturbance rejection of high frequency components (e.g., input voltage oscillations).

Sinusoidal Reference Tracking

The control loop capability to track a large-signal sinusoidal reference is illustrated in **Fig. 7.24**, where the system response to a 150 Hz, 10 A peak-to-peak current reference is reported. The resonant tank current i_r, the rectifier output current i_o, the battery-side current I_b, the reference output current I_o^* and the feedback current I_o are shown. Also in

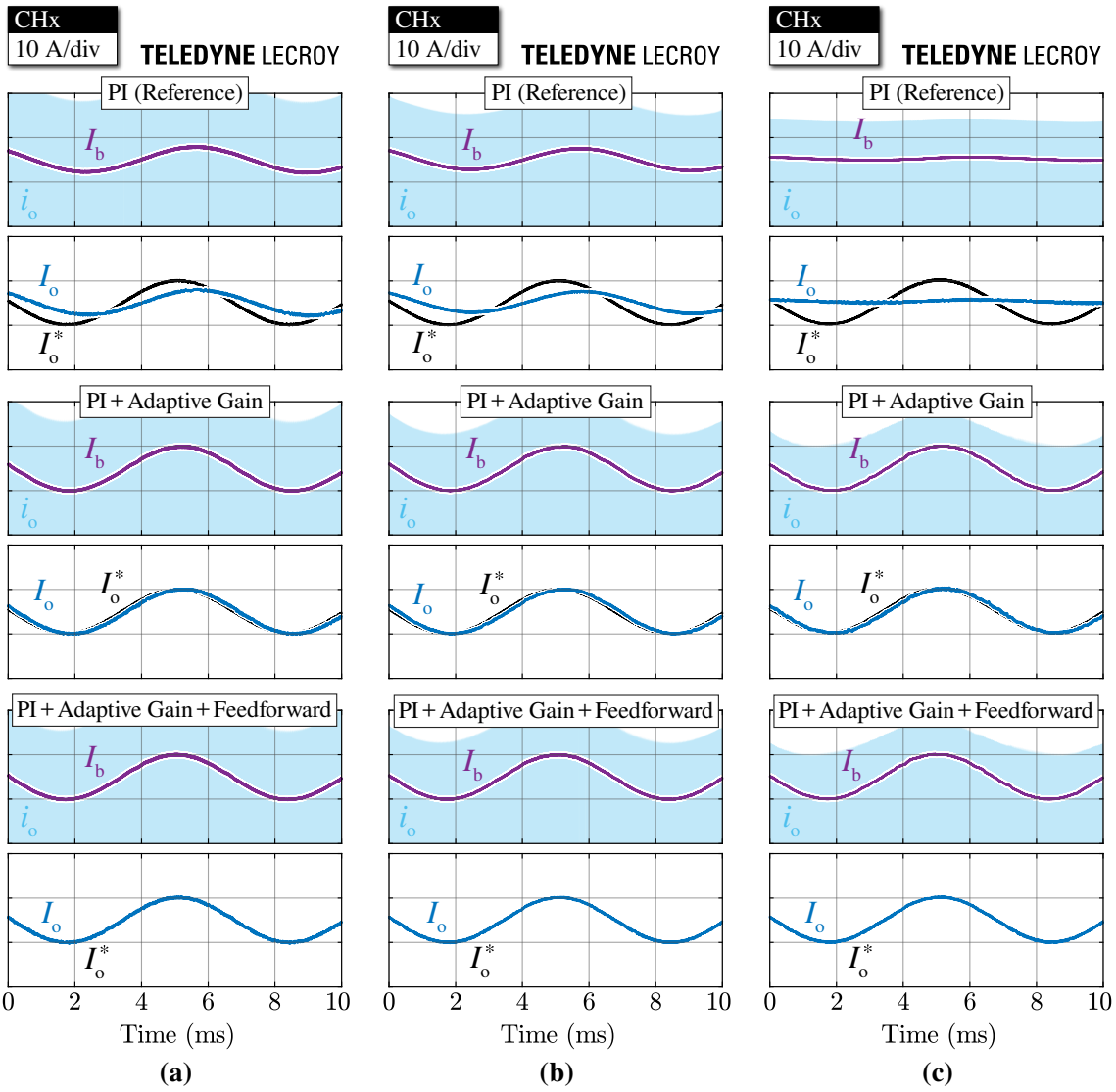


Fig. 7.24: Experimental steady-state response of the output current control loop to a 150 Hz, 10 A peak-to-peak sinusoidal reference. The waveforms of the rectifier output current i_o, the battery-side current I_b, the reference output current I_o^* and the feedback current I_o are shown for $V_i = 325$ V in **(a)** boost-mode ($V_o = 405$ V, $M \approx 1.25$), **(b)** unity-gain-mode ($V_o = 325$ V, $M = 1$) and **(c)** buck-mode ($V_o = 250$ V, $M \approx 0.77$). I_o^* and I_o are measured at the output of two separate MCU digital-to-analog converters (DACs) with a 0–3.3 V scale, therefore they are properly rescaled. Three control strategies are compared, from top to bottom: *PI* (reference case), *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward* (i.e., the adopted strategy).

this case, the control performance is assessed in three operating points (i.e., boost-mode, unity-gain-mode, buck-mode) and adopting different control strategies, namely *PI*, *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward*. It is immediately observed that the conventional *PI* control is not able to track the reference, as the real control loop bandwidth is much lower than the target value. In unity-gain-mode and boost-mode, this translates in substantial amplitude reduction and phase delay, whereas in buck-mode the system appears to completely neglect the reference due to the large and uncompensated small-signal gain drop of the plant. These issues are addressed by the *PI + Adaptive Gain* control strategy, which closely follows the sinusoidal reference. However a noticeable phase shift is observed, as expected from the simulated closed-loop transfer functions in **Fig. 7.16–Fig. 7.18**. Thanks to the added feedforward contribution, the *PI + Adaptive Gain + Feedforward* control strategy eliminates the phase shift, demonstrating enhanced dynamical performance.

Disturbance Rejection Capability

The last experimental tests assess the control loop capability to reject a large-signal sinusoidal disturbance applied to the input DC-link voltage V_{i}. Specifically, a 150 Hz, 10 V peak-to-peak oscillation is superimposed to $V_{\mathrm{i}} = 325\,\mathrm{V}$ and a 15 A reference output current is targeted at steady-state. The sinusoidal input voltage disturbance specifically emulates the DC-link mid-point voltage oscillation generated by the three-phase three-level rectifier stage connected to the 50 Hz European low-voltage grid (cf. **Chapter 2–Chapter 4**). Nonetheless, a similar situation is also encountered in all single-phase dual-stage (i.e., AC/DC + DC/DC) battery chargers, where the AC/DC converter generates a voltage ripple at two times the grid frequency (i.e., 100 Hz or 120 Hz) at the input of the following DC/DC stage. Therefore, the proper rejection of the input voltage oscillation (i.e., the minimization of the induced output current ripple) is a fundamental requirement in battery charging applications and represents the most demanding control requirement for an LLC converter, due to its strongly non-linear behavior.

The results of these tests are illustrated in **Fig. 7.25**, where the instantaneous input voltage V_{i}, the rectifier output current i_{o} and the battery-side current I_{b} are shown in three operating points (i.e., boost-mode, unity-gain-mode, buck-mode) and adopting different control strategies, namely *PI*, *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward*. It is observed that in all cases the shape of V_{i} is visibly distorted, as the available DC power supply was not able to perfectly synthesize a 150 Hz sine waveform. Therefore, the V_{i} disturbance features higher order harmonics, which are significantly harder to reject by the closed-loop control. Nevertheless, the experimental results still provide a fair

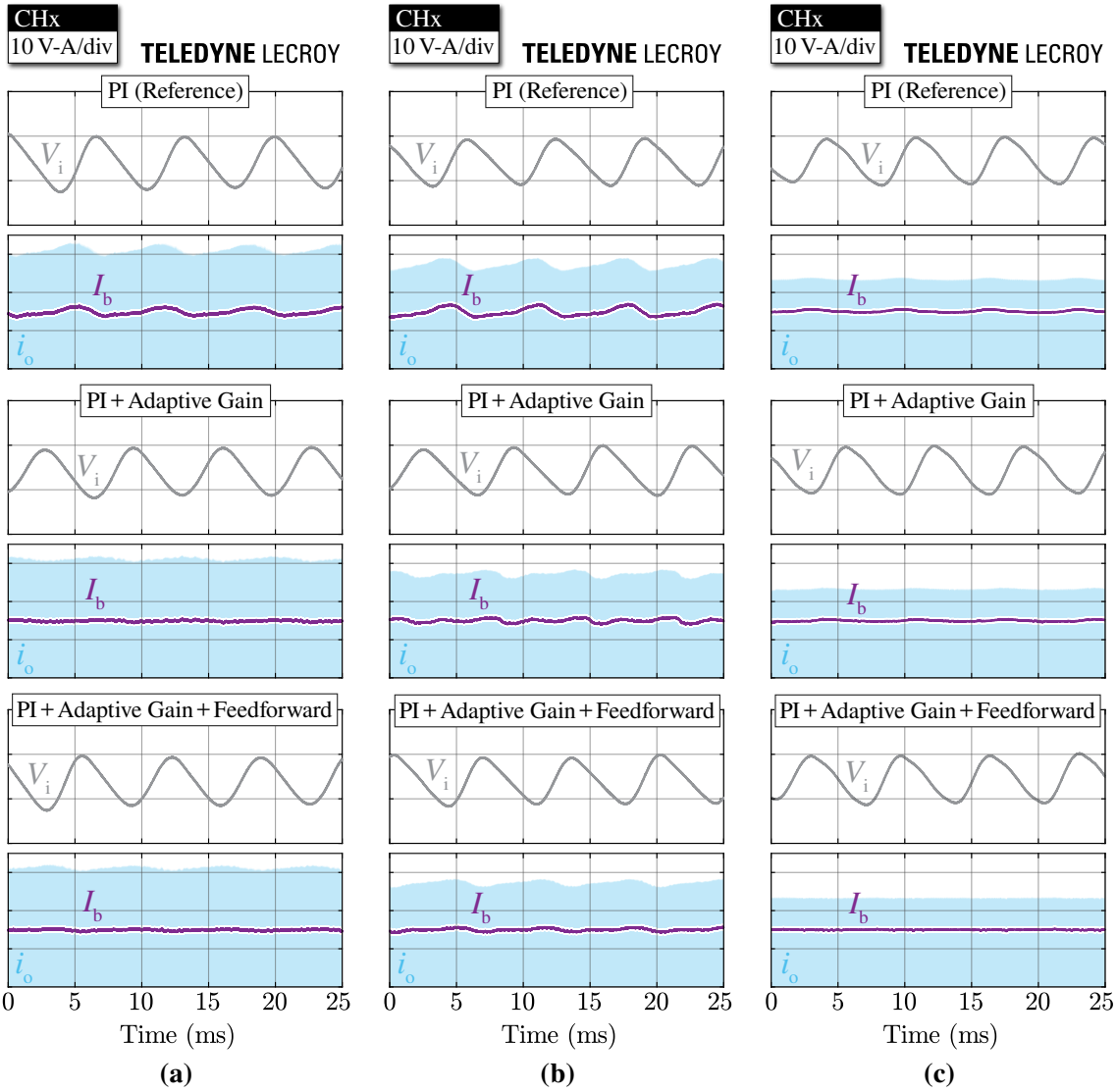


Fig. 7.25: Experimental steady-state response of the output current control loop to a 150 Hz, 10 V peak-to-peak input voltage pseudo-sinusoidal disturbance. The waveforms of the instantaneous input voltage V_i, the rectifier output current i_o and the battery-side current I_b are shown in **(a)** boost-mode ($V_o = 405\,V$, $M \approx 1.25$), **(b)** unity-gain-mode ($V_o = 325\,V$, $M \approx 1$) and **(c)** buck-mode ($V_o = 250\,V$, $M \approx 0.77$). Three control strategies are compared, from top to bottom: *PI* (reference case), *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward* (i.e., the adopted strategy).

performance comparison among control strategies. The conventional *PI* strategy shows the worst overall rejection performance, due to the design bandwidth overestimation and the uncompensated small-signal gain variation of the plant. Better performance is achieved by the *PI + Adaptive Gain* control, which features a lower output current ripple as a result of the adaptive gain and the consistent control bandwidth over the complete LLC operating region. Finally, the *PI + Adaptive Gain + Feedforward* strategy demonstrates the best disturbance rejection capabilities, approximately eliminating the current ripple in boost-mode and buck-mode, while strongly reducing it around unity-gain operation.

In particular, unity-gain operation represents the most challenging condition to reject the input voltage ripple, since the derivative $\partial Q/\partial M$ (i.e., proportional to the output current variation induced by the input voltage oscillation $\partial I_o/\partial V_i$) reaches its maximum, as attested by the slope of the iso-frequency lines in **Fig. 7.14(c)**.

7.6 Summary

This chapter has presented the design, tuning and experimental assessment of the adopted digital multi-loop control strategy for the considered LLC resonant converter for EV ultra-fast battery charging. A novel simplified dual first order small-signal model of the LLC converter has been derived from the well-known seventh order model, aiming to provide a straightforward tool for the design of the closed-loop controllers. Therefore, a dual-loop control scheme consisting of an outer voltage loop and an inner current loop has been designed and a complete analytical tuning procedure for both controllers has been described. In particular, the non-linear behavior of the frequency-to-current transfer function has been counteracted by a real-time controller gain adaptation process ensuring constant control bandwidth. To achieve best compensation accuracy, the adaptive gain values have been derived from a static switching frequency LUT obtained by experimental characterization of the converter. Moreover, the steady-state switching frequency value has been fed forward at the output of the current loop regulator to further enhance the system dynamical performance. The effectiveness of the proposed control strategy has been verified both in simulation environment and experimentally on the 15 kW LLC converter prototype, adopting a general purpose MCU for the digital control implementation (i.e., running at 20 kHz). In particular, the reference step response, the sinusoidal reference tracking ability and the input DC-link voltage ripple rejection degree of the current control loop have been assessed. The results have demonstrated the quasi-constant closed-loop bandwidth of the proposed control strategy across the complete converter operating range (i.e., variable load and voltage gain) and its superior dynamical performance with respect to a state-of-the-art solution based on a PI regulator.

Appendix 7.A Linearized State-Space Model Coefficients

Matrices $A = \frac{\partial F}{\partial X}\big|_{\bar{X},\bar{U}}$, $B = \frac{\partial F}{\partial U}\big|_{\bar{X},\bar{U}}$, $C = \frac{\partial G}{\partial X}\big|_{\bar{X},\bar{U}}$ and $D = \frac{\partial G}{\partial U}\big|_{\bar{X},\bar{U}}$ are the seventh order system Jacobian matrices evaluated at a selected equilibrium operating point, obtained by numerically solving (7.19). In the following, F_1, F_2, F_3, F_4, F_5, F_6, F_7 refer to the system

non-linear equations (7.11), (7.12), (7.13), (7.14), (7.15), (7.16), (7.17), respectively. It is worth noting that the superscript – indicates steady-state/equilibrium variables.

Matrix A consists of the following elements:

- $a_{11} = \dfrac{\partial F_1}{\partial I_{\mathrm{rs}}} = -\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{r}}} \dfrac{\bar{I}_{\mathrm{p}}^2 - (\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})^2}{\bar{I}_{\mathrm{p}}^3},$
- $a_{12} = \dfrac{\partial F_1}{\partial I_{\mathrm{rc}}} = +\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{r}}} \dfrac{(\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})(\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})}{\bar{I}_{\mathrm{p}}^3} - 2\pi\bar{f}_{\mathrm{sw}},$
- $a_{13} = \dfrac{\partial F_1}{\partial V_{\mathrm{cs}}} = -\dfrac{1}{L_{\mathrm{r}}},$
- $a_{14} = \dfrac{\partial F_1}{\partial V_{\mathrm{cc}}} = 0,$
- $a_{15} = \dfrac{\partial F_1}{\partial I_{\mathrm{ms}}} = +\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{r}}} \dfrac{\bar{I}_{\mathrm{p}}^2 - (\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})^2}{\bar{I}_{\mathrm{p}}^3},$
- $a_{16} = \dfrac{\partial F_1}{\partial I_{\mathrm{mc}}} = -\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{r}}} \dfrac{(\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})(\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})}{\bar{I}_{\mathrm{p}}^3},$
- $a_{17} = \dfrac{\partial F_1}{\partial V_{\mathrm{o}}} = -\dfrac{4n}{\pi L_{\mathrm{r}}} \dfrac{\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}}}{\bar{I}_{\mathrm{p}}},$
- $a_{21} = \dfrac{\partial F_2}{\partial I_{\mathrm{rs}}} = +\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{r}}} \dfrac{(\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})(\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})}{\bar{I}_{\mathrm{p}}^3} + 2\pi\bar{f}_{\mathrm{sw}},$
- $a_{22} = \dfrac{\partial F_2}{\partial I_{\mathrm{rc}}} = -\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{r}}} \dfrac{\bar{I}_{\mathrm{p}}^2 - (\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})^2}{\bar{I}_{\mathrm{p}}^3},$
- $a_{23} = \dfrac{\partial F_2}{\partial V_{\mathrm{cs}}} = 0,$
- $a_{24} = \dfrac{\partial F_2}{\partial V_{\mathrm{cc}}} = -\dfrac{1}{L_{\mathrm{r}}},$
- $a_{25} = \dfrac{\partial F_2}{\partial I_{\mathrm{ms}}} = -\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{r}}} \dfrac{(\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})(\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})}{\bar{I}_{\mathrm{p}}^3},$

- $a_{26} = \dfrac{\partial F_2}{\partial I_{\mathrm{mc}}} = +\dfrac{4\,n\,\bar{V}_{\mathrm{o}}}{\pi\,L_{\mathrm{r}}}\dfrac{\bar{I}_{\mathrm{p}}^2 + (\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})^2}{\bar{I}_{\mathrm{p}}^3}$,
- $a_{27} = \dfrac{\partial F_2}{\partial V_{\mathrm{o}}} = -\dfrac{4\,n}{\pi\,L_{\mathrm{r}}}\dfrac{\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}}}{\bar{I}_{\mathrm{p}}}$,
- $a_{31} = \dfrac{\partial F_3}{\partial I_{\mathrm{rs}}} = \dfrac{1}{C_{\mathrm{r}}}$,
- $a_{32} = \dfrac{\partial F_3}{\partial I_{\mathrm{rc}}} = 0$,
- $a_{33} = \dfrac{\partial F_3}{\partial V_{\mathrm{rs}}} = 0$,
- $a_{34} = \dfrac{\partial F_3}{\partial V_{\mathrm{rc}}} = -2\pi\bar{f}_{\mathrm{sw}}$,
- $a_{35} = \dfrac{\partial F_3}{\partial I_{\mathrm{ms}}} = 0$,
- $a_{36} = \dfrac{\partial F_3}{\partial I_{\mathrm{mc}}} = 0$,
- $a_{37} = \dfrac{\partial F_3}{\partial V_{\mathrm{o}}} = 0$,
- $a_{41} = \dfrac{\partial F_4}{\partial I_{\mathrm{rs}}} = 0$,
- $a_{42} = \dfrac{\partial F_4}{\partial I_{\mathrm{rc}}} = \dfrac{1}{C_{\mathrm{r}}}$,
- $a_{43} = \dfrac{\partial F_4}{\partial V_{\mathrm{rs}}} = 2\pi\bar{f}_{\mathrm{sw}}$,
- $a_{44} = \dfrac{\partial F_4}{\partial V_{\mathrm{rc}}} = 0$,
- $a_{45} = \dfrac{\partial F_4}{\partial I_{\mathrm{ms}}} = 0$,

- $a_{46} = \dfrac{\partial F_4}{\partial I_{\mathrm{mc}}} = 0,$
- $a_{47} = \dfrac{\partial F_4}{\partial V_{\mathrm{o}}} = 0,$
- $a_{51} = \dfrac{\partial F_5}{\partial I_{\mathrm{rs}}} = +\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{m}}} \dfrac{\bar{I}_{\mathrm{p}}^2 - (\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})^2}{\bar{I}_{\mathrm{p}}^3},$
- $a_{52} = \dfrac{\partial F_5}{\partial I_{\mathrm{rc}}} = -\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{m}}} \dfrac{(\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})(\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})}{\bar{I}_{\mathrm{p}}^3},$
- $a_{53} = \dfrac{\partial F_5}{\partial V_{\mathrm{cs}}} = 0,$
- $a_{54} = \dfrac{\partial F_5}{\partial V_{\mathrm{cc}}} = 0,$
- $a_{55} = \dfrac{\partial F_5}{\partial I_{\mathrm{ms}}} = -\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{m}}} \dfrac{\bar{I}_{\mathrm{p}}^2 - (\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})^2}{\bar{I}_{\mathrm{p}}^3},$
- $a_{56} = \dfrac{\partial F_5}{\partial I_{\mathrm{mc}}} = +\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{m}}} \dfrac{(\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})(\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})}{\bar{I}_{\mathrm{p}}^3} - 2\pi\bar{f}_{\mathrm{sw}},$
- $a_{57} = \dfrac{\partial F_5}{\partial V_{\mathrm{o}}} = +\dfrac{4n}{\pi L_{\mathrm{m}}} \dfrac{\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}}}{\bar{I}_{\mathrm{p}}},$
- $a_{61} = \dfrac{\partial F_6}{\partial I_{\mathrm{rs}}} = -\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{m}}} \dfrac{(\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})(\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})}{\bar{I}_{\mathrm{p}}^3},$
- $a_{62} = \dfrac{\partial F_6}{\partial I_{\mathrm{rc}}} = +\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{m}}} \dfrac{\bar{I}_{\mathrm{p}}^2 - (\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})^2}{\bar{I}_{\mathrm{p}}^3},$
- $a_{63} = \dfrac{\partial F_6}{\partial V_{\mathrm{cs}}} = 0,$
- $a_{64} = \dfrac{\partial F_6}{\partial V_{\mathrm{cc}}} = 0,$

- $a_{65} = \dfrac{\partial F_6}{\partial I_{\mathrm{ms}}} = +\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{m}}} \dfrac{(\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}})(\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})}{\bar{I}_{\mathrm{p}}^3} + 2\pi \bar{f}_{\mathrm{sw}},$
- $a_{66} = \dfrac{\partial F_6}{\partial I_{\mathrm{mc}}} = -\dfrac{4n\bar{V}_{\mathrm{o}}}{\pi L_{\mathrm{m}}} \dfrac{\bar{I}_{\mathrm{p}}^2 - (\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}})^2}{\bar{I}_{\mathrm{p}}^3},$
- $a_{67} = \dfrac{\partial F_6}{\partial V_{\mathrm{o}}} = +\dfrac{4n}{\pi L_{\mathrm{m}}} \dfrac{\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}}}{\bar{I}_{\mathrm{p}}},$
- $a_{71} = \dfrac{\partial F_7}{\partial I_{\mathrm{rs}}} = +\dfrac{2n}{\pi C_{\mathrm{o}}} \dfrac{\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}}}{\bar{I}_{\mathrm{p}}},$
- $a_{72} = \dfrac{\partial F_7}{\partial I_{\mathrm{rc}}} = +\dfrac{2n}{\pi C_{\mathrm{o}}} \dfrac{\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}}}{\bar{I}_{\mathrm{p}}},$
- $a_{73} = \dfrac{\partial F_7}{\partial V_{\mathrm{rs}}} = 0,$
- $a_{74} = \dfrac{\partial F_7}{\partial V_{\mathrm{rc}}} = 0,$
- $a_{75} = \dfrac{\partial F_7}{\partial I_{\mathrm{ms}}} = -\dfrac{2n}{\pi C_{\mathrm{o}}} \dfrac{\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}}}{\bar{I}_{\mathrm{p}}},$
- $a_{76} = \dfrac{\partial F_7}{\partial I_{\mathrm{mc}}} = -\dfrac{2n}{\pi C_{\mathrm{o}}} \dfrac{\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}}}{\bar{I}_{\mathrm{p}}},$
- $a_{77} = \dfrac{\partial F_7}{\partial V_{\mathrm{o}}} = -\dfrac{1}{R_{\mathrm{b}} C_{\mathrm{o}}},$

Vector B consists of the following elements:

- $b_{11} = \dfrac{\partial F_1}{\partial f_{\mathrm{sw}}} = -2\pi I_{\mathrm{rc}},$
- $b_{21} = \dfrac{\partial F_2}{\partial f_{\mathrm{sw}}} = +2\pi I_{\mathrm{rs}},$
- $b_{31} = \dfrac{\partial F_3}{\partial f_{\mathrm{sw}}} = -2\pi V_{\mathrm{cc}},$

- $b_{41} = \dfrac{\partial F_4}{\partial f_{\mathrm{sw}}} = +2\pi V_{\mathrm{cs}},$
- $b_{51} = \dfrac{\partial F_5}{\partial f_{\mathrm{sw}}} = -2\pi I_{\mathrm{mc}},$
- $b_{61} = \dfrac{\partial F_6}{\partial f_{\mathrm{sw}}} = +2\pi I_{\mathrm{ms}},$
- $b_{71} = \dfrac{\partial F_7}{\partial f_{\mathrm{sw}}} = 0,$

Depending on which system output variable is selected, vector C changes expression. Assuming $G = V_{\mathrm{o}}$, the following elements are obtained:

- $c_{11} = \dfrac{\partial G}{\partial I_{\mathrm{rs}}} = 0,$
- $c_{12} = \dfrac{\partial G}{\partial I_{\mathrm{rc}}} = 0,$
- $c_{13} = \dfrac{\partial G}{\partial V_{\mathrm{cs}}} = 0,$
- $c_{14} = \dfrac{\partial G}{\partial V_{\mathrm{cc}}} = 0,$
- $c_{15} = \dfrac{\partial G}{\partial I_{\mathrm{ms}}} = 0,$
- $c_{16} = \dfrac{\partial G}{\partial I_{\mathrm{mc}}} = 0,$
- $c_{17} = \dfrac{\partial G}{\partial V_{\mathrm{o}}} = 1,$

Assuming $G = I_{\mathrm{o}}$, vector C can be obtained deriving (7.9):

- $c_{11} = \dfrac{\partial G}{\partial I_{\mathrm{rs}}} = \dfrac{2n}{\pi} \dfrac{\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}}}{\bar{I}_{\mathrm{p}}},$

- $c_{12} = \dfrac{\partial G}{\partial I_{\mathrm{rc}}} = \dfrac{2n}{\pi}\dfrac{\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}}}{\bar{I}_{\mathrm{p}}}$,
- $c_{13} = \dfrac{\partial G}{\partial V_{\mathrm{cs}}} = 0$,
- $c_{14} = \dfrac{\partial G}{\partial V_{\mathrm{cc}}} = 0$,
- $c_{15} = \dfrac{\partial G}{\partial I_{\mathrm{ms}}} = -\dfrac{2n}{\pi}\dfrac{\bar{I}_{\mathrm{rs}} - \bar{I}_{\mathrm{ms}}}{\bar{I}_{\mathrm{p}}}$,
- $c_{16} = \dfrac{\partial G}{\partial I_{\mathrm{mc}}} = -\dfrac{2n}{\pi}\dfrac{\bar{I}_{\mathrm{rc}} - \bar{I}_{\mathrm{mc}}}{\bar{I}_{\mathrm{p}}}$,
- $c_{17} = \dfrac{\partial G}{\partial V_{\mathrm{o}}} = 0$,

In both previous cases $D = \partial G / \partial f_{\mathrm{sw}} = 0$.

Appendix 7.B LUT Interpolation and Derivative

This section describes the 2D LUT interpolation and derivative calculation approaches implemented on the MCU.

Being (x, y) the value pair identifying the interpolation point, the LUT (i.e., matrix) indices related to the lower left corner of the interpolation region are identified as

$$\begin{cases} i_{\mathrm{x}} = 1 + \mathrm{floor}\left(\dfrac{x - X_{\mathrm{min}}}{\Delta X}\right) \\ i_{\mathrm{y}} = 1 + \mathrm{floor}\left(\dfrac{y - Y_{\mathrm{min}}}{\Delta Y}\right) \end{cases}, \tag{7.54}$$

where i_{x}, i_{y} are the matrix indices along the horizontal and vertical directions, respectively, ΔX, ΔY are the x, y spacings between elements, and X_{min}, Y_{min} are the minimum x, y values of the LUT, as shown in **Fig. 7.26**. Defining the remainders of the floor function, i.e.,

$$\begin{cases} r_{\mathrm{x}} = \dfrac{x - X_{\mathrm{min}}}{\Delta X} - \mathrm{floor}\left(\dfrac{x - X_{\mathrm{min}}}{\Delta X}\right) \\ r_{\mathrm{y}} = \dfrac{y - Y_{\mathrm{min}}}{\Delta Y} - \mathrm{floor}\left(\dfrac{y - Y_{\mathrm{min}}}{\Delta Y}\right) \end{cases}, \tag{7.55}$$

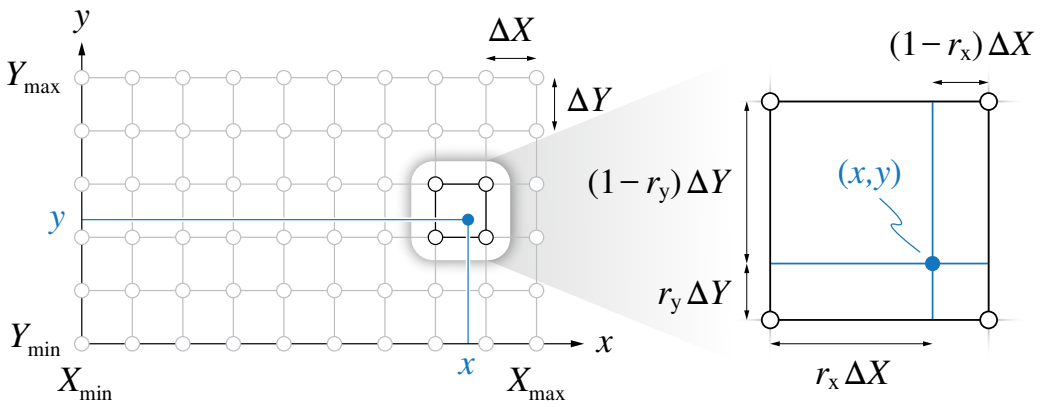


Fig. 7.26: Simplified schematic of the adopted 2D interpolation approach.

the interpolated function value f can be calculated as

$$f(x,y) = (1-r_y)\left[r_x F(i_x+1,i_y) - (1-r_x)F(i_x,i_y)\right] + r_y\left[r_x F(i_x+1,i_y+1) - (1-r_x)F(i_x,i_y+1)\right], \quad (7.56)$$

where $F(i_x,i_y)$ is the LUT/matrix element identified by i_x and i_y.

Furthermore, the derivative values of f along both x and y directions can be approximated as

$$\left.\frac{\partial f}{\partial x}\right|_{x,y} \approx (1-r_y)\frac{F(i_x+1,i_y)-F(i_x,i_y)}{\Delta X} + r_y\frac{F(i_x+1,i_y+1)-F(i_x,i_y+1)}{\Delta X}, \quad (7.57)$$

$$\left.\frac{\partial f}{\partial y}\right|_{x,y} \approx (1-r_x)\frac{F(i_x,i_y+1)-F(i_x,i_y)}{\Delta Y} + r_x\frac{F(i_x+1,i_y+1)-F(i_x+1,i_y)}{\Delta Y}. \quad (7.58)$$

Even though better approaches for the calculation of the derivatives are available, they are more computationally intensive with respect to (7.57) and (7.58), therefore they are not considered here.

It is worth noting that, for the proposed interpolation and derivative calculation approaches to work in every possible condition, the values of x and y must be initially saturated within

$$\begin{cases} x \geq X_{\min} \\ x \leq X_{\max} - \varepsilon\,\Delta X \end{cases}, \quad \begin{cases} y \geq Y_{\min} \\ y \leq Y_{\max} - \varepsilon\,\Delta Y \end{cases}, \quad (7.59)$$

where $\varepsilon \ll 1$.

Chapter 8

Conclusions and Outlook

This chapter summarizes the content of this dissertation, highlighting the most significant findings and research contributions. Furthermore, an outlook on potential improvements and future developments is provided.

8.1 Results and Summary

This thesis has dealt with the analysis, design, control and experimental assessment of a modular converter concept for electric vehicle (EV) ultra-fast charging, addressing the strict requirements and the multiple challenges related to the application. In particular, in view of the maturity, reliability and cost-effectiveness of silicon (Si) semiconductor devices, full-Si converter prototypes of the AC/DC and DC/DC stages have been built with the goal of providing an efficiency benchmark (i.e., $> 95.5\,\%$) for full-Si ultra-fast charger implementations. The main results of this thesis are summarized in the following, divided according to the respective chapters.

PART I: AC/DC Converter

- **Chapter 2: Analysis**
  A comprehensive analysis of the grid-tied AC/DC conversion stage of the EV ultra-fast charger module has been provided. A unidirectional three-level T-type rectifier structure has been selected, owing to its promising features such as low semiconductor count, active switches with reduced voltage rating, three-level AC voltage waveforms and split DC-link output. Therefore, the operational basics of three-level unidirectional rectifiers have been described with a particular focus on the zero-sequence voltage injection limits, which have been shown to determine

the maximum modulation index, the feasible power factor angle range and the mid-point current generation limits. The three-level pulse-width modulation process has been described and seven different modulation strategies have been introduced. In particular, the zero mid-point current modulation (ZMPCPWM) has been selected as the most suited modulation strategy for the present application, as it ensures minimum low-frequency DC-link mid-point voltage oscillation. Finally, with the goal of providing straightforward tools for the design of the rectifier, the converter active and passive component stresses have been extensively assessed analytically and/or numerically, including the semiconductor losses, the DC-link RMS current and charge ripple, and the AC-side inductor RMS and peak-to-peak flux ripple. Such comprehensive analytical assessment is a contribution of this work.

- **Chapter 3: Design**
  A complete design methodology for the considered 60 kW unidirectional three-level T-type rectifier has been described. In view of the high target nominal power, a six-leg (i.e., dual three-phase) converter structure has been adopted, halving the current rating of each bridge-leg and thus allowing for the adoption of discrete Si semiconductor devices (i.e., MOSFETs and diodes). Therefore, a step-by-step converter design procedure has been reported, describing the selection, sizing and/or optimization of all main converter active and passive components, including the semiconductor devices, the DC-link capacitors, the AC-side inductors and the heat dissipation system (i.e., heatsink and fans). Furthermore, the adopted models for the estimation of the component losses have been described. Finally, a converter prototype has been built and its performance in terms of loss and efficiency has been assessed experimentally, successfully achieving the required 98.5 % efficiency in nominal operating conditions. The validity of the proposed design procedure and the adopted loss models has been supported by the excellent agreement between analytical/numerical estimations and experimental results.

- **Chapter 4: Control**
  This chapter has presented the design, tuning and experimental assessment of the adopted digital multi-loop control strategy for the considered three-level unidirectional AC/DC converter. To accurately design the four control loops (i.e., dq-currents, DC-link voltage, DC-link mid-point voltage deviation), the system state-space equations have been exploited to derive a fourth-order small-signal model of the three-level rectifier. The controllers have then been accurately tuned, taking into account the delays and the discretization introduced by the digital control implementation and compensating for the plant non-linearities. Finally, the steady-state and dynamical performances of the proposed multi-loop control strategy have been verified in

circuit simulation and experimentally on the T-type rectifier prototype, adopting a general purpose microcontroller unit (MCU) for the digital control implementation (i.e., running at 20 kHz). Overall, the designed control loops have achieved all requested features, namely sinusoidal input current shaping with low THD under all operating conditions (i.e., with non-unity power factor and unbalanced split DC-link loading), fast response dynamics and strong disturbance rejection.

PART II: DC/DC Converter

- **Chapter 5: Analysis**
  An overview of the most adopted topologies for EV battery charging has been provided and a resonant LLC converter has been selected for the present 4x15 kW application, owing to its promising features such as high conversion efficiency (i.e., due to the soft-switching operation of both primary-side transistors and secondary-side diodes) and wide output load/voltage regulation capability. The operational basics of the LLC converter have been described, with particular focus on the first harmonic approximation (FHA) analysis method. This simplified approach has been exploited to identify the converter feasible operating region in terms of switching frequency, input/output voltage gain and output load. For a better understanding, the LLC time-domain waveforms under boost-mode operation (i.e., below resonance), unity-gain-mode operation (i.e., at resonance) and buck-mode operation (i.e., above resonance) have been shown and described. Additionally, the zero-voltage switching (ZVS) mechanism of the primary-side transistors has been explained in detail and the zero-current switching (ZCS) operation of the secondary-side diodes has been briefly discussed. Finally, with the aim of providing straightforward tools for the design and assessment of the LLC converter, the stresses on the converter active and passive components (i.e., semiconductor devices, resonant capacitor, resonant inductor, transformer, input/output filter capacitors) have been derived analytically with FHA and calculated numerically with the more accurate time-domain analysis (TDA). Such exhaustive analytical assessment was not available in literature and is therefore a contribution of this thesis.

- **Chapter 6: Design**
  The complete step-by-step design process of the DC/DC converter stage has been reported. A novel iterative design procedure for resonant LLC converters, aimed at minimizing the total converter conduction losses, has been proposed and described in detail. This procedure has been then applied to the considered modular 4x15 kW application, assuming an unconventional LLC circuit structure to split the power rating of the magnetic components (i.e., enabling the use of commercially available

magnetic cores) and the current rating of the output rectifier diodes (i.e., allowing for the adoption of discrete Si semiconductor devices). Being hardly available in literature, the selection, sizing and/or optimization of all main converter active and passive components has been performed, including the semiconductor devices (i.e., MOSFETs and diodes), the resonant capacitor, the resonant inductors, the isolation transformers, the input/output filter capacitors and the heat dissipation system (i.e., heatsink and fans). Furthermore, the adopted models for the estimation of the component losses have been reported. Finally, a 15 kW LLC converter prototype has been built and its performance in terms of loss and efficiency has been assessed experimentally, achieving a nominal efficiency of 97.6 %, successfully satisfying (and exceeding) the initial design requirements. The validity of the proposed design procedure and the accuracy of the adopted loss models has been supported by the good agreement between analytical/numerical estimations and experimental results.

- **Chapter 7: Control**
  This chapter has presented the design, tuning and experimental assessment of the adopted digital multi-loop control strategy for the considered LLC resonant DC/DC converter. A novel simplified dual first order small-signal model of the LLC converter has been derived from the well-known seventh order model, aiming to provide a straightforward tool for the design of the closed-loop controllers. Therefore, a dual-loop control scheme consisting of an outer voltage loop and an inner current loop has been designed and a complete analytical tuning procedure for both controllers has been described. In particular, the non-linear behavior of the frequency-to-current transfer function has been counteracted by a real-time controller gain adaptation process ensuring constant control bandwidth. To achieve best compensation accuracy, the adaptive gain values have been derived from a static switching frequency LUT obtained by experimental characterization of the converter. Moreover, the steady-state switching frequency value has been fed forward at the output of the current loop regulator to further enhance the system dynamical performance. The effectiveness of the proposed control strategy has been verified both in simulation environment and experimentally on the 15 kW LLC converter prototype, adopting a general purpose MCU for the digital control implementation (i.e., running at 20 kHz). In particular, the reference step response, the sinusoidal reference tracking ability and the input DC-link voltage ripple rejection degree of the current control loop have been assessed. The results have demonstrated the quasi-constant closed-loop bandwidth of the proposed control strategy across the complete converter operating range (i.e., variable load and voltage gain) and its superior dynamical performance with respect to a state-of-the-art solution based on a PI regulator.

Remarkably, combining the results of the AC/DC and the DC/DC stages, a total converter efficiency of 96.0 % has been achieved in nominal operating conditions, outperforming all commercial EV ultra-fast chargers reported in **Table 1.1** (i.e., which however may include additional loss components not considered herein, such as filters, wirings, contacts, etc.).

8.2 Future Developments

Although silicon (Si) is currently the most mature, reliable and cost-effective semiconductor technology, a new generation of ultra-fast battery chargers will be unlocked by modern wide bandgap (WBG) semiconductor devices, such as silicon carbide (SiC) MOSFETs and gallium nitride (GaN) high electron mobility transistors (HEMTs). These devices feature outstanding properties such as low specific on-state resistance, fast switching and high-temperature operation capability [187–190]. These properties, together with advanced converter topologies and/or modulation strategies [50, 191], will unlock unprecedented performance at the converter level, simultaneously pushing the boundaries of achievable power density and conversion efficiency [192–194]. Nonetheless, the adoption of SiC and GaN semiconductors will bring along several new challenges related to e.g. PCB layout, gate driving, increased electromagnetic interference (EMI), etc., requiring a major research and development effort from both industry and academia.

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