M 25364

Reg. No. : .....

Name : .....

VI Semester B.Tech. Degree (Reg./Supple./Improv. – Including-Part Time) Examination, May 2014
(2007 Admn. Onwards)
PT 2K6/2K6 EC 606 (A) : DESIGNING WITH VHDL

Time : 3 Hours Max. Marks : 100

***Instruction** : Answer **all** questions.*

1. a) What is an architecture in VHDL ?

   b) Implement a 4 : 1 MUX using 'when-else' statement.

   c) What is operator overloading ?

   d) Write a note on function kind attributes.

   e) What is the significance of writing a test bench in VHDL ?

   f) Differentiate between observability and controllability of circuits.

   g) What is Metastability ?

   h) Differentiate CPLD with FPGA.

2. a) Write a VHDL program to find the factorial of a given number.

   OR

   b) Compare the different types of architectural models used in VHDL.

3. a) Write a note on functions and procedures used in VHDL.

   OR

   b) Using 'Generic', implement a parity detector in VHDL.

P.T.O.

4. a) With an example, illustrate how to design a circuit that is free from all stuck-at faults.

OR

b) Implement a circuit that can detect the presence of three consecutive ones in a given input sequence of numbers.

5. a) What is clock skew ? With examples illustrate how to overcome the problem of clock skew in synchronous circuits.

OR

b) With a block diagram, explain the configuration of an FPGA.
