Nirma University

Institute of Technology

Supplementary Examination (SPE), August - 2022

B. Tech. in Computer Science and Engineering, Semester-IV

2CS401 Computer Architecture

Roll / Exam No. _____ Supervisor's initial with date _____

Time: 3 Hours Max. Marks : 100

Instructions:
1. Attempt all questions.
2. Figures to right indicate full marks.
3. Use section-wise separate answer book.
4. Draw neat sketches wherever necessary.

SECTION – I

Q-1 Answer the following Questions **[24]**

A CO2, BL3 Write a program to evaluate the arithmetic statement [08]
$X = [A + B - C * (D * E - F)] / [G + H * K]$
a) Using a general register computer with two address instructions
b) Using a general register computer with zero address instructions

B CO2, BL3 The content of PC in the basic computer is 3AF. The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. [08]
a) What is the instruction that will be fetched and executed next?
b) Show the binary operation that will be performed in the AC when the instruction is executed.
c) Give the contents of registers PC, AR, DR, AC, and IR in hexadecimal and the values of E, I, and the SC in binary at the end of the instruction cycle.

C CO2, BL6 Assume that the following changes are made in the basic computer: The hardwired control unit is replaced by the microprogrammed control unit; The size of control memory is 128 X 20. There are two registers SBR and CAR available in the control unit; A microprogram can use eight consecutive memory locations in the control memory. The microinstruction is of 20 bits and contains the following fields: [08]

F1 (3 bits)	F2 (3 bits)	F3 (3 bits)	CD (2 bits)	BR (2 bits)	AD (7 bits)

a) Formulate the correct mapping procedure for this computer
b) Give the symbolic microprogram for the following instructions of the basic computer:
ADD (Opcode : 100) : AC ← AC + M[EA]
BRANCH (Opcode : 101) : If(AC < 0) then PC ← EA
c) Specify the symbolic routines for Fetching the instruction and

reading the effective address phases of the instruction cycle. Assume the necessary values for the fields of a microinstruction. Instruction format of the basic computer is of 16 bits and the opcode is of 3 bits. State your assumptions clearly. The content of AC should not be changed unless it is specified in the instruction.

Q-2 Do as directed **[14]**

A CO3, BL4 Give the design of overlapped register window configuration for a computer having 85 registers and six procedures P1, P2, P3, P4, P5 and P6. Adjacency of procedures is defined as follows: P3 is adjacent to P1 and P6. P2 is adjacent to P1 and P5. P5 is adjacent to P2 and P4. P4 is adjacent to P5 and P6. P6 is adjacent to P3 and P4. There are 13 global registers and 5 common registers between two adjacent procedures. Also specify the window size for each procedure. [08]

B CO3, BL6 Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for the first two stages. [06]

S	Cin = 0	Cin = 1
0	F = A + B (add)	F = A + 1 (increment)
1	F = A – 1 (decrement)	F = A + B' + 1 (subtract)

Q-3 Do as directed **[12]**

A CO2, BL3 Derive the control gates associated with the program counter PC in the basic computer and design a circuit for the same. [06]

OR

A CO2, BL6 Design the inter-connection of all the basic computer registers through a common bus. Also specify the purpose and size of each and every register used in terms of number of bits. Assume the memory size to be considered is 4096 x 16. [06]

B CO2, BL4 The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A three word call subroutine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1122. What are the content of PC, SP, and the top of the stack: [06]

a) before the call instruction is fetched from memory?
b) after the call instruction is executed?
c) after the return from subroutine?

OR

B CO2, BL4 A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W+1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is [06]

a) Direct b) Indirect c) Relative d) Indexed

SECTION – II

Q-4 Answer the following Questions **[24]**

A CO1, BL4 In certain scientific computations, it is necessary to perform the arithmetic operation $(A_i * B_i) + (C_i * D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all the registers in the pipeline for tasks i = 1 to 7. Also design a space time diagram for the same. [08]

B CO1, BL5 Show the multiplication of (+14) x (-23) using Booth's algorithm. For each step, give the contents of all the registers, flipflops and counters involved in the process. [08]

C CO3, BL5 Show the division of 123 by 12 using restoring method. For each step, give the contents of E, A, Q, B and SC involved in the process. Assume that the registers with minimum required storage capacity are available. [08]

Q-5 Do as directed **[14]**

A CO2, BL3 Consider the following instructions to be executed using a RISC pipeline: [08]

LOAD from memory to R1
DECREMENT R2
ADD R3 TO R4
ADD R2 to R1
ADD R5 AND R6
BRANCH TO ADDRESS X

a) Design the three segment RISC instruction pipeline for the above instructions by inserting the minimum number of no operation instructions to avoid the conflict.
b) Redesign the same pipeline by removing the no operations to achieve the minimum number of clock cycles.

B CO2, BL6 Assume that a computer system needs 512 bytes of RAM and 512 bytes of ROM. Consider the RAM chips available are of 128 x 8 size and ROM chips available are 512 x 8 size. [06]

a) Design the connection of memory chips to the CPU for the specified configuration
b) Specify the memory address map table for the same

Q-6 Do as directed **[12]**

A CO3, BL2 Design the block diagram to show the configuration of daisy chaining priority mechanism. Give the logic of priority interrupt hardware and one stage of priority arrangement. [06]

OR

A CO3, BL2 Design and explain the block diagram of Associative memory. How is the Match Logic for the same formulated? [06]

B **CO3, BL3**	Design an array multiplier to multiply two 3-bit numbers.	[06]

OR

B **CO3, BL3**	A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. a) How many bits are there in the tag, index, block and word fields of the address format? b) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit. c) How many blocks can the cache accommodate?	[06]