BE ETRX - VIII (R) Advance VLSI design L.B

Con. 3263–11. **(REVISED COURSE)** **RK–4644**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.

2) Attempt any four out of remaining six questions.

3) Assume any suitable data wherever required but justify the same.

1. a. Determine intrinsic gate capacitance with 20
t_{ox}= 150A^0, ε_{0x}= 3.9 x8.85x10^{-14} F/cm, and V_G=3.3 Volts
if W=4 μm L=2μm

b. Explain the need of interconnect delay model? Also define Cross-talk in case of VLSI design.

c. Explain the factors on which dynamic power dissipation depends?

d. Explain the parameters to be taken care while design of the adder circuit.

e. Draw the analog design octagon and explain its significance.

2. a. Explain how process variation can cause variation in speed? Explain the concept of Design Corner. 10

b. Draw the schematic of Carry look ahead adder explain how the speed can be improved? 10

3. a. What are the issues of clock distribution? Explain how they are addressed? Also explain how the cross-talk in multilayer system is modeled? 10

b. State the need of Input and Output circuit? Explain with neat diagram the schematic and design consideration for the same. 10

4. a. Implement the following function using NOR-NOR implementation for a PLA 10

i. Y_1=ac+b'c

ii. Y_2= abc+-a'b'c

iii. Y_3=-a'b + ab

b. Explain the clock generation and different types of clocking schemes for VLSI circuit Explain what do you mean by clock skew and clock jitter and how it can be estimated 10

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5. a. Find resistance Rn for nMOS if electron mobility $\mu_n = 560 cm^2/V\text{-sec}$ 10

$t_{ox} = 10$ nm , $\varepsilon_{0x} = 3.9 \times 8.85 \times 10^{-14}$ F/cm , and $V_G = 3.3$ Volts

$V_{THn} = 0.7$ Volts

i) if W=10μm L=0.5μm

ii) if channel width is increased to a value of W=22μm while the channel length remains same.

b. Explain how propagation delay caused by distributed Resistance-Capacitance (RC) in the long wire can be reduced? Derive the expression to neglect the wire-length delay with respect to gate delay 10

6. a. Explain the three knobs on the basis by which CMOS designer optimize the speed of CMOS gate Explain how to approximate calculation of power dissipation at increasing accuracy 10 10

b. State the need and various applications of analog VLSI circuit design. Why analog circuit design is is difficult as compare to digital design?

7. Write a short note on (any four) : 20

a. Charge sharing and transistor sizing.

b. Different clock system

c. The role of sense amplifier

d. Flash cell construction and working

e. Telescopic cascade op-amps

f. Switched capacitor Amplifier