Reg. No. : .....

Name : .....

K15F 0298

V Semester B.Tech. Degree (Reg./Supple./Imp-Including Part Time) Examination, November 2015

(2007 Admn. Onwards)

PT 2K6/2K6 EC 504 : COMPUTER ORGANISATION AND ARCHITECTURE

Time : 3 Hours

Max. Marks : 100

*Instructions : Q – **I** **All 8** questions **Compulsory**. Q – **II** to Q – **V** answer **A** or **B**.*

PART – A **(8×5=40)**

I. a) Write short note on subroutines.

b) Differentiate between Register, Immediate and Shifted Immediate operands.

c) Explain the sequence of operations for fetching a word from memory.

d) What is PLA ? Explain.

e) Write a note on various disk performance parameters.

f) Explain LRU replacement algorithm.

g) Explain the term Vectored Interrupts.

h) What are the characteristics of RISC architecture ?

PART – B **(4×15=60)**

II. A) i) Explain Booth's Algorithm with an example. **10**

ii) Explain how performance of a computer can be measured. **5**

OR

P.T.O.

B) i) Briefly explain about the basic functional units of a computer. 8

ii) What is an addressing mode ? Explain different types of addressing modes. 7

III. A) Explain the following :

i) Hard wired Control 8

ii) Microinstructions. 7

OR

B) i) Write a short note on microprogram sequencing. 10

ii) What is the advantage of prefetching microinstructions ? Explain. 5

IV. A) i) Explain in detail about Mapping functions of cache memory. 10

ii) Compare and contrast DRAM and SRAM. 5

OR

B) i) Explain in detail about RAID. 10

ii) What is the purpose of a Translation Look aside Buffer ? Explain.. 5

V. A) i) Discuss in detail about Direct Memory Access. 10

ii) Briefly explain about the types of parallel processor systems proposed by Flynn. 5

OR

B) i) What is cache coherence ? Describe the different software and hardware solutions to deal with the cache coherence problem. 8

ii) Explain about symmetric multiprocessor organization with the help of a diagram. 7