SEM-VI(R) - ETRX - Comp Organisation
9/May - 2012

Con. 4843-12. **GN--9707**

(3 Hours) **[Total Marks : 100**

N.B. **(1)** Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Solve using Booth's algorithm. 5
Multiplicand (M) = –7 (1001),
Multiplier (Q) = 3 (0011)
A = 0000.
(b) Write microinstructions for instruction Add R_0, [R_3]. 5
(c) Draw the register structure of IA 32 family. 5
(d) What happens when the following ARM instructions are executed ? 5
(i) MLA R4, R3, R7, R8
(ii) BL func.

2. (a) Explain the concept of Cache memory with reference to the principle of locality of reference, hit ratio and different Cache architectures. 10
(b) Explain how a virtual address is converted into physical address using paging. Also explain TLB. 10

3. (a) What is bus arbitration ? Explain different techniques for bus arbitration. 10
(b) Explain input and output operation in asynchronous bus with the help of timing diagrams. 10

4. (a) What is microprogramming ? Draw and explain microprogrammed control unit. 10
(b) Consider a Cache consisting of 128 blocks of 16 words each, for a total of 2048 (2k) words and assume that the main memory is addressable by a 16 bit address and it consists of 48 blocks. 10
How many bits are there in each of the TAG, SET and WORD fields for different mapping techniques i.e.
(i) Direct
(ii) Associative
(iii) 2-way set associative.

5. (a) Draw flowchart for restoring division method and explain using diagram steps for performing restoring division using numbers Dividend = 8 and Divisor = 3. 10
(b) What is pipelining ? Explain data hazard and code hazard in pipelining. 10

6. (a) What are various steps taken by the CPU in interrupt processing ? Explain how multiple devices share a single interrupt line. 10
(b) Explain different addressing modes of an IA-32 processor with example. 10

7. (a) Explain register structure in ARM family architecture. 10
(b) What is the necessity of replacement algorithm ? Show how pages are replaced between Cache memory and main memory using replacement policies :— 10
(i) LRU (ii) FIFO (ii) LFU.