ETRX 7/6/13

T.E Sem VI Rev. Course M/J-2013

Elective I : CO

ws Feb. 2013-(f) 30

Con. 10047–13. **GS–1513**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Explain restoring division algorithm using an example and draw its flowchart. **5**
   (b) Write microinstructions for the instruction Add R_o, $[R_3]$. **5**
   (c) Draw register structure of IA-32 family. **5**
   (d) Explain in brief using memory segmentation how 64 Terabytes of virtual memory address can be accessed. **5**

2. (a) Multiply following using Booth's algorithm : **10**
      (i) (–4) * (–9)
      (ii) (–7) * (3).
   (b) Compare horizontal microprogramming with vertical microprogramming. **10**

3. (a) Explain various characteristics of memory. **10**
   (b) What is the necessity of replacement algorithm ? Show how pages are replaced between cache and main memory using replacement policies : **10**
      (i) LRU (ii) FIFO (iii) LFU.

4. (a) Explain register structure in ARM family architecture. **10**
   (b) Write various DMA transfer modes in brief with suitable example. **10**

5. (a) What is bus contention ? How is it resolved by using bus arbitration ? Explain various bus arbitration methods. **10**
   (b) Design a 4 bit fast adder (carry look ahead adder). **10**

6. (a) Explain concept of cache memory with reference to principle of locality, Hit ratio and draw and explain different cache architectures. **10**
   (b) What happens when the following ARM instructions are executed ? **10**
      (i) MUL R_1, R_2, R_3
      (ii) BL target
      (iii) ADDS R_2, R_3, R_4
      (iv) RSBLES R_1, R_2, # 5.

7. (a) What are different addressing modes of IA-32 family ? Explain with example. **10**
   (b) What is virtual memory ? How paging is useful in implementing virtual memory ? **10**
